AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Status of LumiCal Readout Electronics

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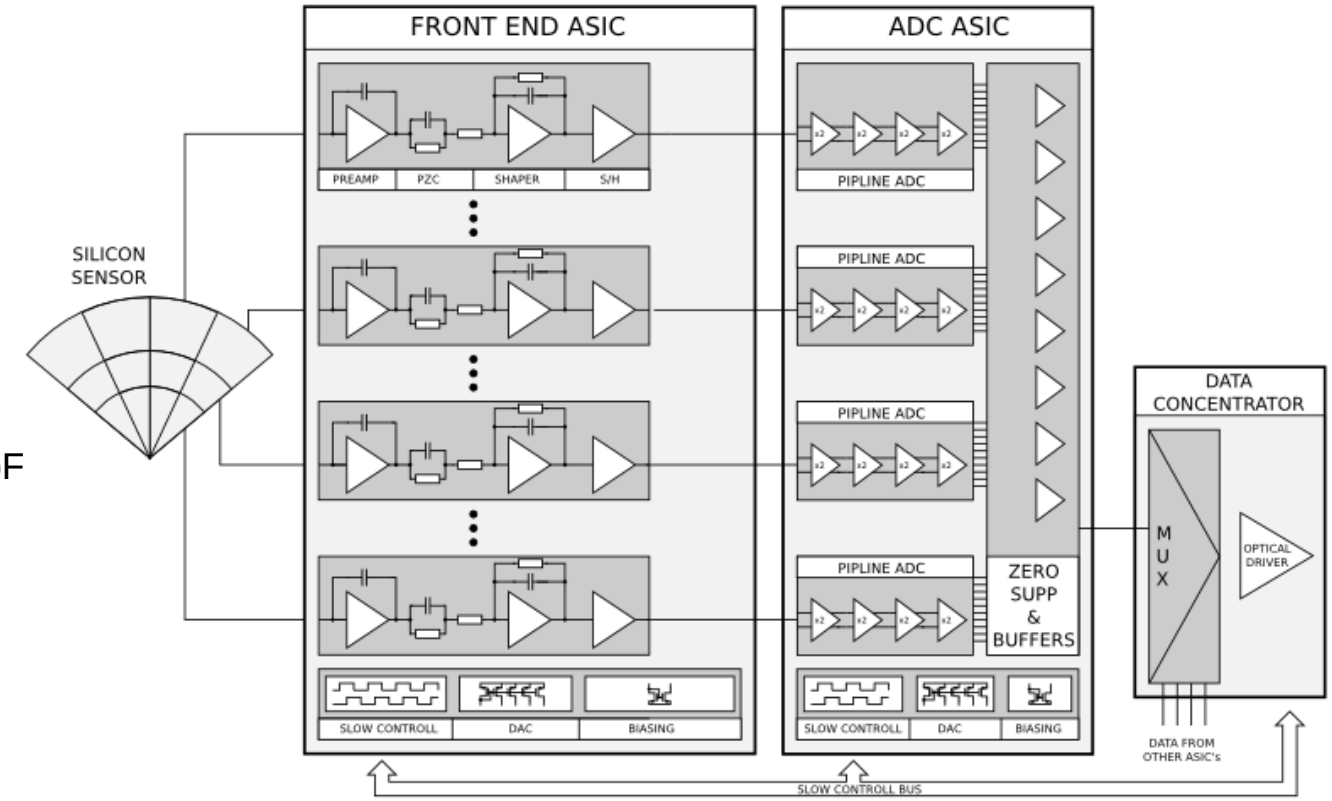
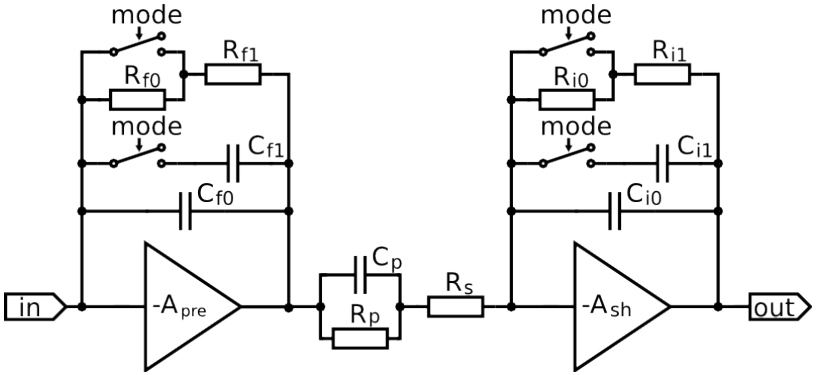
Readout architecture of LumiCal detector

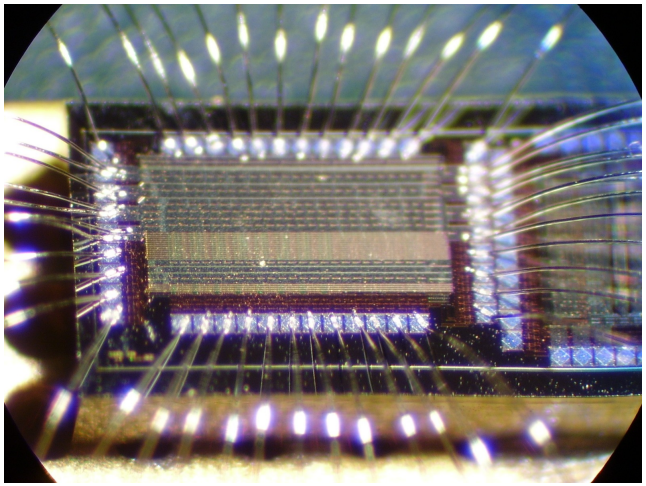


Cdet 10-30 pF

In last few years works on architecture comprising front-end and ADC in each readout channel have been carried. The idea was to have readout chain consisting of two ASICs (FE, ADC) and to complete it with FPGA based data concentrator.

Front-end ASIC





Existing prototypes:

8 channels in AMS0.35um

Cdet ≈ 0 ÷ 100pF (in new specs: Cdet<30pF)

1st order shaper (Tpeak ≈ 60 ns)

Variable gain:

calibration mode - MIP sensitivity (~4fC)

physics mode - input charge up to 10 pC

Power switching off NOT implemented

Designed for OLD specifications

Prototypes fabricated and tested

power consumption 8.9 mW/channel

event rate up to 3 MHz

Crosstalk < 1%

Multichannel ADC ASIC

8 channels of 10 bit ADC

1.5 bit per stage pipeline architecture

AMS 0.35um technology

Layout with 200um ADC pitch

Digital multiplexer/serializer:

Serial mode (~250MHz): one data link per all channels (max fsmp ~ 3 MSps)

Parallel mode (~250MHz): one data link per channel (max fsmp ~ 25 MSps)

Test mode: single channnel (max fsmp ~50 MSps)

High speed LVDS drivers (<=1GHz)

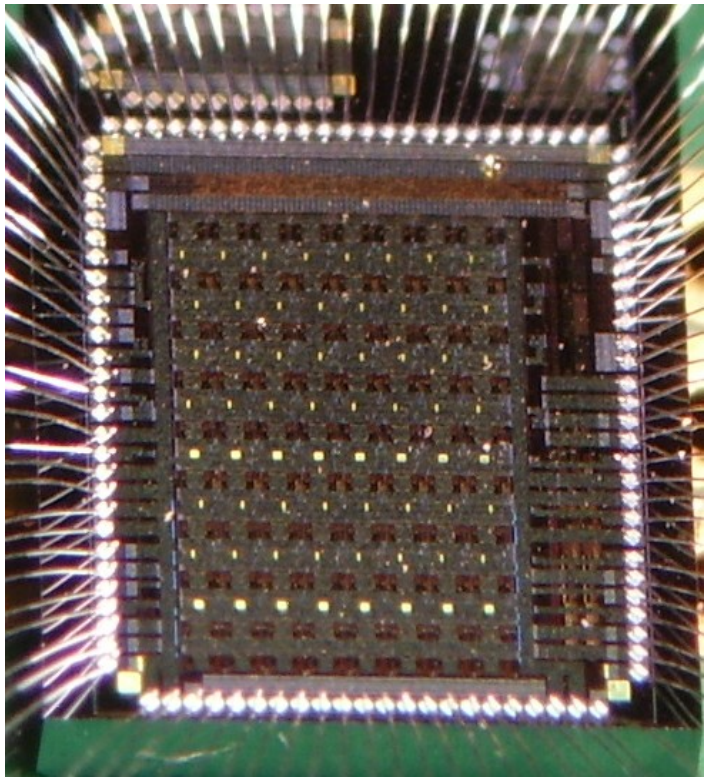
Power pulsing

Precise BandGap reference source

Temperature sensor

ENOB=9.7 bits

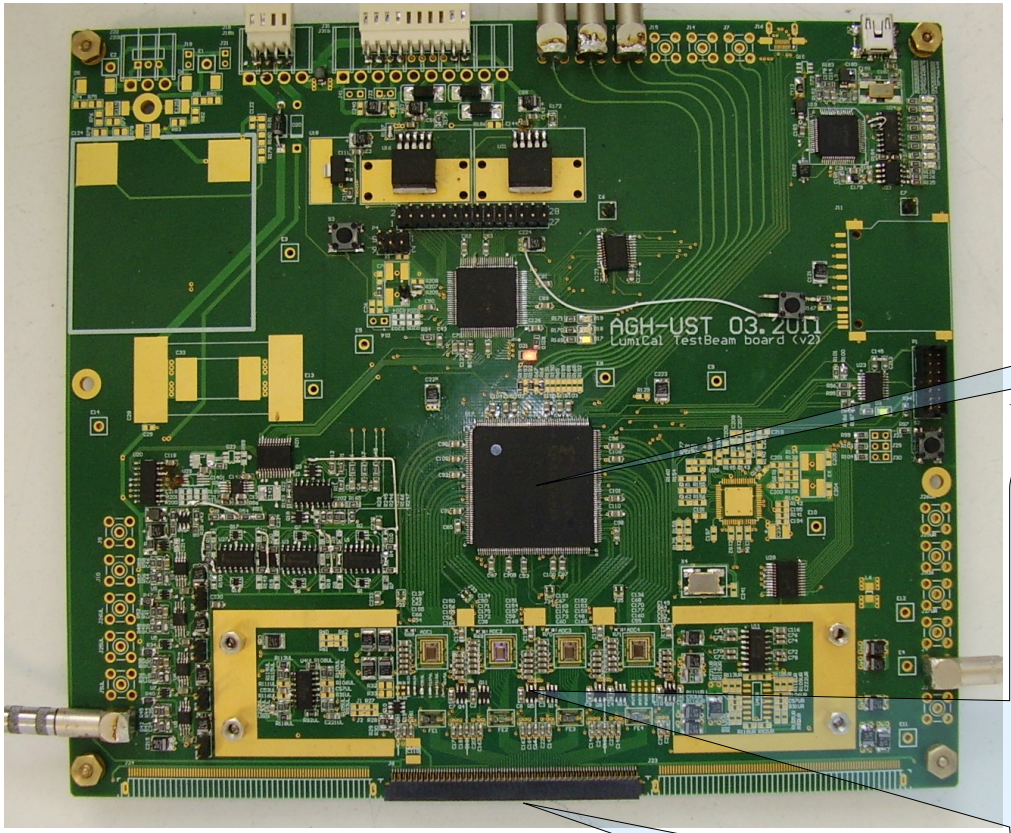
~1.2mW/channel/MHz



2.6mm x 3.2mm

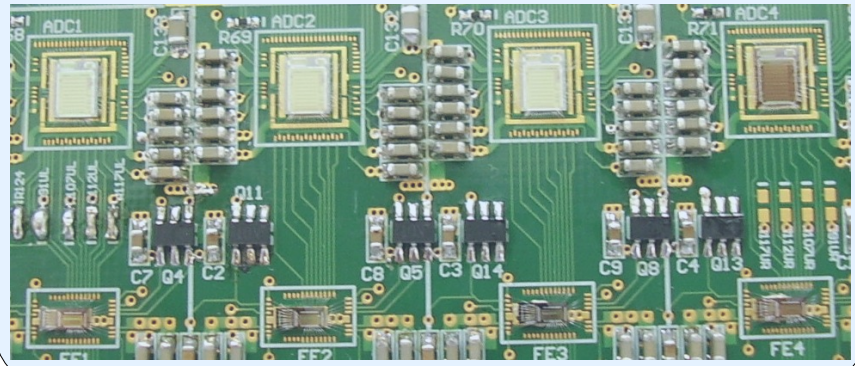
32 channels readout module

4 FE ASICs + 4 ADC ASICs + FPGA concentrator + Power pulsing



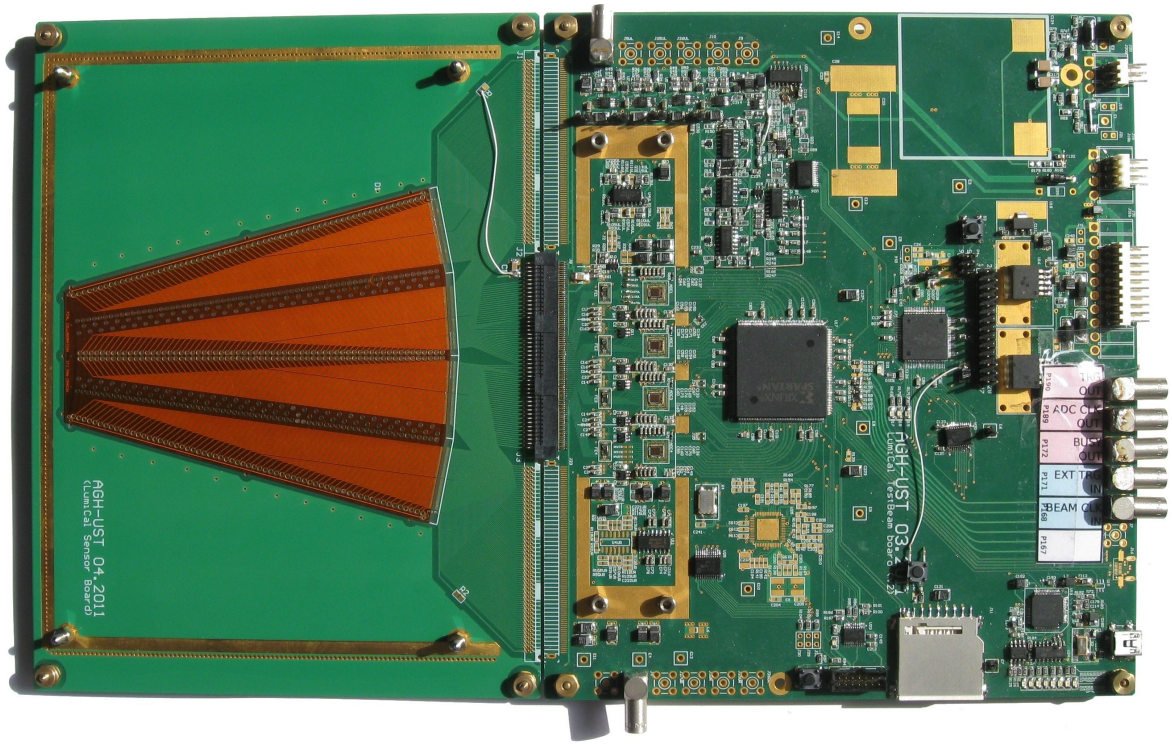
Data concentrator
Xilinx Spartan 3E

4 pairs of front-end + ADC



sensor connector

LumiCal detector module

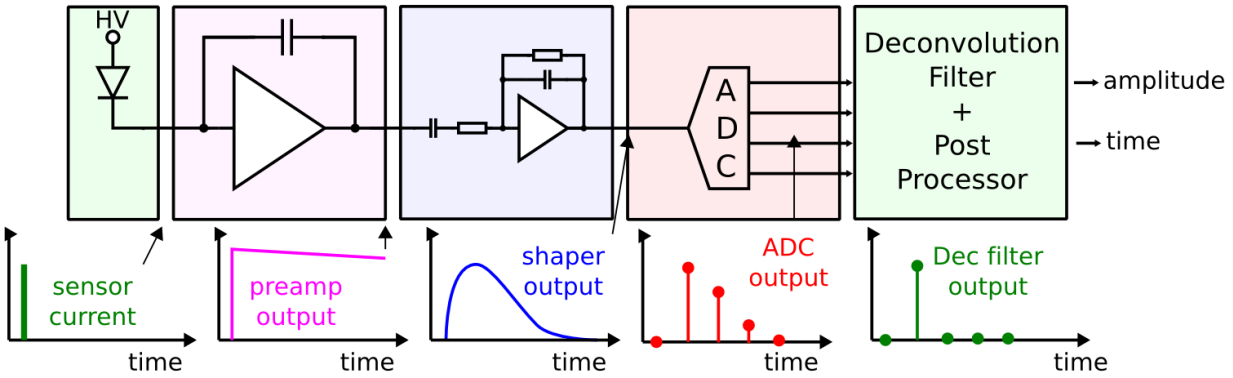


Good performance of detector module verified during july testbeam.

A lot of usefull lab/testbeam measurements and analyses is being, and we hope..., will be done with this module.

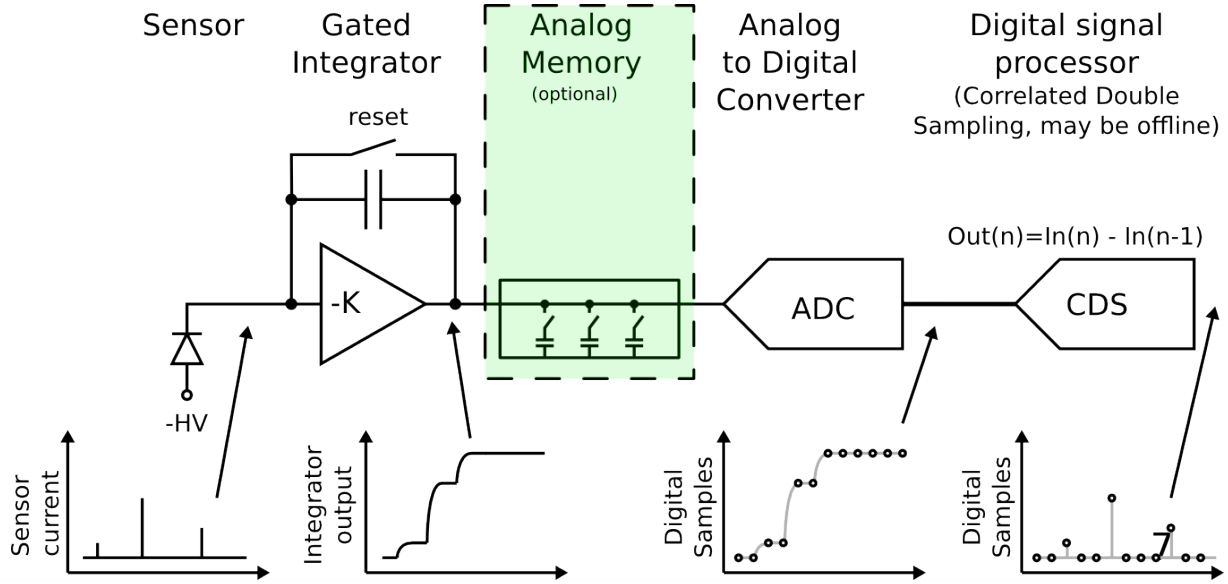
Readout architectures for CLIC

Deconvolution



Look in:

LCD-Note-2011-015

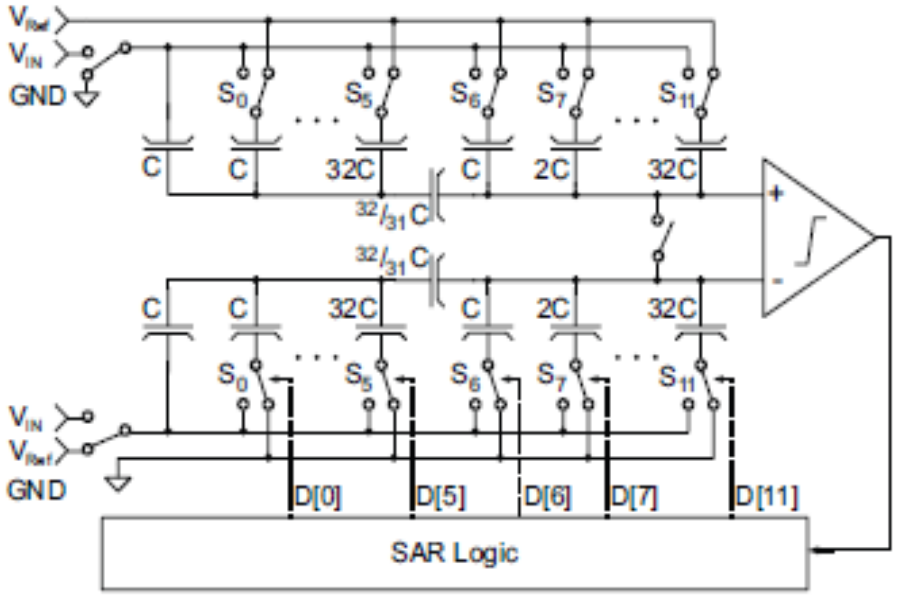


Gated integrator & CDS

What next ???

- Present readout ASICs (FE,ADC) work well and should be used extensively in testbeams and lab to study ILC/CLIC issues.
- No further development-integration of more complex ASICs in AMS 0.35um CMOS foreseen. The main reason is that for final ILC/CLIC detecting system the power consumption and radiation hardness may be not satisfactory with present technology.
- The good choice for future technology seems IBM 130nm CMOS
- New FE and ADC in 130nm need to be designed...
- For ADC decision is simpler since SAR ADC is a perfect candidate for general purpose (ILC/CLIC) very low ADC
  - Design of SAR: 10 bits, up to 50MHz sampling, <2mW power consumption, is underway. We hope to submit it still in 2011.
- For FE there are more questions, design has been started but goes more slowly, submission expected 2011-2012
- Continue studies of readout for CLIC

Segmented/Split capacitor SAR ADC



Typically each of two sub-DACs is split into two (almost) equal capacitor networs connected through coupling capacitor

Instead of 2^N small unit capacitors, $2*2^{N/2}$ larger capacitors are used in split capacitor architecture

Work on such solution in progress...