DRD7 Status Report

Electronics and On-Detector Processing

3rd Workshop on Future Accelerators

Corfu, 1 May 2025

Attilio Andreazza (INFN and University of Milano)

for the DRD7 Collaboration

INFN MILANO

UNIVERSITÀ DEGLI STUDI DI MILANO
DIPARTIMENTO DI FISICA

ECFA Detector Roadmap

- Progresses in Particle Physics require to push the boundary of detector technologies beyond the state-of-art
- **Electronics** is vital to almost **all detector systems**, and modern technologies offer **tremendous opportunities**, for example:
  - Transmission speeds **≥100 Gbps**
  - Extremely **high integration densities**
  - Very high performance **FPGA**s
  - Advanced **interconnection technologies**
- The exploitation of these technologies must face an increase of:
  - the **complexity** of the projects
  - the required **financial** and **human** resources
- Considerations at the base of the ECFA Detector R&D Roadmap

ECFA Detector Roadmap (2)

DRD7 Collaboration

https://cds.cern.ch/record/2901965/

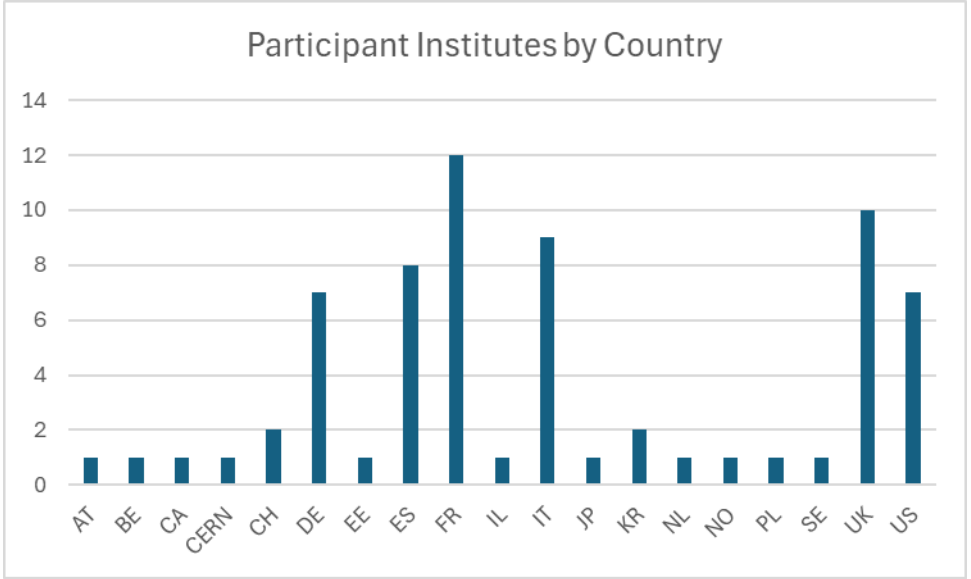
DRD 7: Proposal for an R&D Collaboration on: Electronics and On-Detector Processing

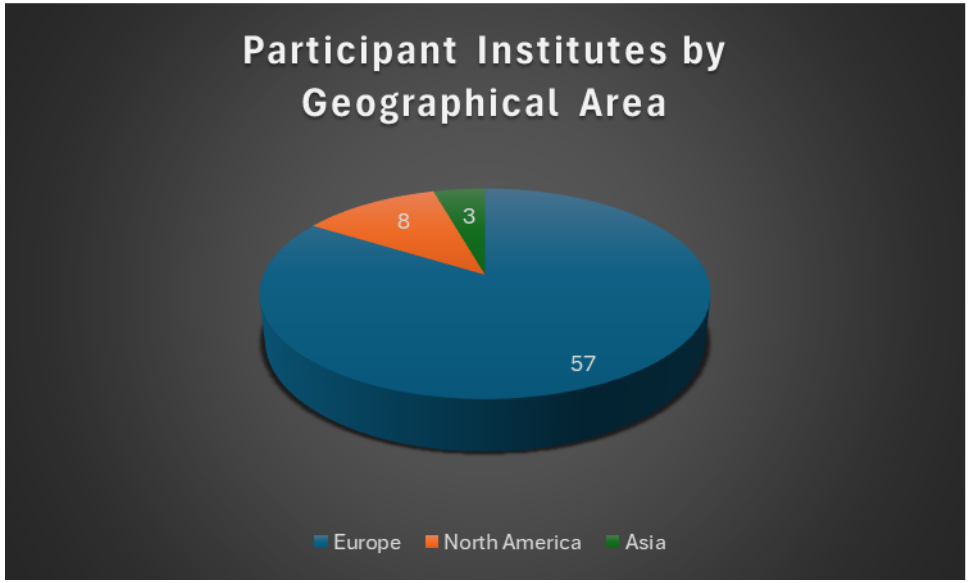
The DRD7 Collaboration

May 21, 2024

Jerome Baudot[1], Marcus French[2], Ruud Kluit[3], Angelo Rivetti[4], Frank Simon[5,*], Francois Vasey[6,*]
(**DRD7 Steering Committee**)

Marlon Barbero[7], Sophie Baron[6] , Giulio Borghello[6] , Michele Caselle[5], Davide Ceresa[6] , Francesco Crescioli[8], Manuel Da Rocha Rolo[4], Oscar Augusto De Aguiar Francisco[9], Conor Fitzpatrick[9], Marek Idzik[10], Kostas Kloukinas[6] , Szymon Kulis[6] , Xavi Llopart Cudie[6] , Niko Neufeld[6] , Jeffrey Prinzie[11] , Iain Sedgwick[2], Walter Snoeys[6] , Jan Troska[6] , Mark Willoughby[2]
(**DRD7 Work Package Conveners**)





Collaboration Proposal approved by DRDC on June 5th 2024

- 67 **Institutes** from 19 **countries**
- 6 **Work Packages**, fitting with the ECFA Detector R&D Roadmap objectives
  - 15 **Projects** (deliverables)
- 1 Transversal **Working Group** on *Tools and Technologies*

Since then, formal collaboration forming process has progressed.

DRD7 Collaboration

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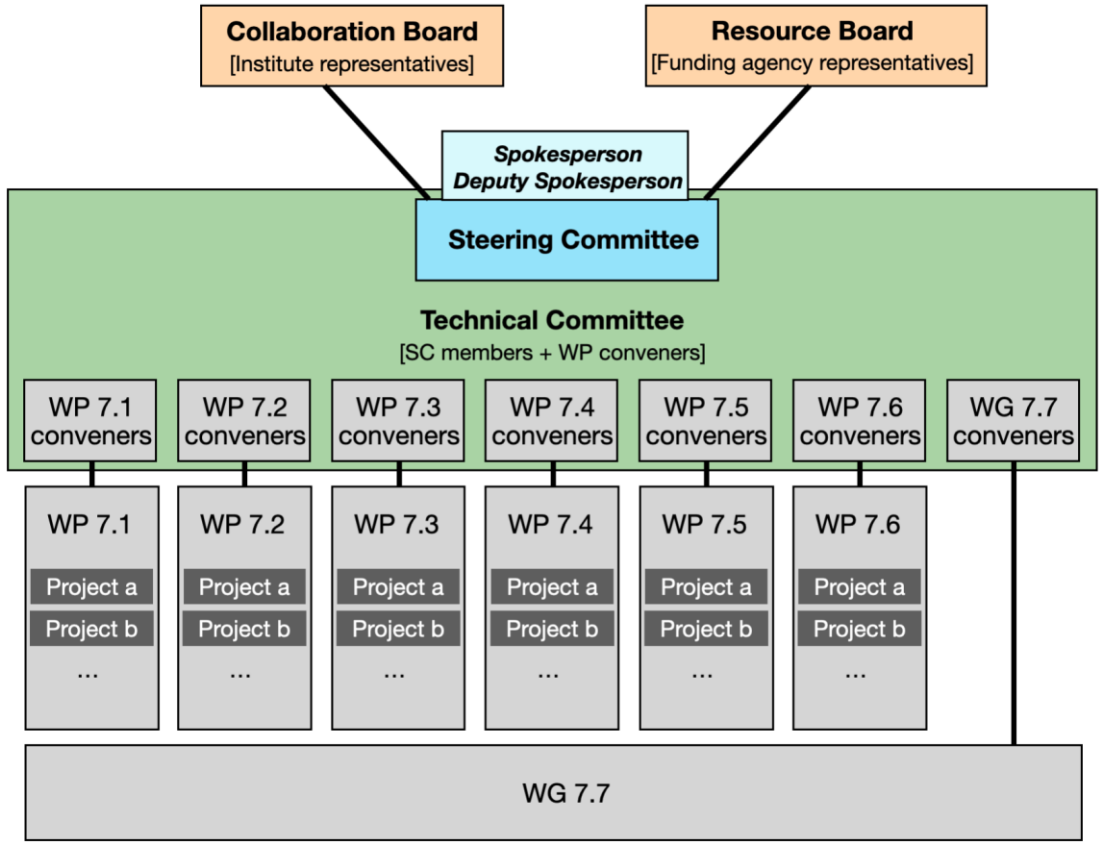

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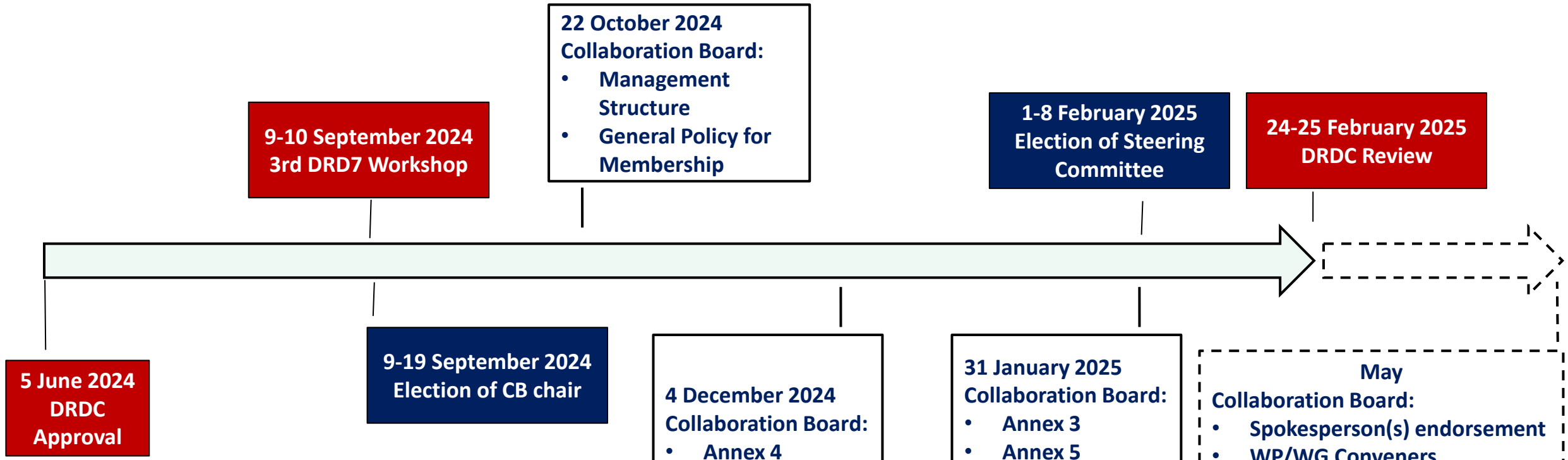
Timeline



Elected management:
Collaboration Board Chair: Attilio Andreazza (Milano), Cristina Fernàndez Bedoya (Deputy, CIEMAT)
Steering Committee: Jerome Baudot (IPHC-Strasbourg), Marcus French (STFC RAL), David Gascón Fora (ICCUB) Katja Klein (RWTH Aachen), Ruud Kluit (NIKHEF), Angelo Rivetti (Uni and INFN Torino), Frank Simon (KIT), Francois Vasey (CERN)

DRD7 Projects

Data density	High data rate ASICs and systems New link technologies (fibre, wireless, wireline) Power and readout efficiency
Intelligence on the detector	Front-end programmability, modularity and configurability Intelligent power management Advanced data reduction techniques (ML/AI)
4D-techniques	High-performance sampling (TDCs, ADCs) High precision timing distribution Novel on-chip architectures
Extreme environments and longevity	Radiation hardness Cryogenic temperatures Reliability, fault tolerance, detector control Cooling
Emerging technologies	Novel microelectronic technologies, devices, materials Silicon photonics 3D-integration and high-density interconnects Keeping pace with, adapting and interfacing to COTS

Must happen or main physics goals cannot be met Important to meet several physics goals Desirable to enhance ... reach Novel needs being met

* LHCb Velo

- 7.1 Data density and power efficiency
  - 7.1a Silicon photonics transceivers
  - 7.1b Powering next generation detector systems
  - 7.1c Wireless allowing data and power transmission
- 7.2 Intelligence on detector
  - 7.2a Radiation Tolerant RISC-V SoC
  - 7.2b Virtual Electronic System Prototyping
- 7.3 4D and 5D techniques
  - 7.3a High Performance ADCs and TDCs
  - 7.3b Characterizing and calibrating sources impacting time measurements
  - 7.3c Timing distribution techniques
- 7.4 Extreme environnements
  - 7.4a: Modelling and development of cryogenics PDKs and IPs
  - 7.4b Radiation resistance of advanced CMOS nodes
  - 7.4c Cooling and cooling plates
- 7.5 Back-end system and COTS
  - 7.5a: DAQOverflow
  - 7.5b: From front-end to back-end with 100 GbE
- 7.6 Complex imaging ASICs and technologies
  - 7.6a: Common access to selected imaging technologies
  - 7.6b: Shared access to 3D integration

General Remarks

- Compared to some other DRDs, DRD7 is a rather small collaboration
  - **No pre-existent large collaboration communities** (like for example RD50, RD42, RD51, RD52, Calice...) joining the DRD framework (RD53 was a very focused effort)
  - Many strongly **detector-oriented electronics development** within their **specific DRDs**
    - Set up **liasons** with the other DRD for common topics and overlapping activities (for example monolithic CMOS sensor with DRD3, or advanced cooling technologies with DRD8)
  - Management of **IP, PDKs** and software **licenses** are particularly relevant withing the electronics community

- Balancing between focused collaboration on **concrete deliverables** and reaching a **wider audience** of users/applications
  - Collaboration **membership** linked to **active contributions**(*) in **projects**
  - **Observer role**, for everybody interesting to follow the technological evolution in view of applications, or eventually interested to contribute to future projects

(*) either funds, infrastructures or personpower

General Remarks

- Similarly to other DRDs, funding structure is complex
  - Memorandum of Understanding, with **commitments to deliverables**
  - Providing **resources for a multiple year time-span**
  - Funding Agencies to be **included** in the project approvals
  - **Not matching the usual R&D funding scheme** from national or multinational sources
    - Approaches differs country-to-country
    - MoU signatories are not always clear;
      sometimes strong indication an MoU will not be explicitly signed
  - Projects usually starting on R&D topics the groups are already pursuing
    - activity progressing on **existing funds** whenever possible: degree of advancement **very different** across projects
    - many group waiting for grants assignment before being able to commit resources
- Some very small groups non linked to existing HEP experiments
  - avoiding common funds to be as inclusive as possible

WP 7.1: Data density and power efficiency

More channels and more bits per sample require higher data rates inside and out of the front-end ASICs.

Novel link technologies must be developed to cope with these higher data rates, including radiation-hard optical links, wireline, wireless, and free-space optics

Achieving new functionalities (like timing) with affordable power budget needs **low-power design** techniques.

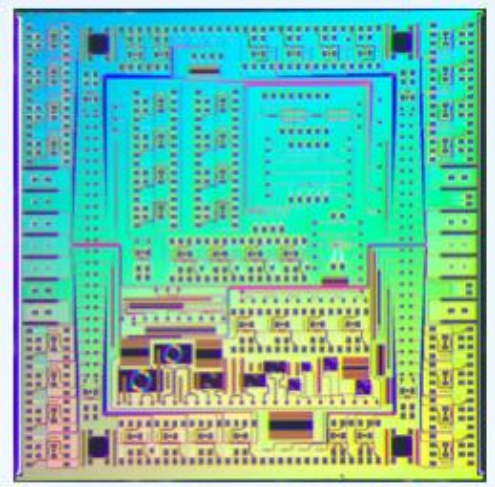
Efficient power **distribution**, power **converters** and **regulator devices**, and protection circuits are required to minimise detector mass and heating.

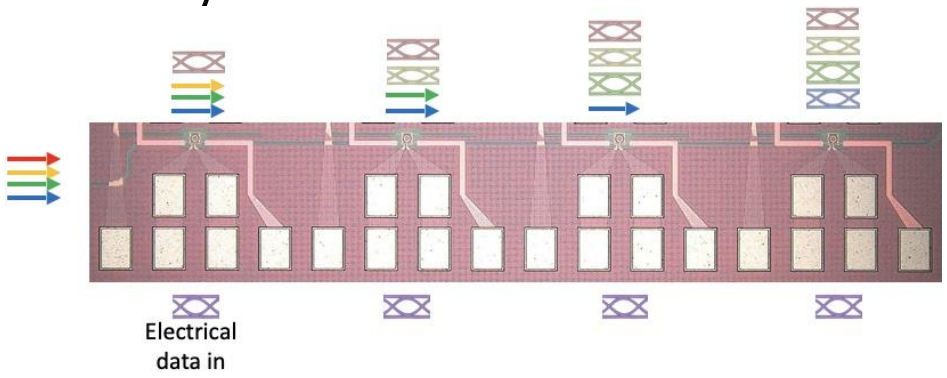
Carry on the development of **low Technology Readiness Level** approaches that may have **disruptive** and **far-reaching** goals

- Conveners: *Szymon Kulis* [CERN], *Jeffrey Prinzie* [KU Leuven], *Jan Troska* [CERN]
- Projects
  a. Silicon photonics transceivers
  b. Powering next generation detector systems
  c. Wireless allowing data and power transmission

Silicon photonics transceivers

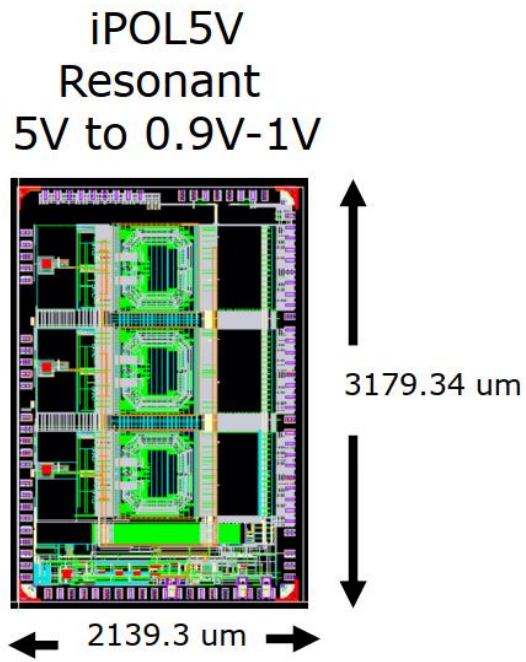
- **Deliverable:**
  High-speed optical transceivers based on Silicon Photonics technology
  - applications from low-temperature neutrino detectors to high-radiation environment HL-HLC pixel detectors
- **Goals:**
  - 100 Gb/s per fibre optical readout with 2.5 Gb/s control optical link
  - Operation at a BER of 10^{-12}
  - Radiation tolerance up to 1×10^{16} particles/cm^2 and 10 MGy
  - Power consumption of 250 mW
  - Cryogenic temperature operation for some lower-speed variants.
- First Photonic Integrated Circuits received and tested for functionality and performance at 25 Gb/s per lane for 100 Gb/s per fibre
- Challenge: System operation across range of environmental conditions, packaging & integration with FEICs
- Community: Canada, CERN, Germany, Italy, Spain, UK, USA

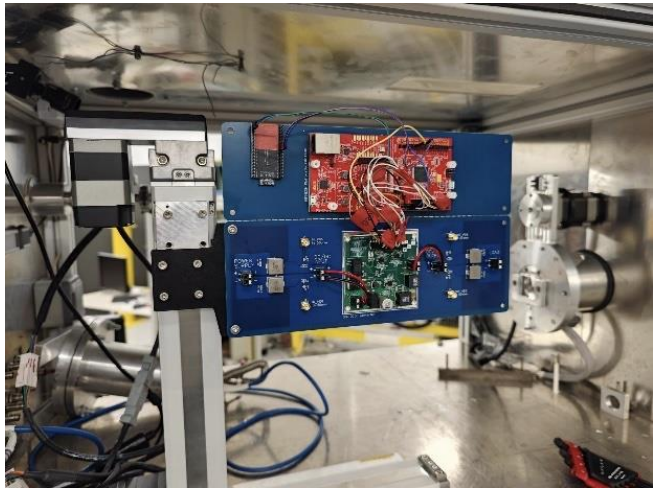




Powering next generation detector systems

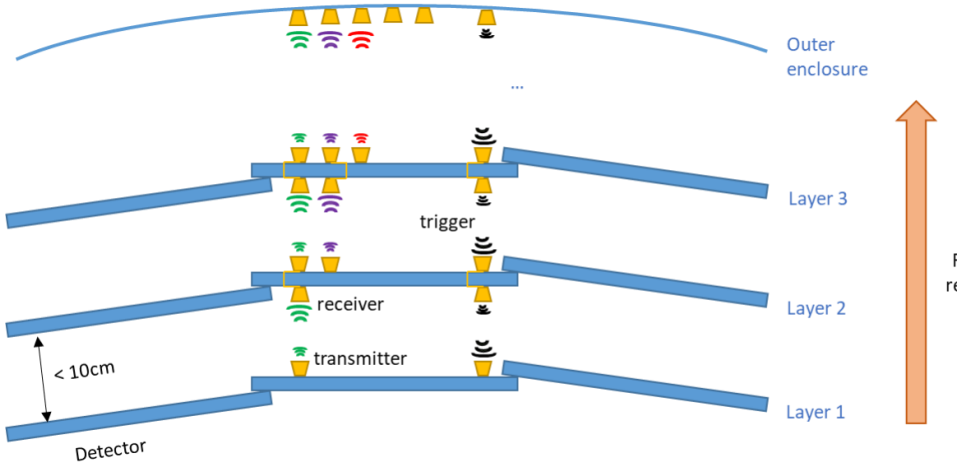
- **Deliverable:**
  Power distribution schemes and their voltage/current regulators and converters.
- **Goals:**
  - Fully integrated DCDC converters in 28 nm technology
    - 75% power efficiency
  - Discrete components DCDC converters using GaN or HV CMOS 0.18µm
    - suitable for serial power chains with 10 A load
    - 90% power efficiency
  - Radiation tolerance up to 1×10^{16} particles/cm^2 and 10 MGy
- Evaluation of prototypes in parallel with design of the fully integrated and GaN-based converter.
- Measurement setups established and radiation testing carried out.
- HV-CMOS module realized for serial power testing: collaboration of designers and evaluation/measurement teams
- Community: Austria, CERN, Estonia, Germany, Italy, Spain



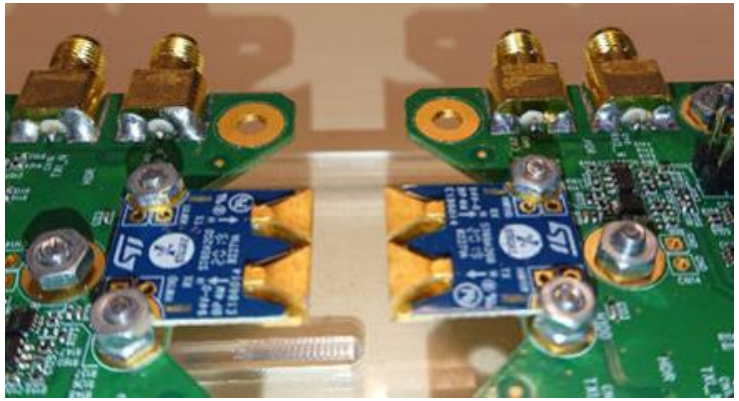


Wireless allowing data and power transmission

- **Deliverable:**
  Wireless technology based on a millimeter wave and Free Space Optics
- **Goals:**
  - Alternative to cables and optical links that may revolutionize the detector design
  - Serialize detector front-end modules as channels up to 10 Gb/s
  - Aggregation across detector layers (25 to 100 Gb/s)
  - Technology radiation hard at the level required by e^+e^- colliders.
  - Development of rad-hard links for HL-LHC and FCC-hh (2-6 × 10^{16} particles/cm^2)



- Active wireless repeater system demo & RFSOC integration, first tests of Power over Fibre
- Challenges: Design, fabrication and integration of RF ASICs, integration of PoF with detector electronics
- Community: France, Israel, Italy, South Korea, Sweden, US



WP 7.2: Intelligence on detector

Front-end **programmability, modularity and configurability** must be vastly enhanced in order to allow fewer, more versatile front-end electronics to be developed.

- Manage **complexity** by increasing **flexibility** and **re-usability**
- Radiation-tolerant **processors** and **programmable logic** elements with **common interfaces** and **protocols** will allow re-use of shared developments.

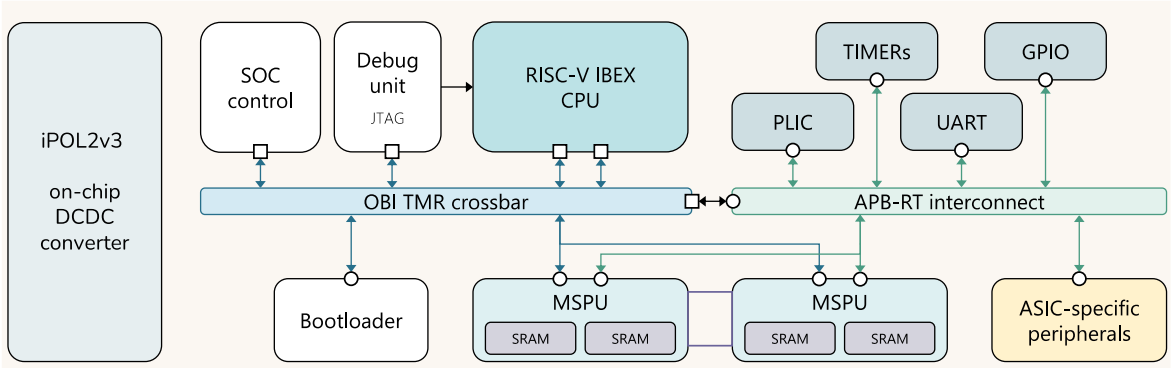
High level system modelling will enable optimizing the overall readout chain efficiency for a given power and bandwidth budget, while providing a robust specification and verification framework for the hardware design phase.

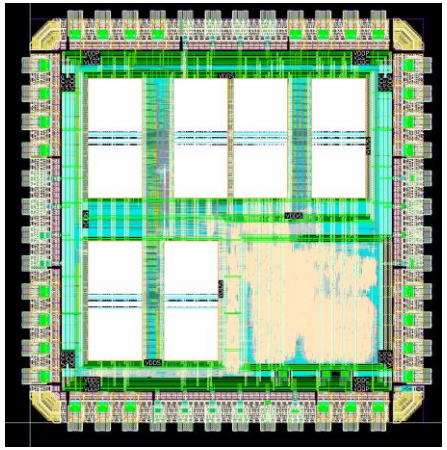
- **Reduce risks** and **optimize performance** exploiting **simulation** tools and computing power

- Conveners: *Davide Ceresa* [CERN], *Francesco Crescioli* [LPNHE]
- Projects
  a. Radiation Tolerant RISC-V SoC
  b. Virtual Electronic System Prototyping

Radiation Tolerant RISC-V SoC

- **Deliverable:**
  Radiation-hardened SoC based on the RISC-V ISA standard
- **Process flow:**
  - Define a roadmap for SoC architectures, radiation tolerant design methodology, SoC generator toolchain
  - Define target performance:
    Processing Speed, Power Consumption, Radiation Tolerance, Memory and Storage, Communication Interfaces, Scalability and Flexibility, Verification and Testing
  - Delivery of Rad-Tol SoC building block test chip





- Three chips scheduled for testing in 2025, demonstrating tangible progress
- The project spans multiple interconnected topics, making effective coordination across institutes a challenge
  - Try to define clear priorities and deliverables
- Community: Belgium, CERN, Estonia, Germany, UK

Virtual Electronic System Prototyping

- **Deliverable:**
  A framework for the simulation of the readout chain of a particle detector at a high level modelling the processes from the particle interaction with the detector to the digital readout of the collected data

- **Goals:**
  - Frameworks for *signal generation* in detector elements, *digitization and signal processing*, *data readout* architecture, operating as a complete toolchains.
  - Model different detector technologies at high level
  - Perform architectural studies before detailed implementation
  - Provide a reference for the ASICs verification
- Key to **involve beta users** to test and improve the simulation environment, becoming active collaborators in the project
- Community: CERN, France

WP 7.3: 4D and 5D techniques

Combine **high spatial resolution** (μm-level) and **high timing resolution** (10s ps level) in a single 4D tracking device.

Combine 4D with accurate measurements of the **energy deposited** in the sensor providing 5D-capability.

High performance ADCs and TDCs can be **power-hungry**

- Developing solutions to improve the noise-speed-resolution trade-offs in advanced technologies with **low supply voltage** and **high transistor density**.

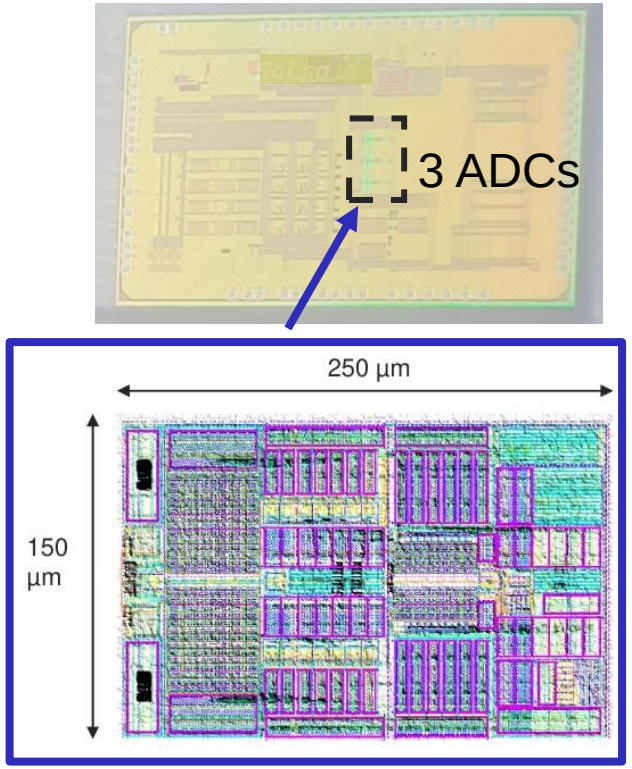
HEP application requires in addition unprecedented precision for the distribution of frequency and time references.

- Keeping **timing performance** at the **system level** a key challenge

- Conveners: *Sophie Baron* [CERN], *Marek Idzik* [Krakow]
- Projects
  a. High Performance ADCs and TDCs
  b. Characterizing and calibrating sources impacting time measurements
  c. Timing distribution techniques

High Performance ADCs and TDCs

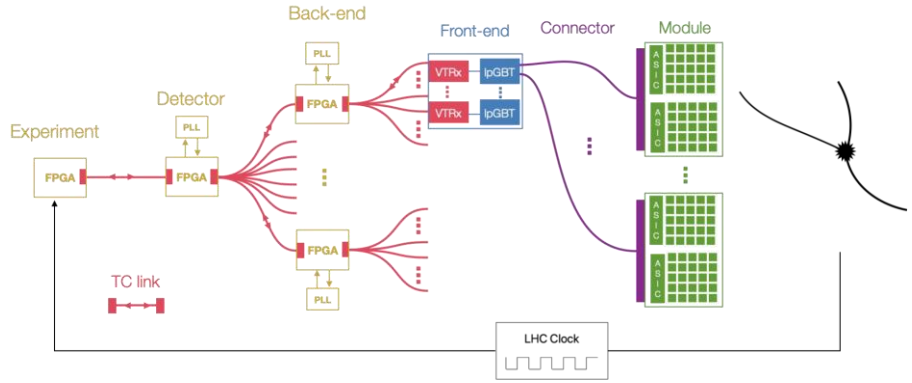
- **Deliverable:**
  Ultra-low power high performance TDC and ADC blocks for use in future particle physics experiments
- **Goals:**
  - High resolution (~ 10 ps) **TDC blocks**
  - Medium-high resolution (10-14 bits) and fast sampling (>40 MSps) **ADC blocks**
  - Ready to be deployed as key components of SoC readout ASICs for future particle detectors
  - Improve performance with respect to the state-of-the-art solutions obtained using the same CMOS technology and characterized by similar parameters

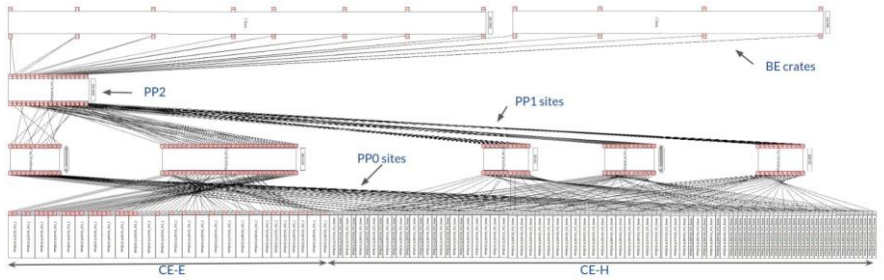


- Kick-off meeting September 2024
- A forum where participating institutes share knowledge and status of their projects, improving the collaborative effort
- Community: Austria, Belgium, France, Korea, Poland, Spain, US

Characterizing and calibrating sources impacting time measurements

- **Deliverable:**
  Data-driven calibration strategies for the time measurements in detectors requiring high precision timing
- **Planning:**
  - Design of a protocol of measurement.
  - Development of simulation tools in the different experiments.
  - Definition of common figures of merit.
  - Measurement of the properties in test facilities to compare with the predictions.
  - Design of calibration chain inside the experiments.

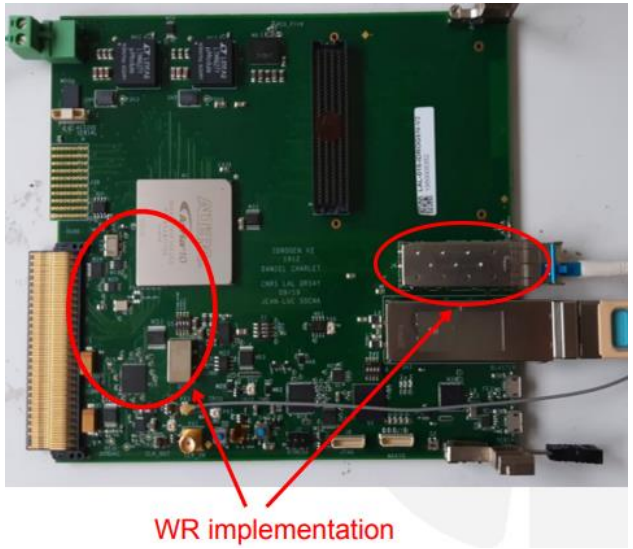




- Driven by the HL-LHC upgrades: ATLAS HGTD, CMS HGCAL and ETL
- First opportunity to have a common strategy between the different experiments for data-driven timing studies.
- Community: CERN, France, US

Timing distribution techniques

- **Deliverable:**
  Strategies to optimize and assess ultimate precision and determinism of timing distribution systems for future detectors
- **Goals:**
  - Bench-marking of the performance of COTS- or custom-based solutions to assess achievable timing precision:
    - random jitter, clock phase stability and determinism (at ps level)
  - Studies and implementation of FPGA-agnostic or ground-breaking solutions to mitigate the observed limitations



- The program includes the characterization of different FPGAs (PolarFire, Agilex, Versal)
- Combination with custom ASICs for building deterministic link (DCPS) and phase monitoring and phase shifting (PMPS)

- Community: CERN, France, Netherlands, Spain, UK, US

WP 7.4: Extreme environments

Interest in **cryogenic ASICs** is growing:

- Cryogenic detectors offer high **sensitivity** and **resolution** (for instance for future neutrino dark matter experiments) but are **challenging** for the design and operation of microelectronics.
- Foundries often lack **reliable characterization** and **modelling** of their ASIC technologies at low temperature

Future particle physics experiments, particularly at energy-frontier colliders, will face **extreme particle fluences**.

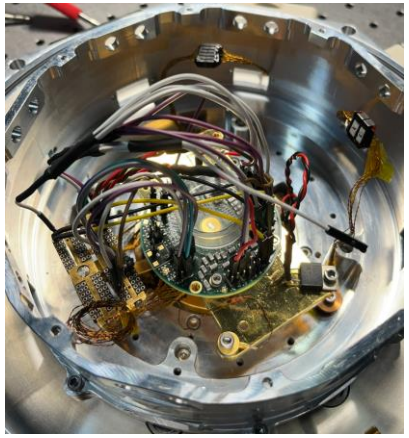
- ASICs, optoelectronics, powering devices, and on- or near-detector FPGAs must be designed and qualified for new level of radiation-hardness
- Radiation **qualification** of new technologies is **critical** and **complex**

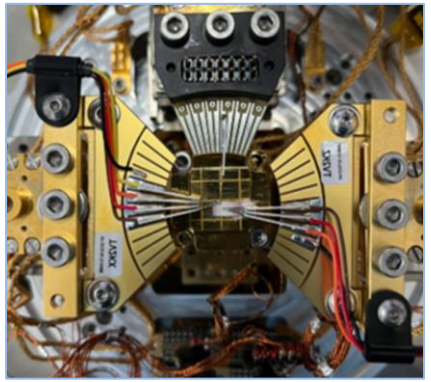
Low temperature operation requires novel techniques at the **interface** between **electronics** and **cooling** systems

- Conveners: *Giulio Borghello* [CERN], *Manuel Da Rocha Rolo* [INFN TO], *Oscar Augusto De Aguiar Francisco* [Manchester]
- Projects
  a. Modelling and development of cryogenics PDKs and IPs
  b. Radiation resistance of advanced CMOS nodes
  c. Cooling and cooling plates

Modelling and development of cryogenics PDKs and IPs

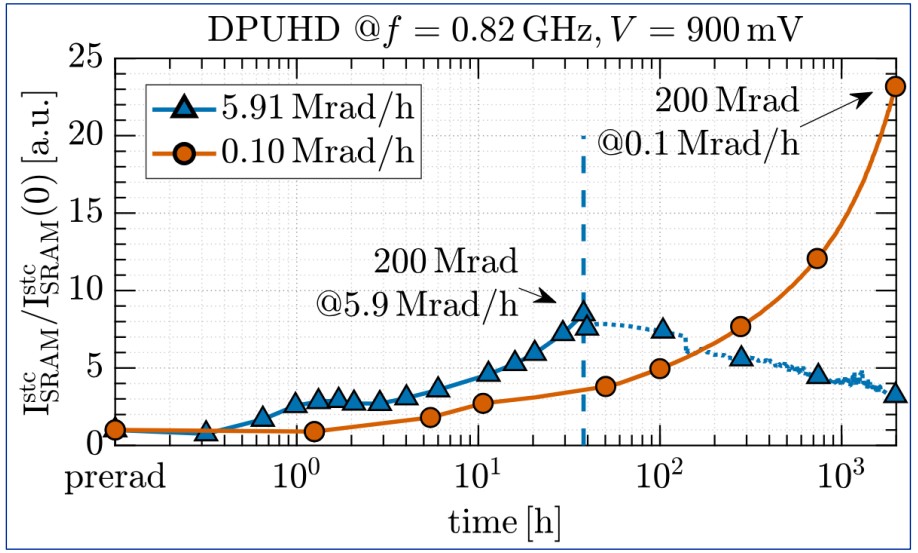
- **Deliverables:**
  1. Cryo-PDK for the TSMC 28nm technology node
  2. Prototype demonstrator chip with the cold-PDK
- **Goals:**
  - cold PDK for a deep sub-micron CMOS technology, with temperature corners at 165-87-77-4K
  - cold IP blocks demonstrated on board of a multi-channel mixed-mode demonstrator chip
- Applications:
  - photon detection in (LAr, LXe) noble liquid experiments
  - quantum computing interface and sensing
- Activity started on TSMC 65 nm, then moving to 28 nm
- Community: Germany, Italy





Radiation resistance of advanced CMOS nodes

- **Deliverable:**
  Report on developments and progress in the study of radiation effects in advanced CMOS technologies for HEP applications
- **Process flow:**
  - Realization and irradiation of front-end circuits:
  - Realization and irradiation of front-end matrices
  - Realization and irradiation of rad-hard memory elements

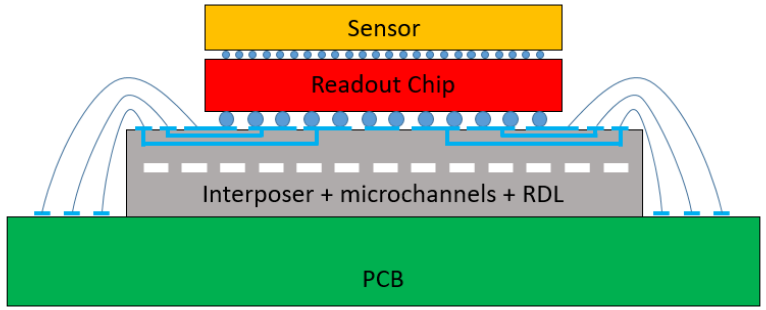


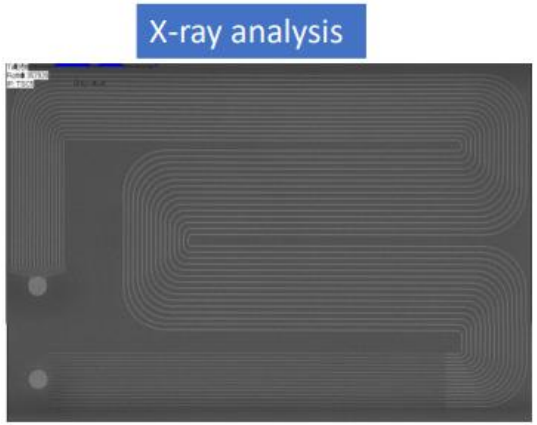
- Radiation studies being performed on 40 nm and 28 nm technology nodes
- Plan to perform the initial steps in the radiation characterization of finFETs
- TCAD modeling of radiation damage shows good fit to measurements

- Community: Austria, CERN, France, Italy

Cooling and cooling plates

- **Deliverable:**
  Next generation cooling plates for front-end electronics
- **Goals:**
  - Ceramics
    - Initial samples produced and tested, optimized design to be ma
  - 3D metal printing
    - New partner identified, first samples produced and under test
  - Si Microchannel
    - Thermo-compression with Au layer
    - Integration of microchannel in silicon interposer with signal and power traces
    - CMOS sensors with cooling channels





- Overlapping and synergies with the analogous DRD8 work packages will be carefully monitored

- Community: France, Spain, UK

WP 7.5: Back-end systems and COTS

Commercial off-the-shelf (COTS) **components** for **computing** (CPUs, GPGPUs, FPGAs, AI-accelerators) and **networking** are evolving rapidly

- driven by Data Center applications
- keeping the pace for future DAQ systems is both important and challenging

With more and more intelligence on detector, **direct connection** between the **front-end** and **COTS** component is an option to explore:

- different solutions explored for 100 GbE from front-end to back-end

- Conveners: *Conor Fitzpatrick* [Manchester], *Niko Neufeld* [CERN]
- Projects
  a. DAQOverflow
  b. From front-end to back-end with 100 GbE

DAQOverflow

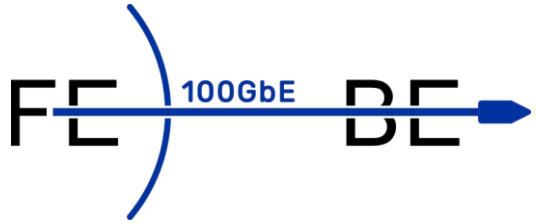
- **Deliverables:**
  1. Benchmarking of heterogeneous COTS architectures
  2. TDAQ tools and algorithms for near-detector/real-time ba processing
     - distributed via a common repository
     - kept up-to-date with evolving COTS technologies for cost and performance
- **Goals:**
  - Identify experiment-agnostic common TDAQ activities
  - Define generic benchmarks to allow easy comparison of cost/energy efficiency for various computing architectures for the purposes of backend/trigger processing.
  - Make generic algorithms / tools available for various architectures
- Several milestones already achieved: a set of specific test workflows, initial hardware platforms, common repository set-up

- Community: Spain, Switzerland, UK

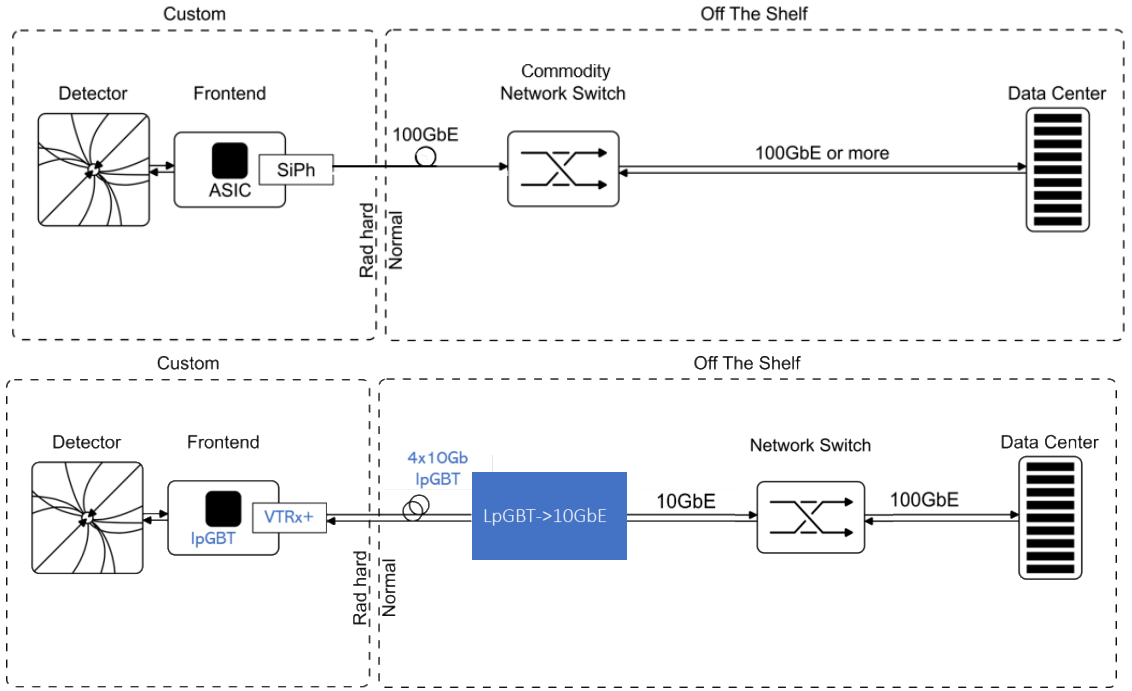
From front-end to back-end with 100 GbE

- **Deliverable:**

  Full 100Gb Ethernet-based solutions
  for Data Readout-links from Front-End to DAQ



- **Goal:**
  - ASIC implementing protocol IPs
    (may be common with RISC-V SoC project)
  - Demonstrator of the full system
- Three approaches identified:
  - **No back-end**: full demonstrator underway,
    in cooperation with 7.1
  - Intermediate approach with **translators/module board**: proof-of-concept done, dedicated hardware under development
  - **Smart switch**



- Community: CERN, France, Netherlands, Romania, UK, US

WP 7.6: Complex imaging ASICs and technologies

Increase the **integration** level of **sensor** and **front-end** electronics

CMOS Imaging Sensor (CIS) platforms are suitable technologies for **monolithic active pixel sensors**

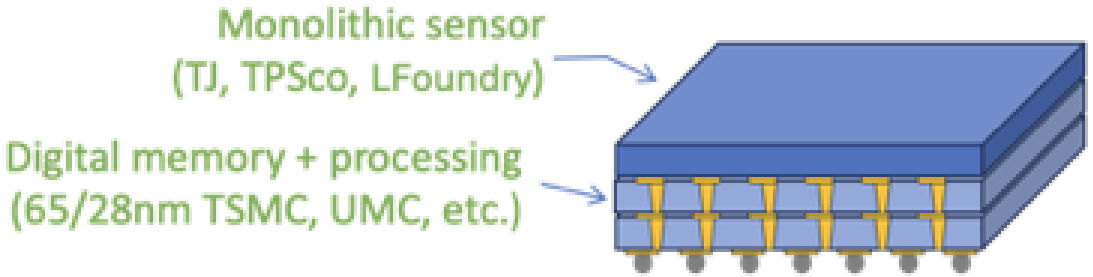
- Difficult to access CIS sensor technologies through standard MPWs

3D integration is powerful in expanding further the FE system capabilities,

- but challenging with **high initial barrier**

Organization of **common access** to these technologies:

- Reticle assembly
- Thinning and dicing
- IP development
- Design flow and PDK support
- Exploration of foundry for 3D integration



Strong connections with DRD3 activities

- Conveners: *Marlon Barbero* [CPPM], *Michele Caselle* [KIT], *Ian Sedgwick* [STFC RAL], *Walter Snoeys* [CERN]
- Projects
  a. Common access to selected imaging technologies
  b. Shared access to 3D integration

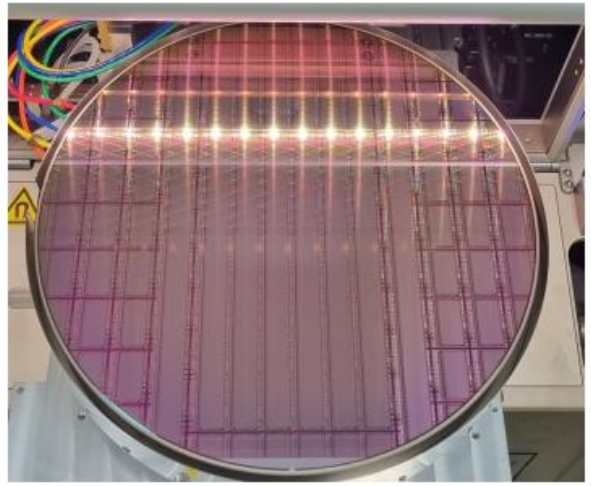
Common access to selected imaging technologies

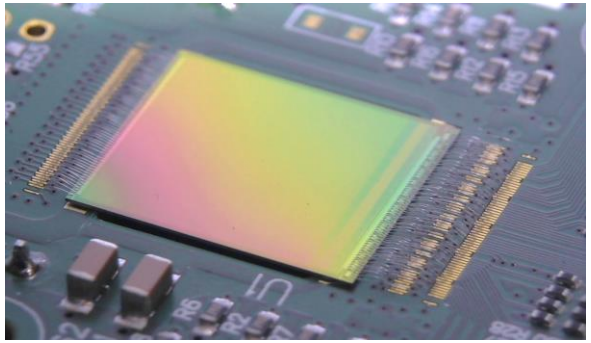
- **Deliverables**

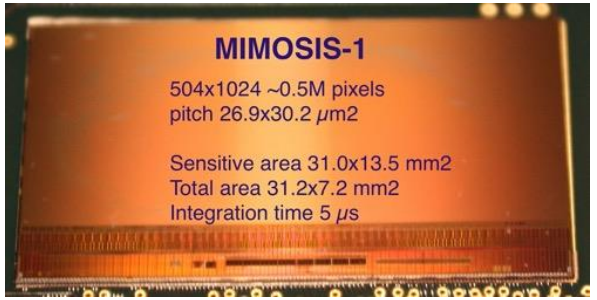
  Organization of common submission to selected processes: TPSCo 65 nm, TowerJazz 180 nm, LFoundry 110 nm

- **Achievements:**
  - Support for PDK, design flow, reticle assembly prior to submission, thinning and dicing
  - Several IPs available or under development
  - Single point interface to the foundry
  - Technologies adopted for construction projects in HEP
  - Recently: new metal stack for low IR drop also for stitched sensors in TPSCo 65nm, preparation of quartpic2 run in TJ 180 nm, functional CMOS LGAD prototypes in LF 110 nm IS

- Putting in place framework, both administratively and technically, concentrate resources to allow institutes to access the technologies
- Community: managing access to TPSCo (CERN), TowerJazz (CERN+IPHC), LFoundry (INFN), but a much wider user community







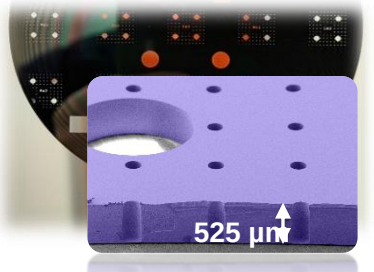
Shared access to 3D integration

- **Deliverables:**

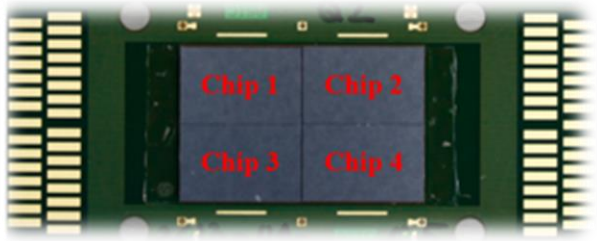
  Common access to 2.5 and 3D integration

- **Achievements:**
  - Focusing primarily on in-house infrastructure and service
  - several in-house processes qualified or under development

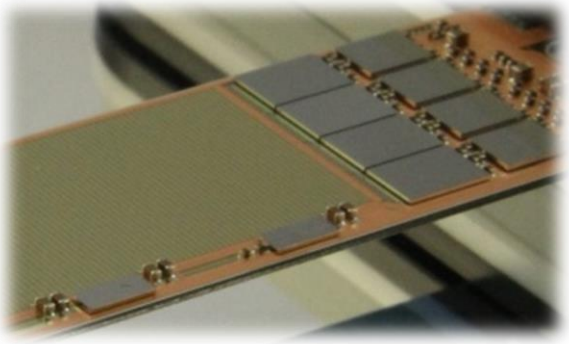
- Challenge: provide a distributed international laboratory operating as a hub-service for the community
- Strategy to address the challenge: use a demonstrator project (Pilot Heterogeneous Integration project) to validate and implement a distributed production flow



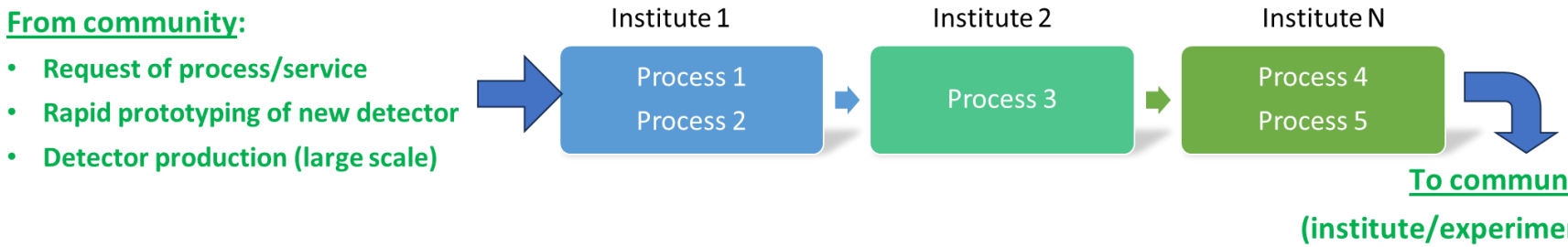
TSVs @ KIT



Multi-bonding @ USN



ASM *(All-Silicon Module)* @ MPG-HLL



WP 7.7: Tools and Technologies

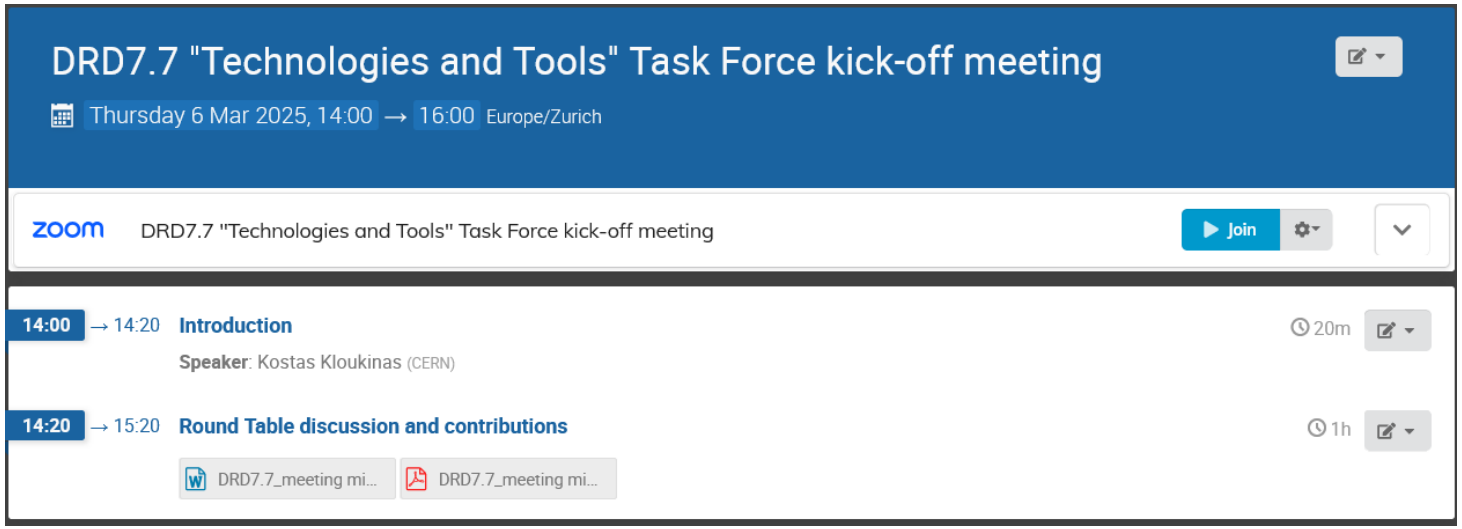
Effective support of technologies and tools to the HEP community is both essential and demanding

Models adopted in the past might not allow to keep the pace

A task force has been established to discuss new cooperative models

Initial mandate: *To propose an implementation solution for a hub-based structure for ASICs developments.*

Kick-off meeting on March 6, planning regular monthly meetings



- Conveners: *Kostas Kloukinas* [CERN], *Xavi Llopart Cudie* [CERN], *Mark Willoughby* [STFC RAL]

Call for contributions

- The **MoU annexes** related to the **existing projects** are under **finalization**
  - still technically possible (but short in time) to **join existing projects** before the projects are circulated to the Collaboration and the Funding Agencies
  - **R&D projects** will anyhow continue to evolve and will be **regularly updated** with new contributions

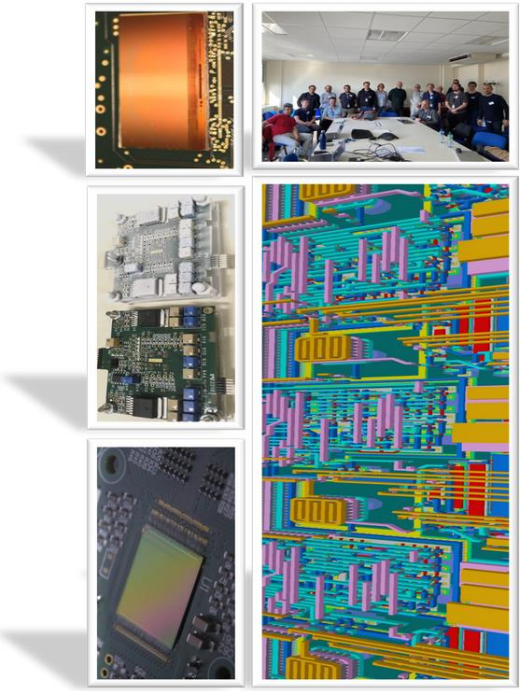
- **Promoting new projects** is also encouraged
  - Expect a **yearly review cycle** for new projects and contributors
  - A very interesting project in WP7.2 concerning ASICs **embedding FPGA** need to reach a critical mass to collect the resources
  - Some ECFA strategic topics not covered by projects yet:
    - *Intelligent power management*
    - *Reliability, fault tolerance, detector control*
    - *Novel on-chip architectures for 4D detectors*

If interested, please contact the WP conveners

Thanks for your attention

Thanks to the organizers for giving the DRD7 Collaboration the opportunity to advertise its activities

DRD7 COLLABORATION

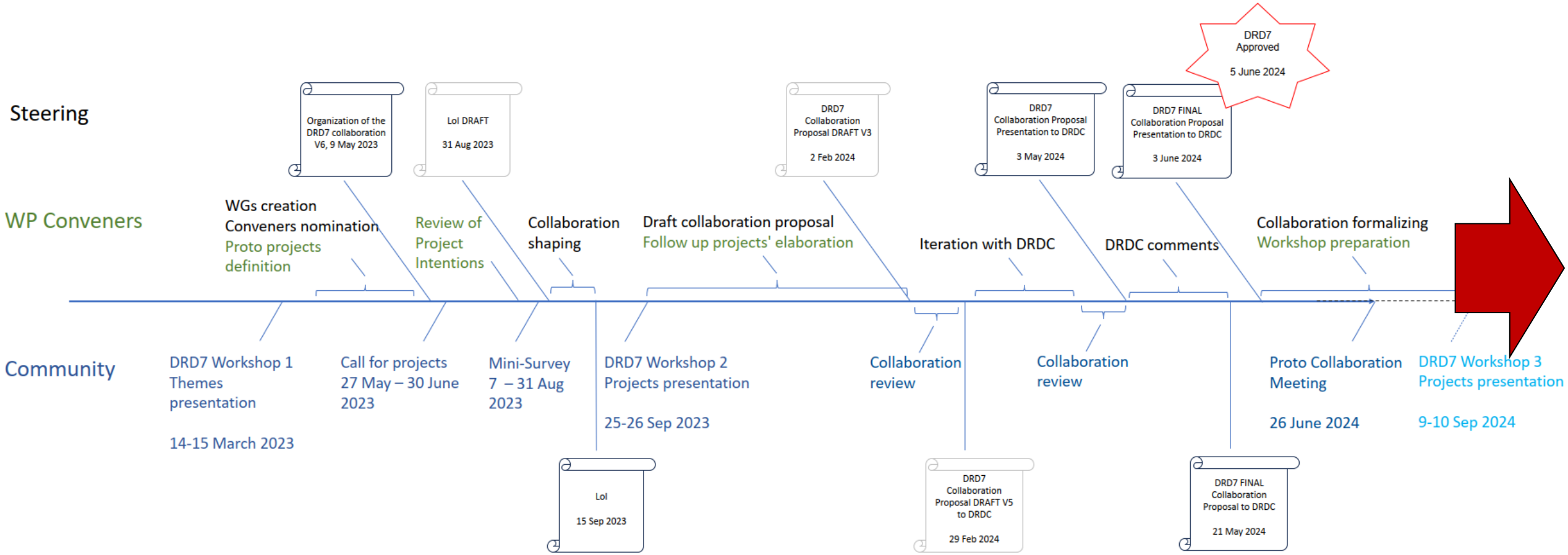


- If you would like to know more:
  - Check the DRD7 website: **https://drd7.web.cern.ch/**
  - Subscribe to the *observers* e-groups (**ECFA-DRD7*Observers@cern.ch**)
  - CDS and Indico material being populated

BACKUP

INFN MILANO
UNIVERSITÀ DEGLI STUDI DI MILANO
DIPARTIMENTO DI FISICA

DRD7 History and Timeline



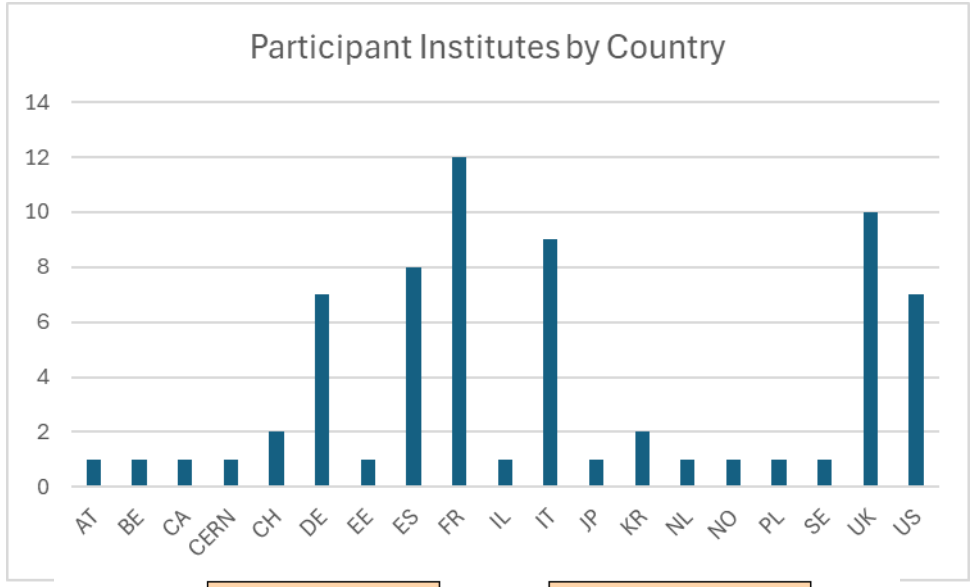
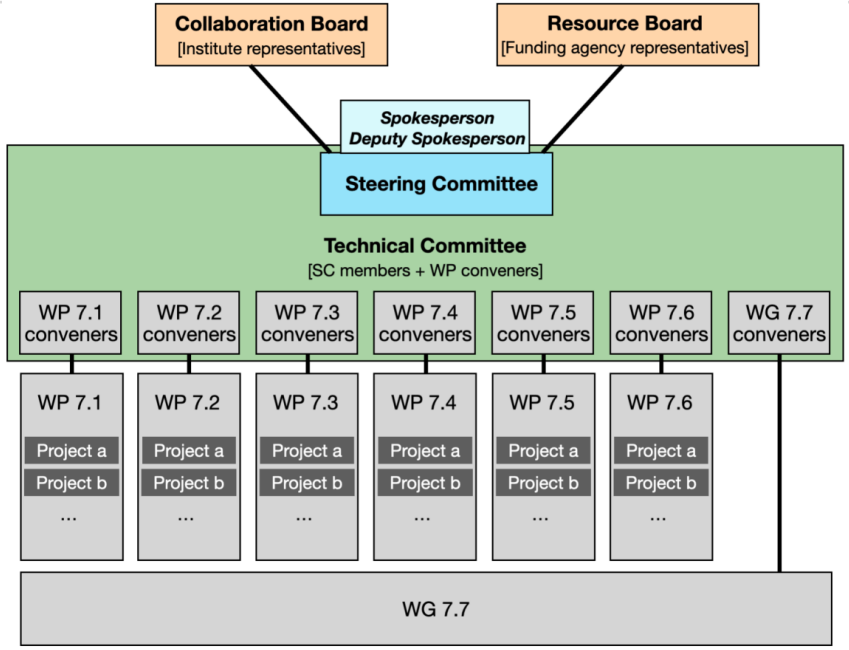
- DRD7 Collaboration Proposal was approved by DRDC in June 2024
- Since then, the formal collaboration forming process has progressed smoothly
- Today a summary of the activity in the last months and next steps to be performed

DRD7 Collaboration

Collaboration Proposal approved by DRDC on June 5th 2024

- 67 **Institutes** from 19 **countries**
- 6 **Work Packages**, fitting with the ECFA Detector R&D Roadmap objectives
  - 15 **Projects** (deliverables)
- 1 Transversal **Working Group** on *Tools and Technologies*

Since then, formal collaboration forming process has progressed:

- Election of management
- Approval of MoU annexes containing collaboration rules
- Annexes with Work Packages implementation under review of the Steering Committee

Elected management:
Collaboration Board Chair: Attilio Andreazza (Milano), Cristina Fernàndez Bedoya (Deputy, CIEMAT)
Steering Committee: Jerome Baudot (IPHC-Strasbourg), Marcus French (STFC RAL), David Gascón Fora (ICCUB), Katja Klein (RWTH Aachen), Ruud Kluit (NIKHEF), Angelo Rivetti (Uni and INFN Torino), Frank Simon (KIT), Francois Vasey (CERN)