



Design and development of a Data Acquisition System for a Cosmic Muon Veto Detector

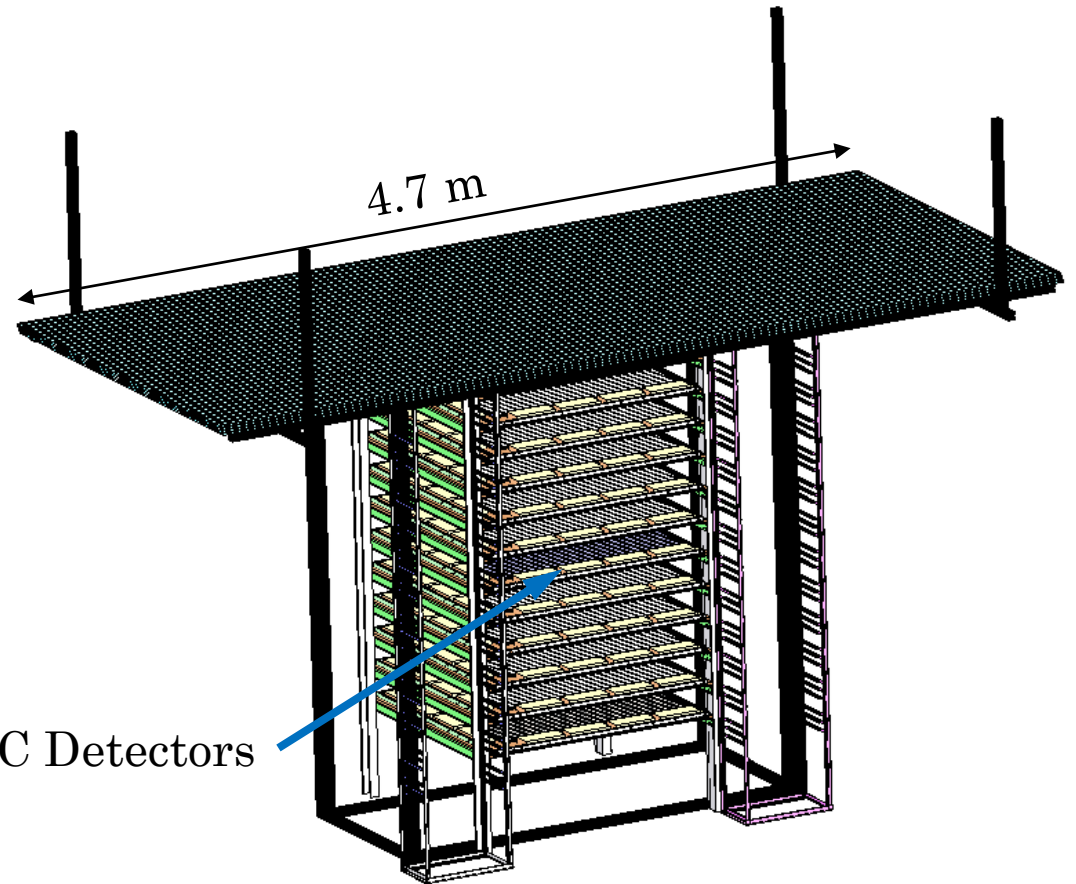
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C, Gobinda Majumder, Ravindra Shinde, Suresh Upadhya

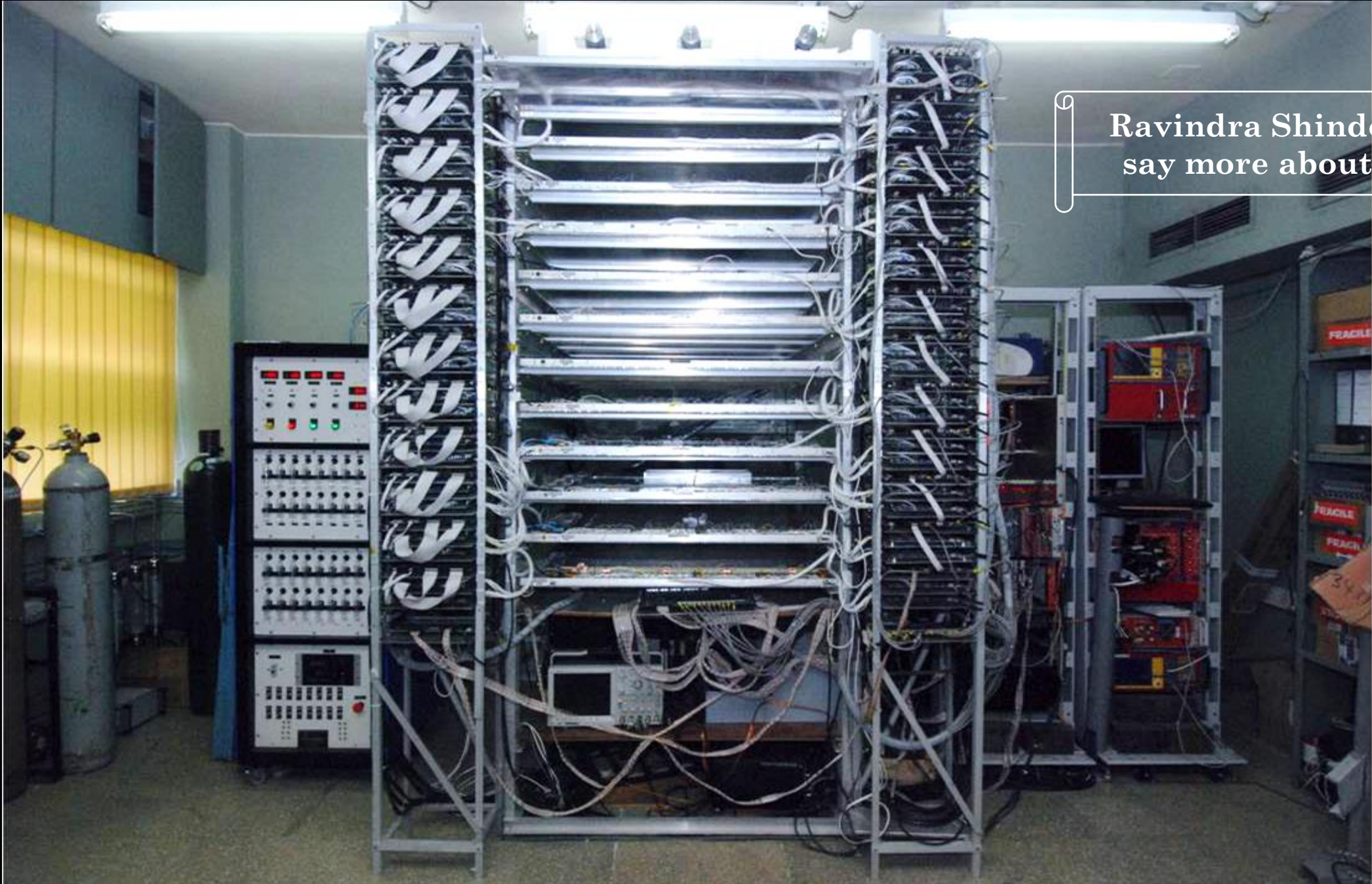
TIFR, Mumbai

TIPP 2026, February 2-6, 2026, at TIFR, Mumbai

Motivation

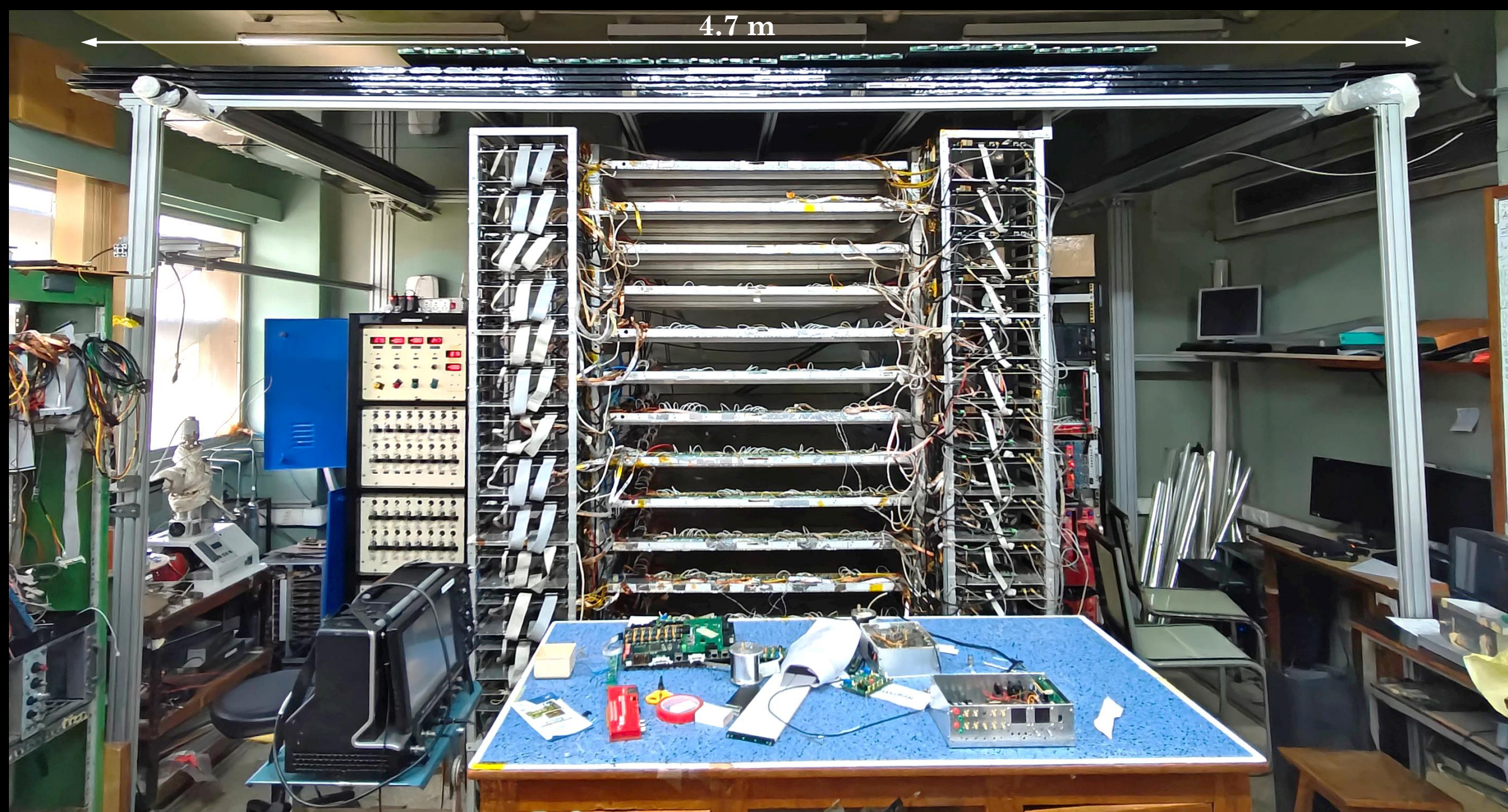
- To study the feasibility of a shallow-depth neutrino detector, a Cosmic Muon Veto Detector (CMVD) is being built around the RPC detector stack at TIFR, Mumbai.
- The CMVD will use extruded plastic scintillators for muon detection and wavelength-shifting fibres coupled with silicon photomultipliers (SiPMs) for signal readout.
- 4 Layers of plastic scintillators in one direction, and 1 layer in orthogonal direction
- Total 200 scintillator strips will be used amounting to 800 SiPMs to be read out





Ravindra Shinde will say more about this

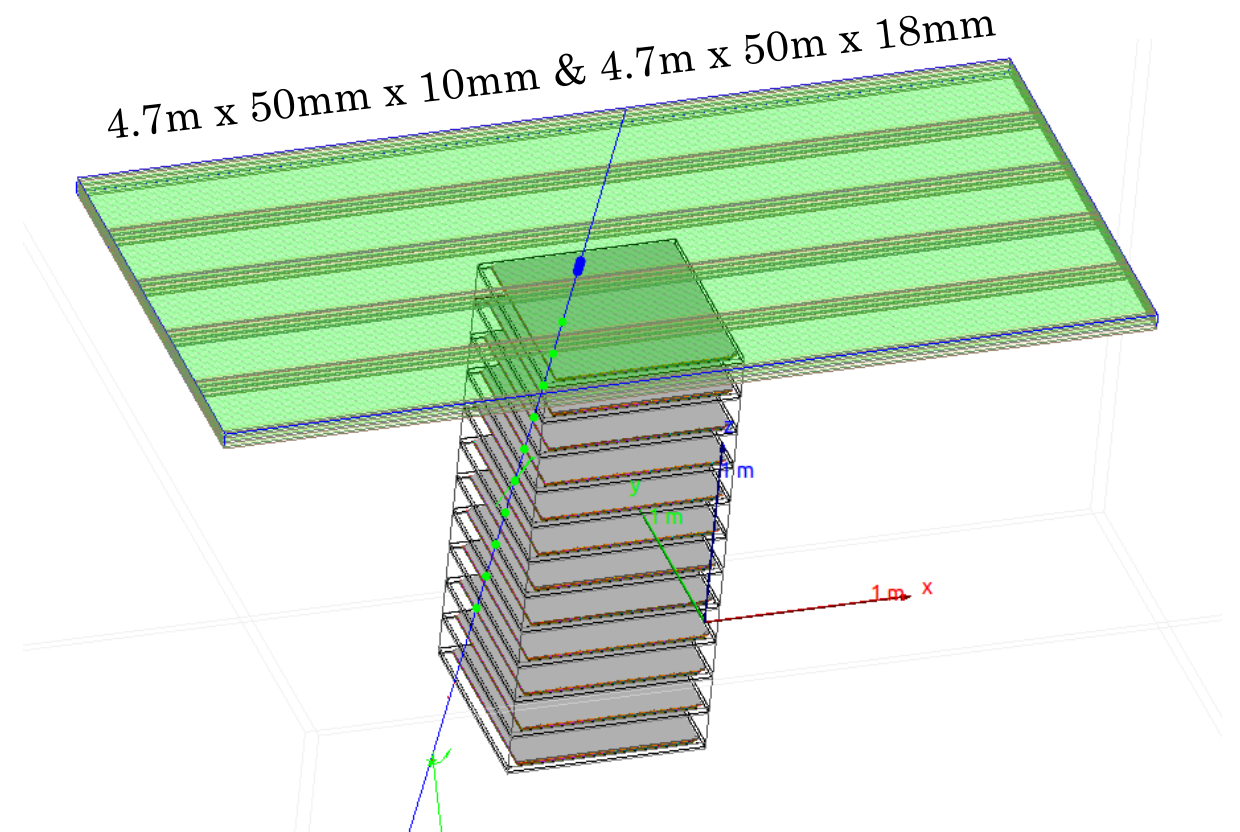
The 12-Layered C217 RPC Stack @ TIFR



The C217 Stack with Arrangement for Keeping the CMVD Plastic Scintillators

Concept of Operation

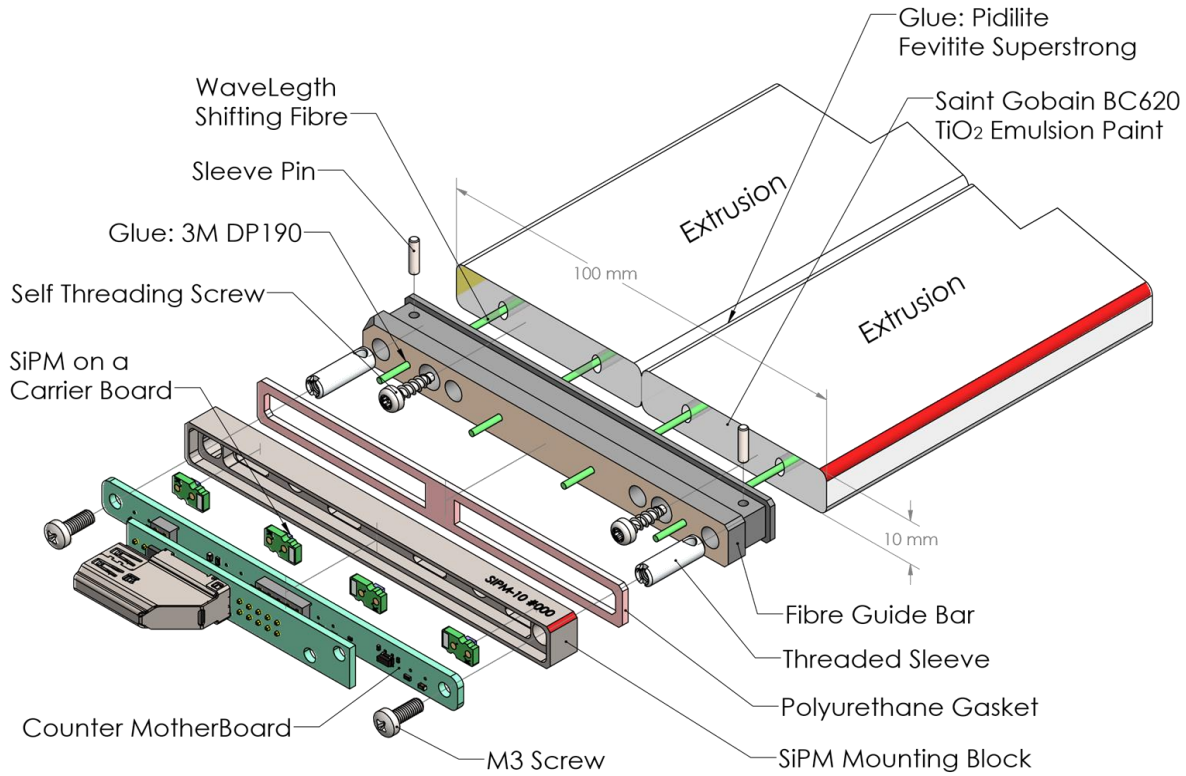
- We want to determine the efficiency of the veto detector
- We do this by recording the status of the veto detector during an RPC trigger
- For every data point, the muon trajectory reconstructed from the RPC data is extrapolated into the veto detector
- For all the events, we check if the veto detector has a muon signature at the extrapolated location to evaluate the veto detector's efficiency



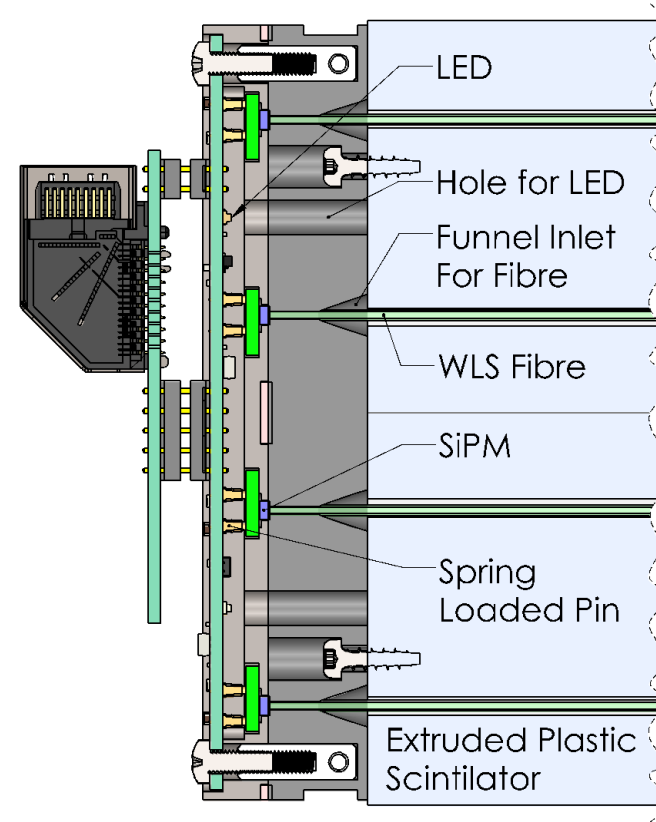
Veto Detector Requirements

- Design Requirements
 - Efficiency 99.99%, false trigger rate $< 10^{-5}$
 - Charge and relative arrival time for SiPM signal on RPC trigger
 - Charge: Dynamic range of 80 pC, least count of 20 fC
 - In-situ detector calibration – Noise data and LED source
- Supporting results from test studies
 - Single PE avalanche charge: 0.28 pC @ 2.5 V_{ov}
 - Average PE yield for a cosmic muon trajectory in 10 mm scintillators: 16

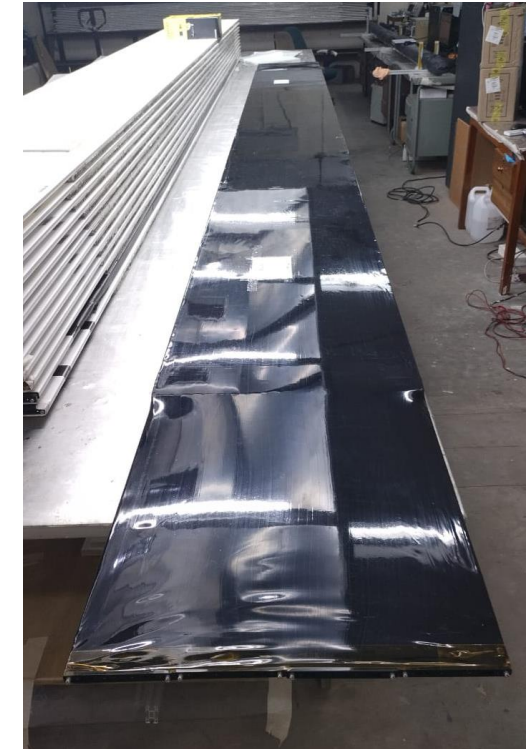
Scintillator Assembly (Di-counter)



Blown up view of a Di-Counter Assembly



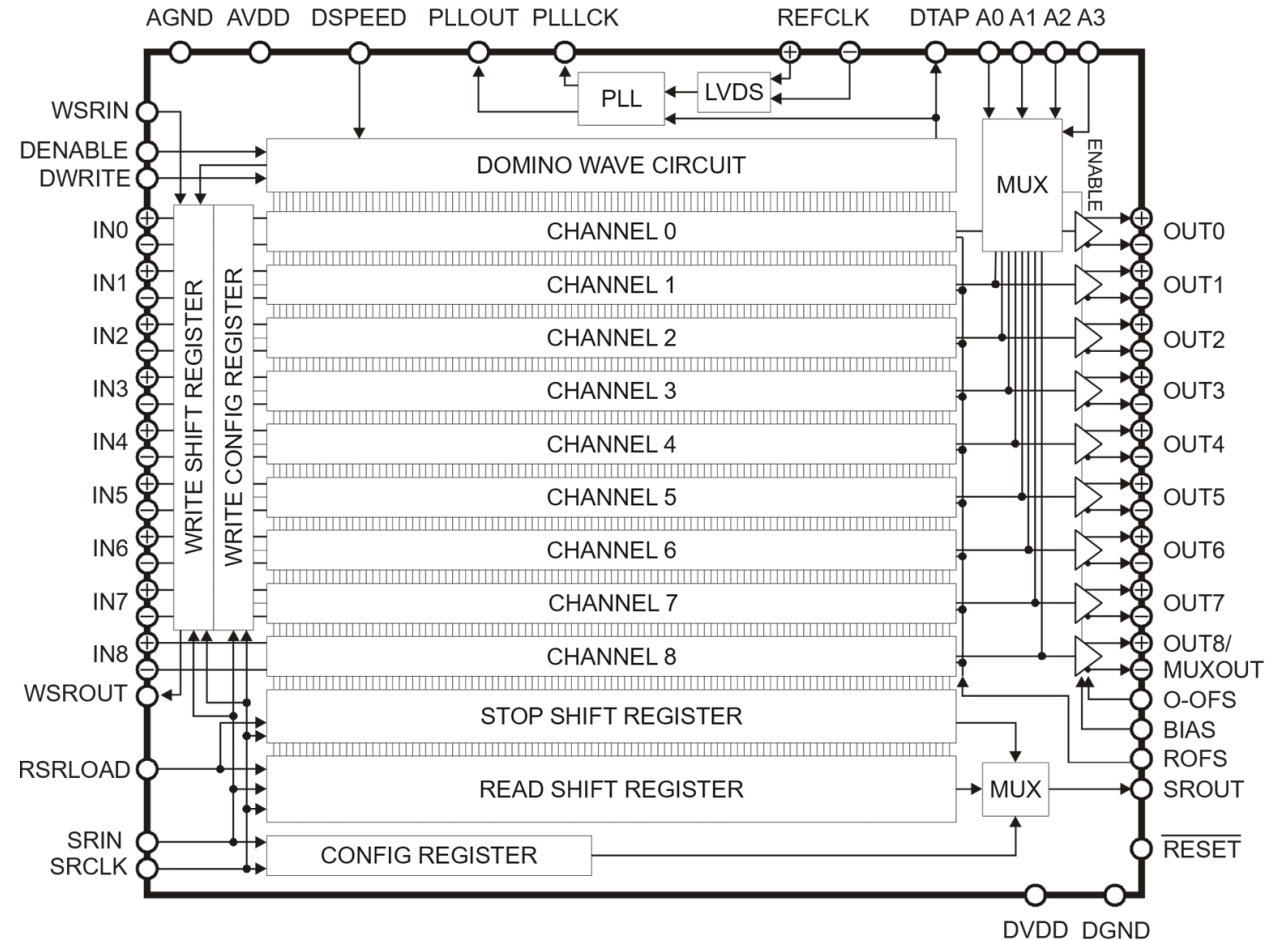
Cross sectional view of a Di-Counter Assembly



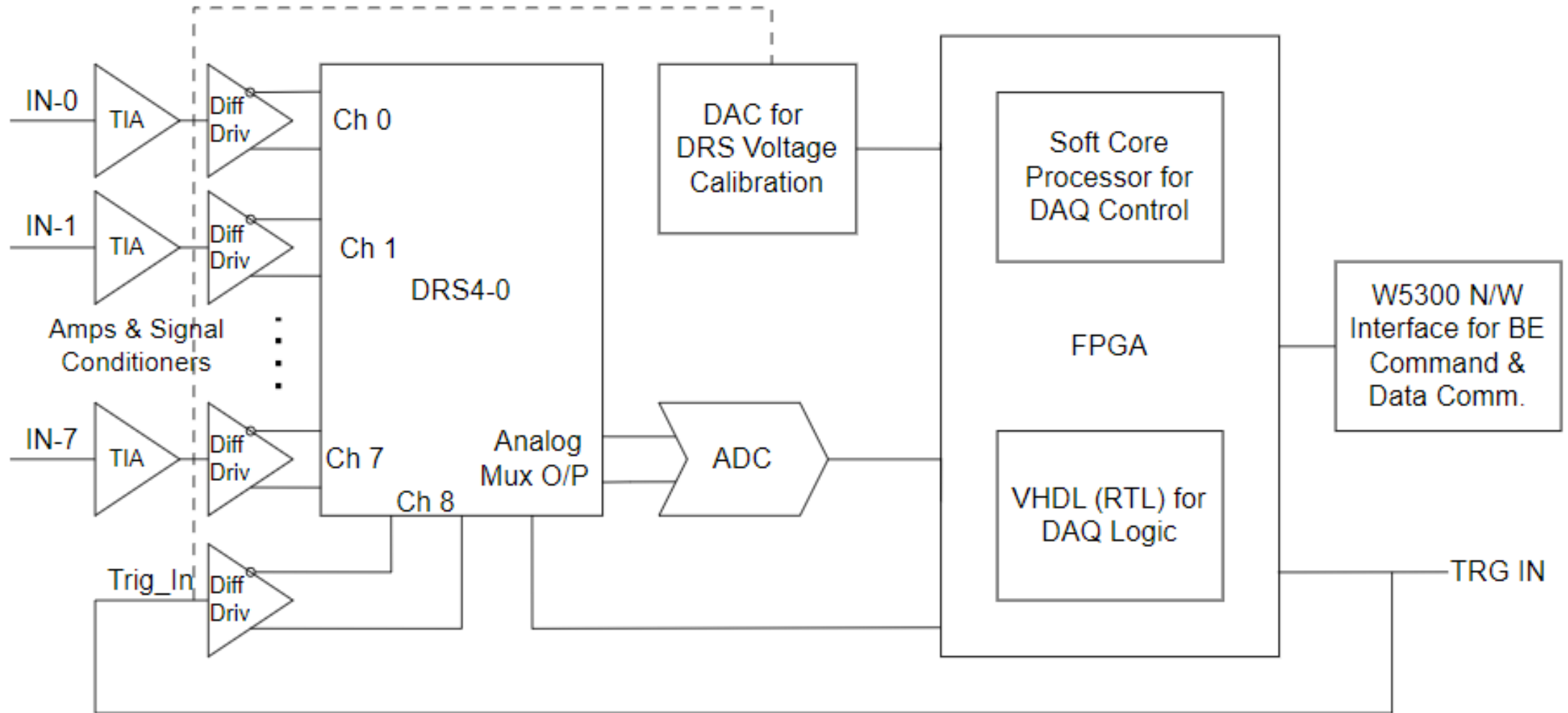
Detector Tile consisting of 4 Di-counters of length 4.7 m

DRS4 Waveform Sampler

- DRS4 – developed by PSI (Paul Scherrer Institut)
- Domino Ring Sampler is a switched capacitor array.
- Samples 9 input channels at speed of 0.7 to 5 GSPS
- Memory depth of 1024 cells per channel
- When trigger occurs sampling is stopped and readout process is started
- Capacitors are read out with much slower rates - typically around 33 MHz

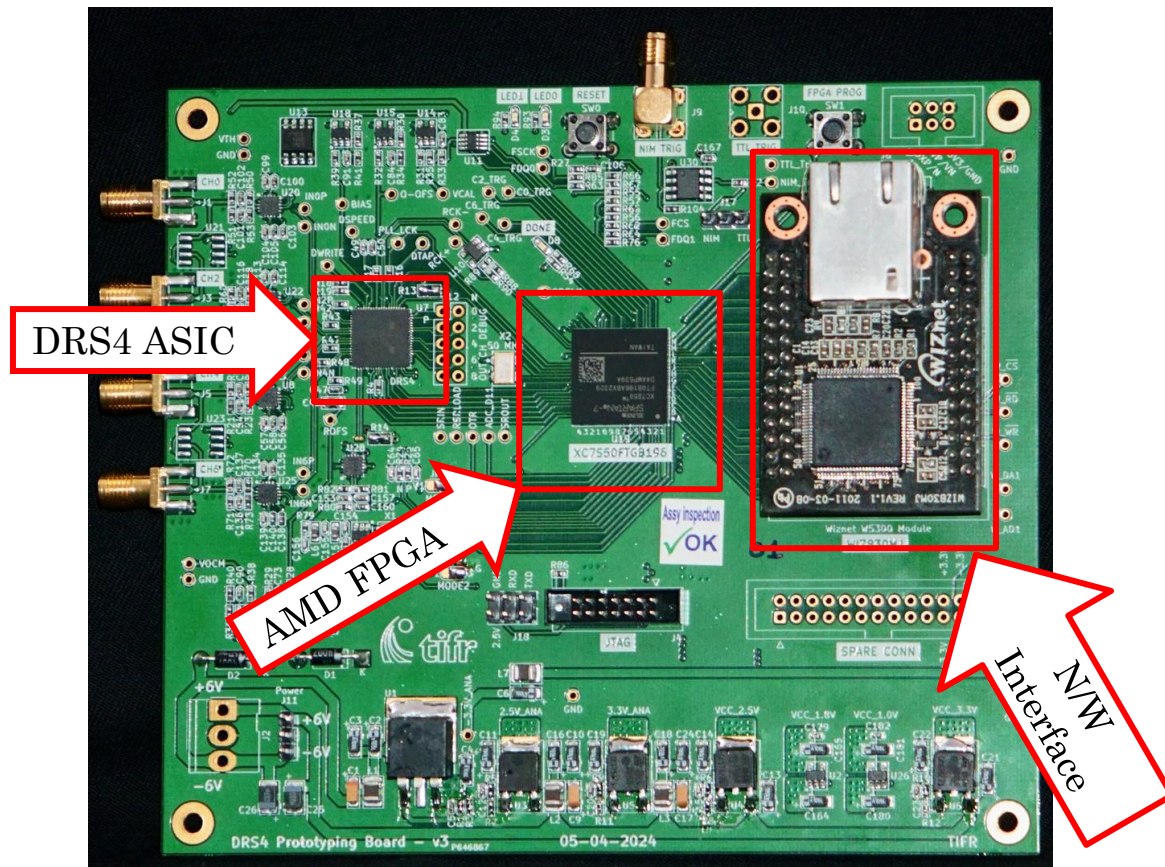


Prototyping with the DRS4 and AMD Spartan-7 FPGA



Prototyping

Single DRS Prototype Board



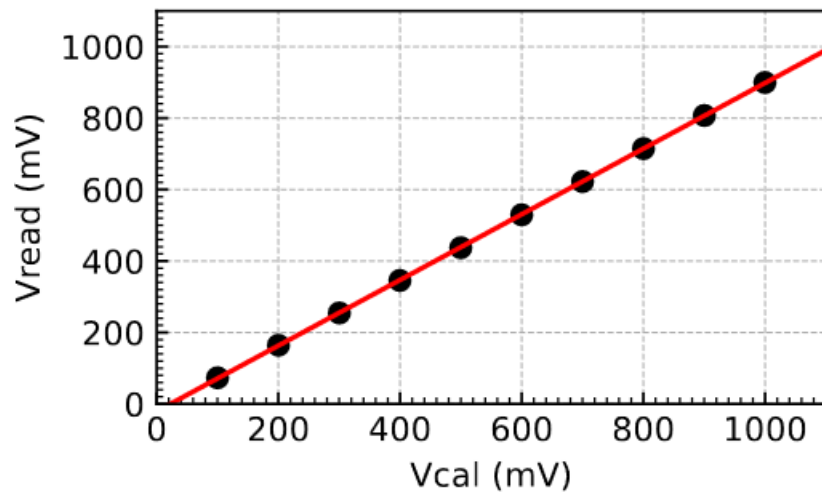
Test Setup



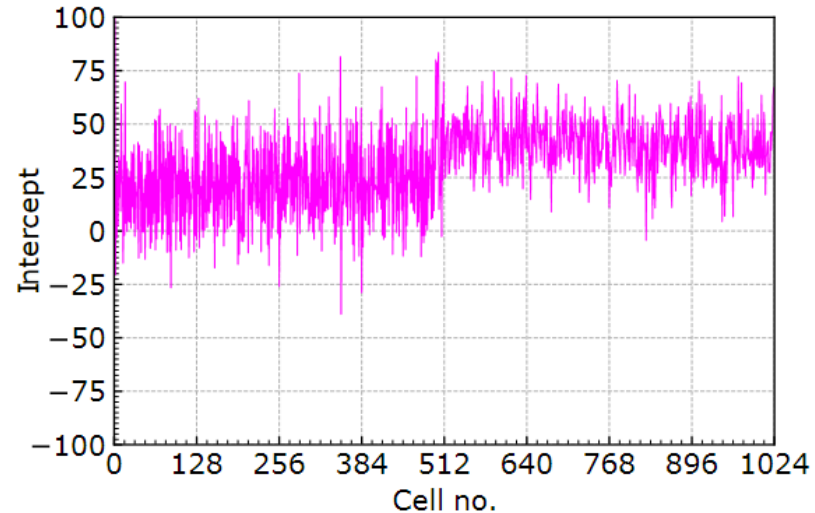
Processes Involved in DRS4

- Measure the DRS4 offsets for all the 1024 cells of each channel
 - DAC applies 0 to 1V DC to the inputs of the DRS4 and the DAQ records the value of each cell for every channel
 - Data is analyze to get 1024 offset values or every channel
- Full cell readout of a single channel on an external interrupt
- Region of Interest (RoI) readout of a single channel on an external interrupt

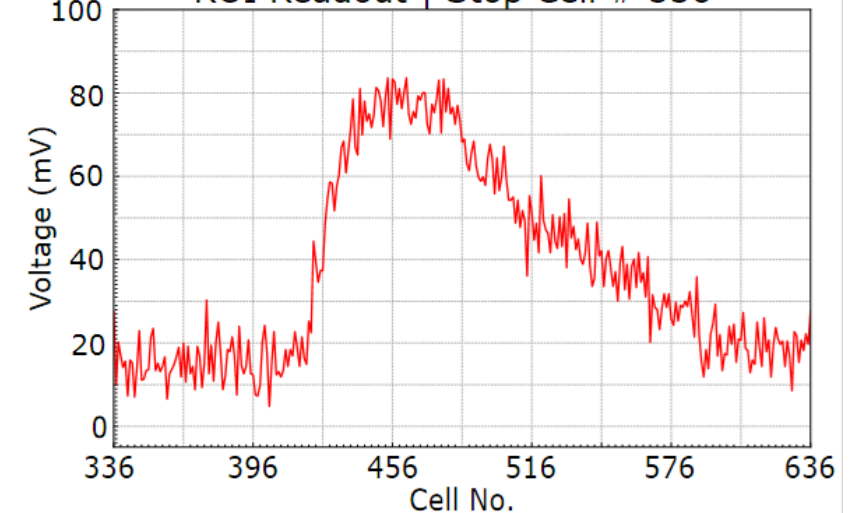
Channel 3 Cell 2



Cell wise Offsets



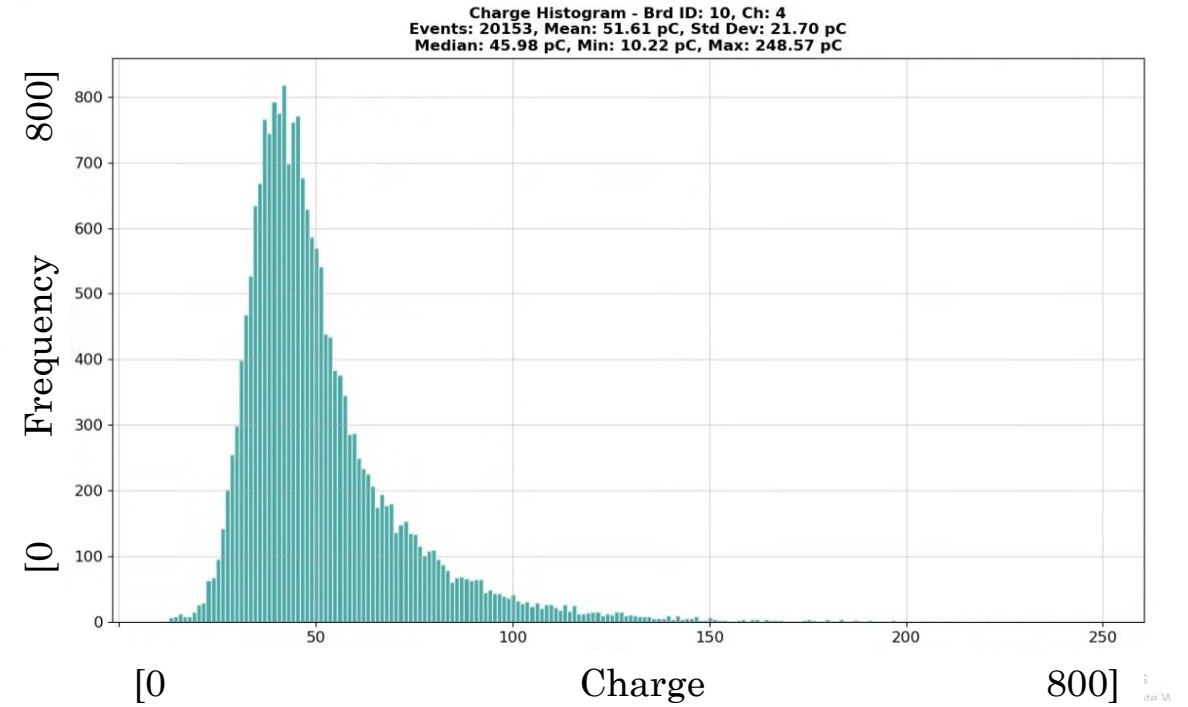
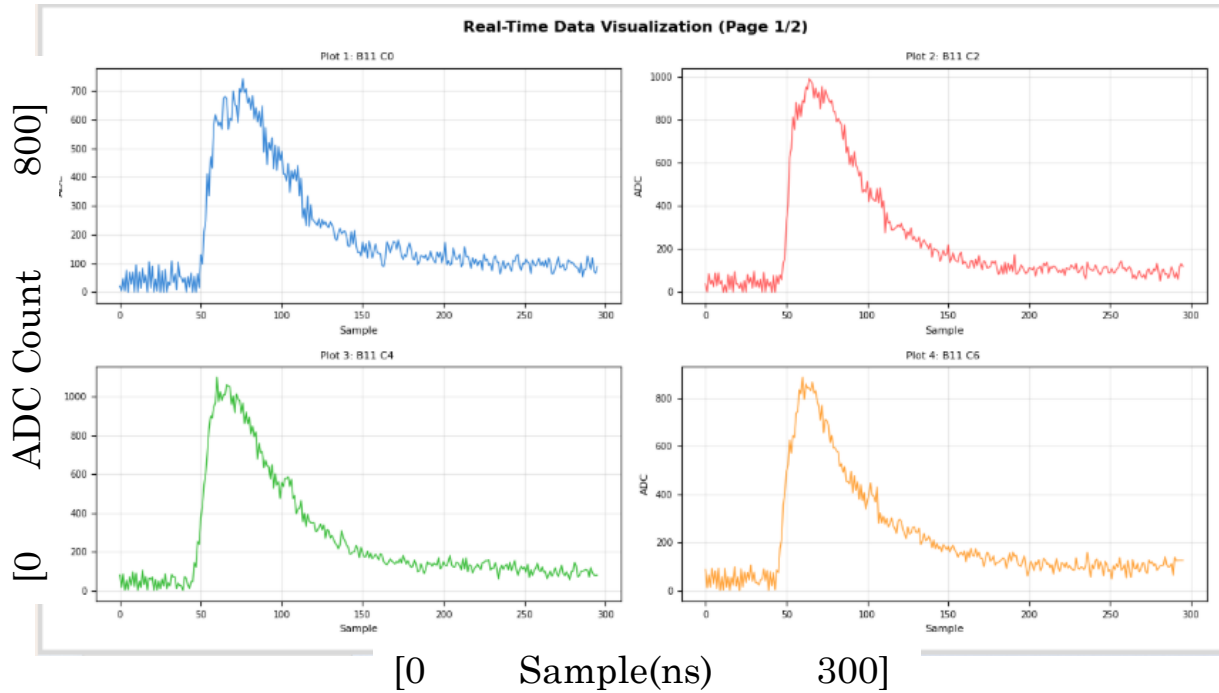
ROI Readout | Stop Cell # 336



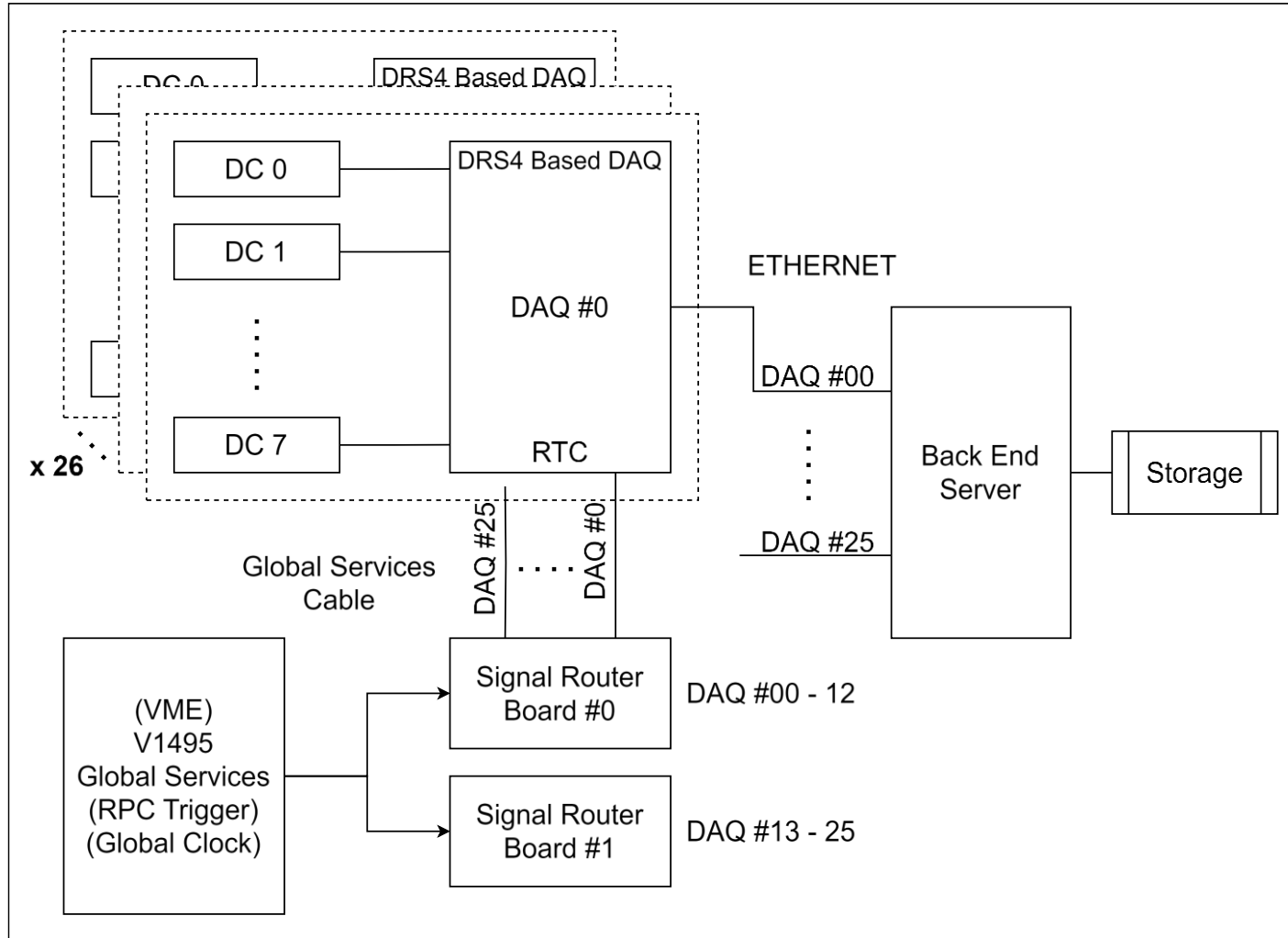
Test Results

Cosmic Muon Signals from Plastic Scintillators

Charge Distribution of the Muon signals



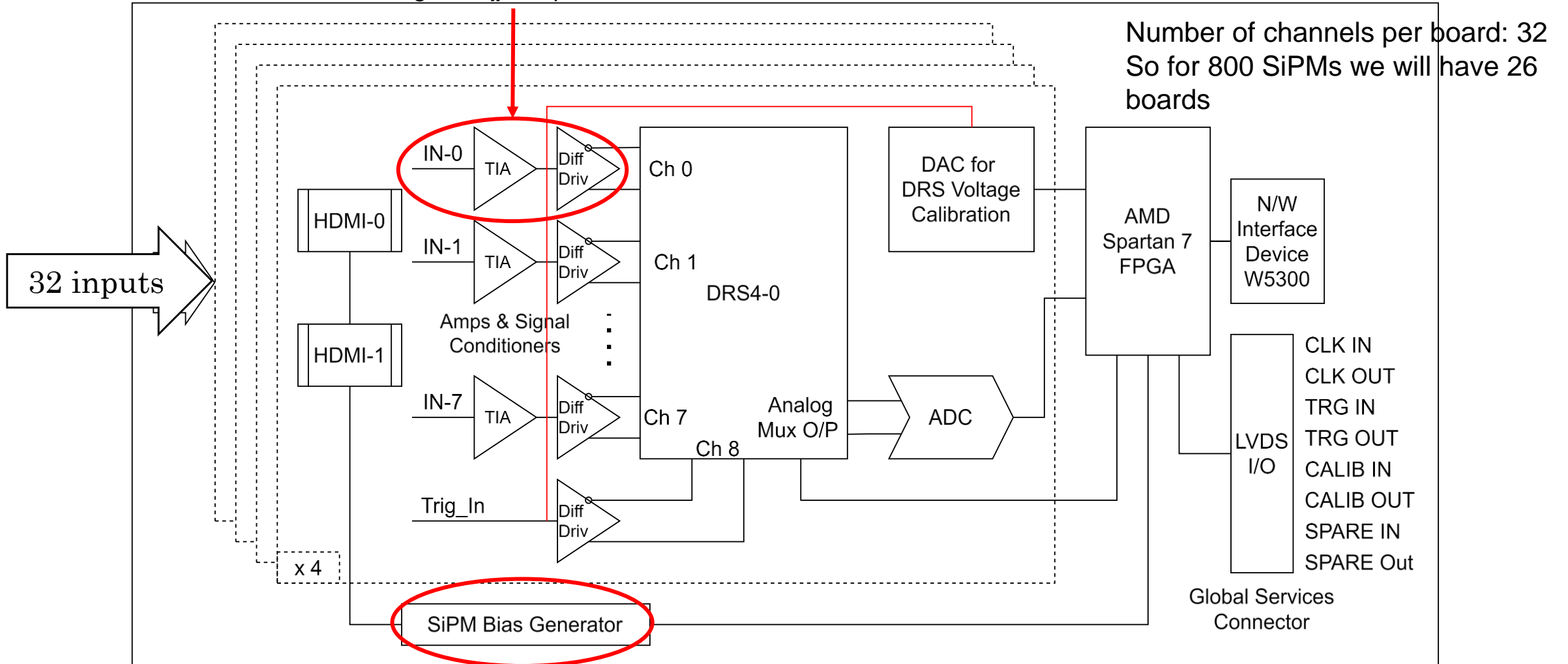
CMVD Data Acquisition Scheme



- 26 DAQ Boards for 800 SiPMs
- Data throughput per board: 300 kB/s
- For 26 boards the Data generated is: 7.6 MB/s

Moving to the Final DAQ Board Design

Custom design. Prajjalak presents this next



Custom development. Prajjalak presents this as well next

Further Functionalities and Scaling up

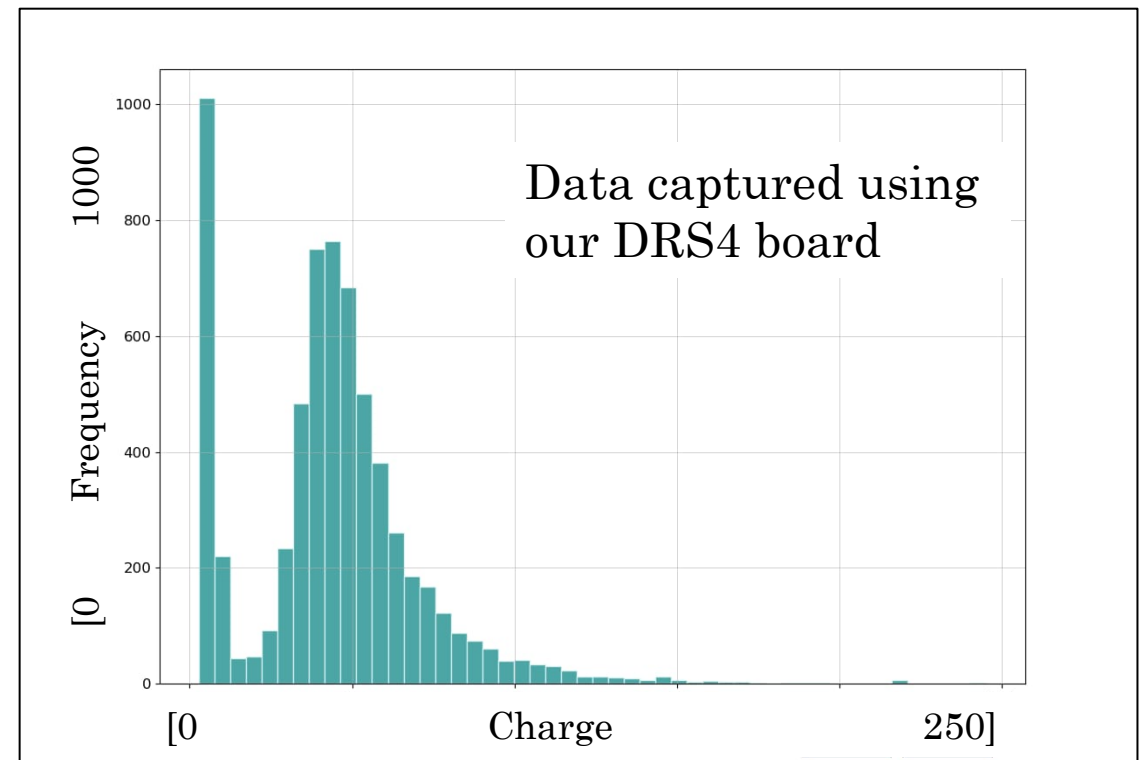
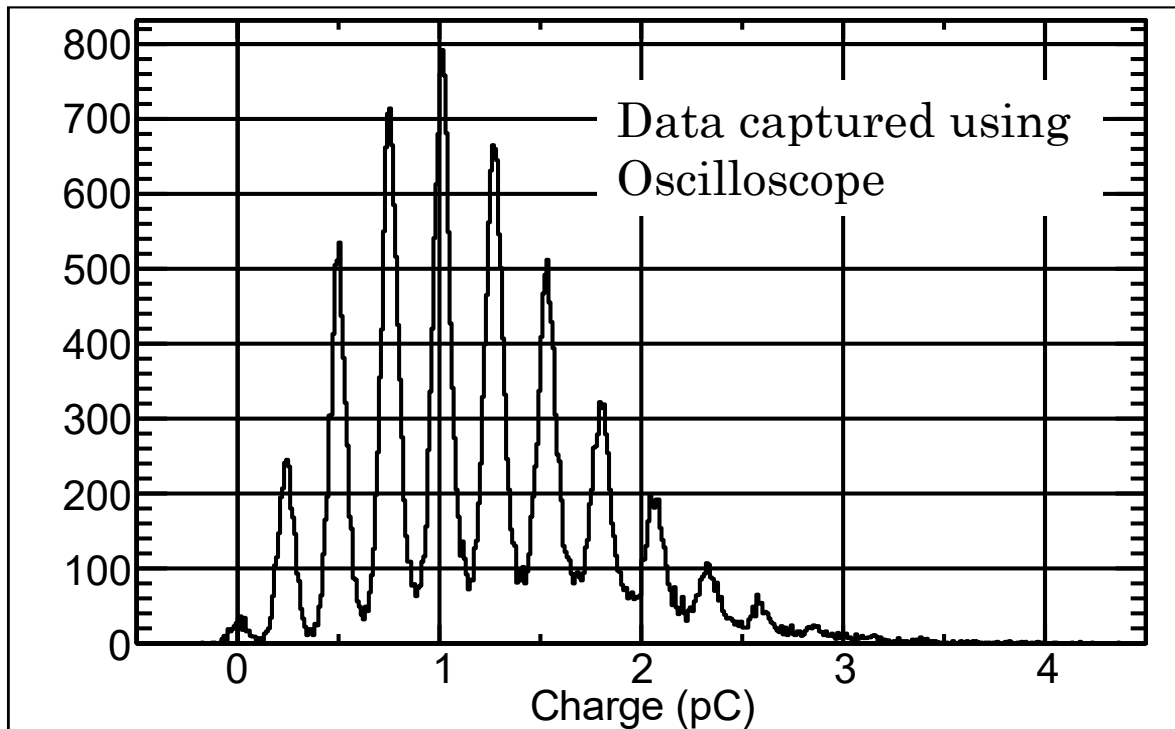
- Online zero suppression
 - Suppression of SiPM noise pulses below a threshold of 2.5 Photo-Electrons to reduce data size
- Online charge measurement in the FPGA (Optional)
 - The charge value of a voltage pulse waveform in a discrete data system is given by the following equation:

$$q = \frac{1}{R} \sum_{n=0}^N V(n)\Delta t$$

- Where, Δt is the sampling period, and N is the number of samples, R is gain of the Transimpedance Amplifier
- An accumulator in an FPGA can do this on the fly and reduce the data size by a factor of 100

Status and Summary

- Prototyping completed for a single DRS4 DAQ board AMD Spartan 7 FPGA
- Meanwhile we are adding more functionality to the firmware of the prototype boards
- Work has already started on the 32 channels board which will use 4 DRS4 ICs and one FPGA
- Need to address noise problem, which blurs out the single PE peaks as seen below



Thank You

Any Questions please??

You are welcome to visit our lab (C217) to see the setup