FPGA-based Emulator Platform Targeting ATLAS Phase-2 ITk DAQ System Development

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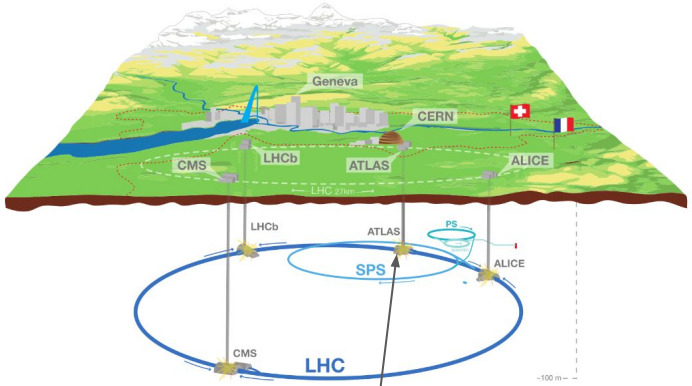
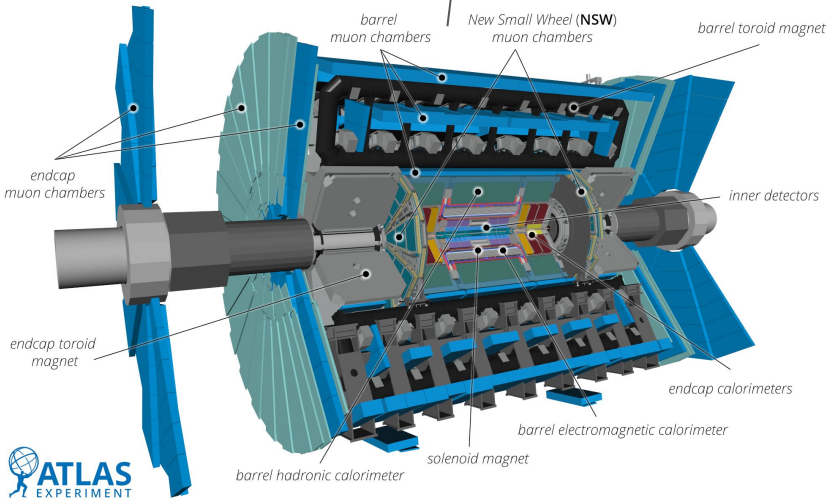
ATLAS ITk

LHC and ATLAS

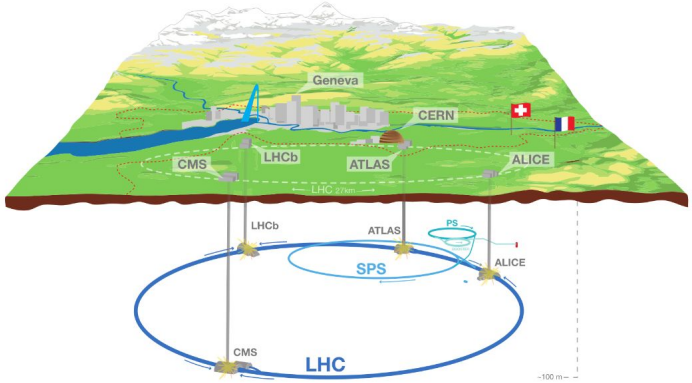




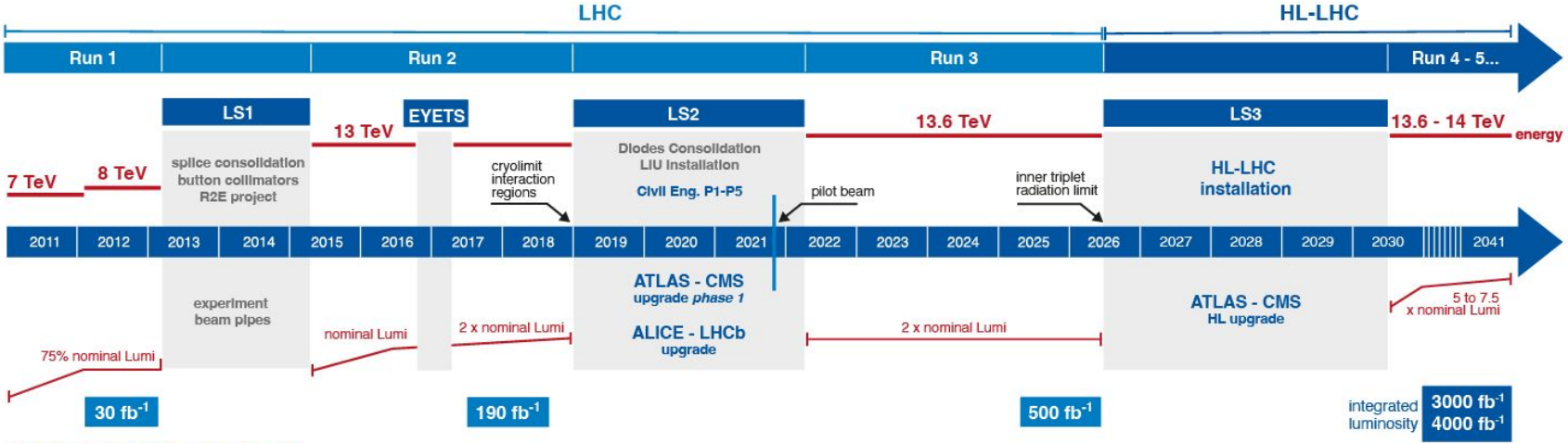
- Large Hadron Collider (LHC)
  - Largest particle collider at a circumference of 27 km
  - $\sqrt{s}$ = 13.6 TeV
  - 4 main experiments: ATLAS, ALICE, CMS, LHCb
- ATLAS
  - General purpose detector
  - Well suited for Higgs/top quark physics and searches

  → Discovery of Higgs boson together with CMS

HL-LHC



- Successive upgrades of the LHC and the experiments
- LHC →High-Luminosity LHC (HL-LHC) for 2030
  - Inst. Lumi. 2×10^{34} $cm^{-2}s^{-1}$ →up to 7.5×10^{34} $cm^{-2}s^{-1}$
  - 3000 fb^{-1} of data until end of programme
- For ATLAS:
  - Phase-I upgrade for Run-3 (2022)
  - Phase-II upgrade for High-Luminosity era



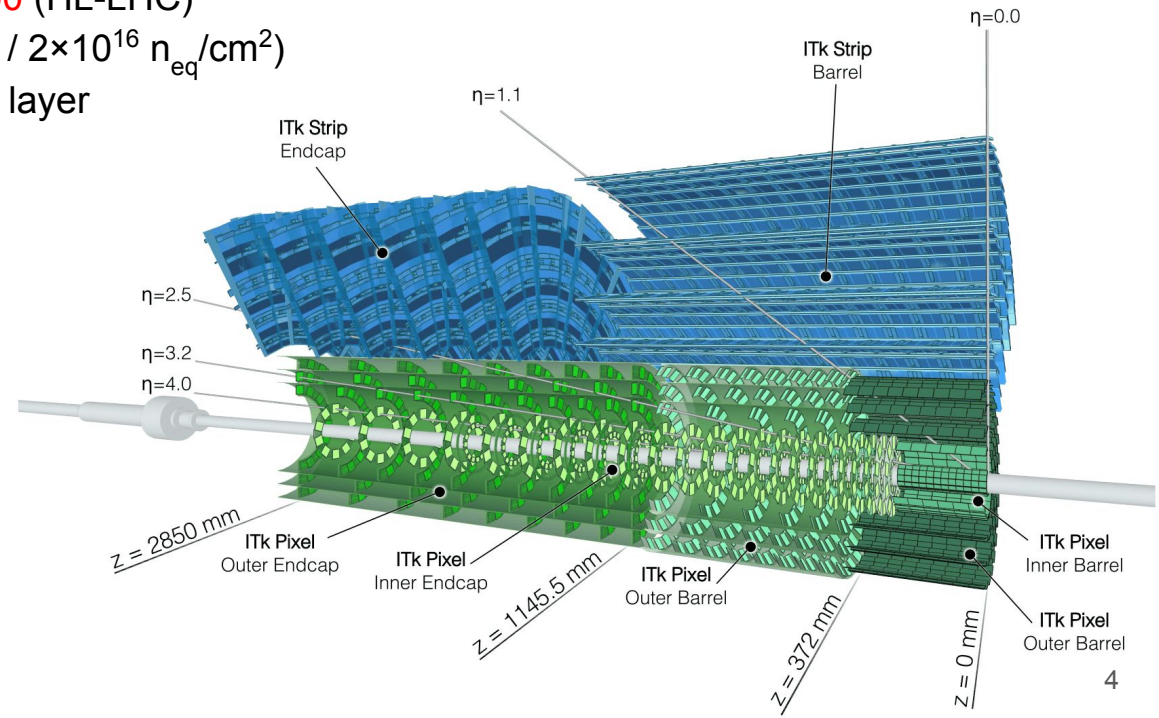
ATLAS ITk

New ATLAS tracking detector to face harsh HL-LHC environment:

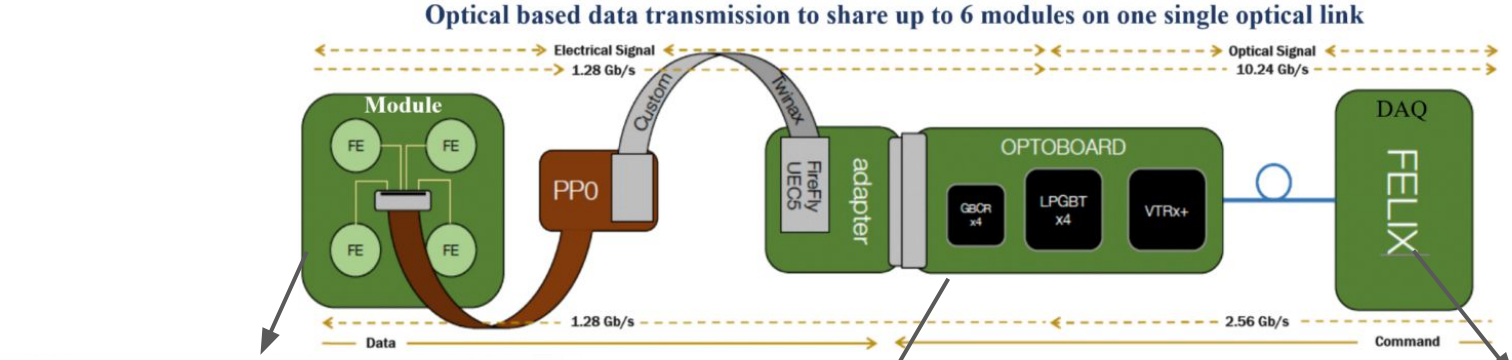
See Tony Affolder's talk
Tuesday 11:15 AM

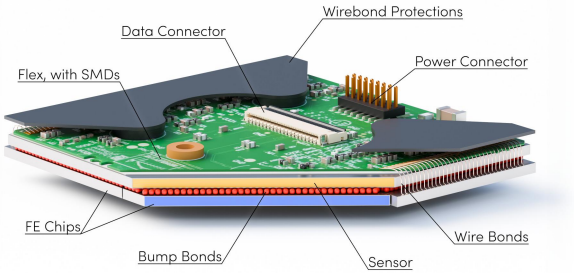
- All-silicon with Pixel and Strip sensors
- Pileup <μ> = 60 (LHC) → <μ> = 200 (HL-LHC)
- Large radiation damage (500 Mrad / 2×10^{16} n_{eq}/cm^2)
- 64 hits/cm^2 hit density in innermost layer

	ID Pixel	ITk Pixel
Active area	≈ 1.9 m^2	≈ 13 m^2
|η| range	|η| < 2.5	|η| < 4
Modules	1744	8372
Pixel size	50 x 400 μm^2 /50 x 250 μm^2	50 x 50 μm^2 /25 x 100 μm^2
Channel count	92M	5G
Trigger rate	100 kHz	**1 MHz**



ITk-Pixel Readout Chain





Hybrid pixel detector modules

- Quad modules (4 front-ends/sensor) or triplets (3x 1 front-end/sensor)
- Innermost layer uses 3D sensors, otherwise planar
- All modules use same front-end chip (ITkPix)

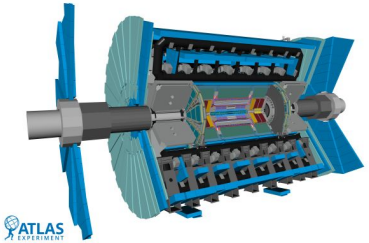
Aggregation and opto-electrical conversion

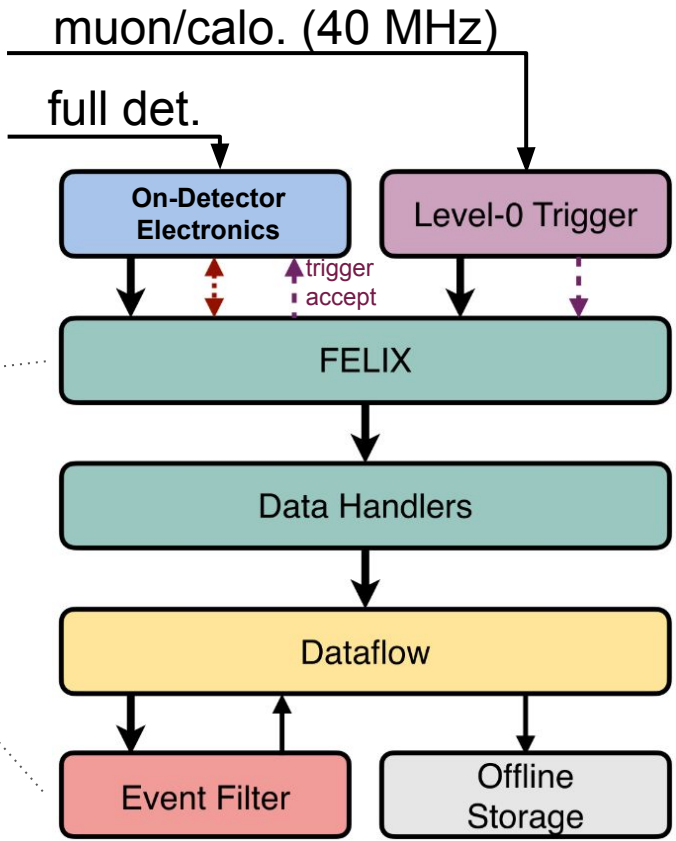
FELIX *(Phase-1/Phase-2)*

- **24 optical links** (bidirectional)
- *FPGA-based* data decoding
- PCIe Gen3/4/5 x16
- + Firmware, Driver, Software

On-Detector | Off-Detector

Phase-II TDAQ System





1st trigger stage
(FPGA-based)
Accept @ 1 MHz

detector readout interface
(hardware ↔ software transition)

detector-specific processing

2nd trigger stage
full event reconstruction
Accept @ 10 kHz

buffer data during reconstruction

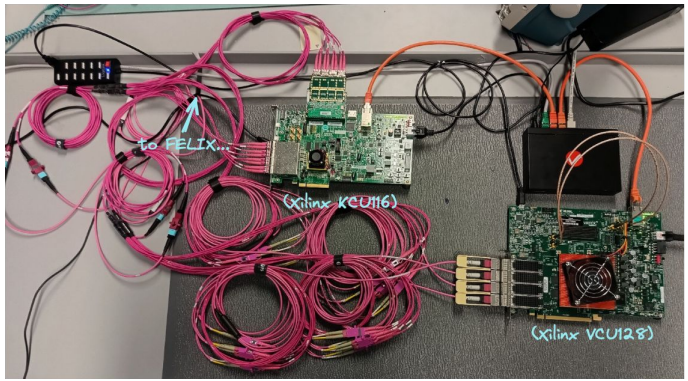
Readout system (FELIX/DH):
Process 5.2 TB/s
at 1 MHz evt. rate

Project Overview

FPGA-based emulator of on-detector components to check readout performance

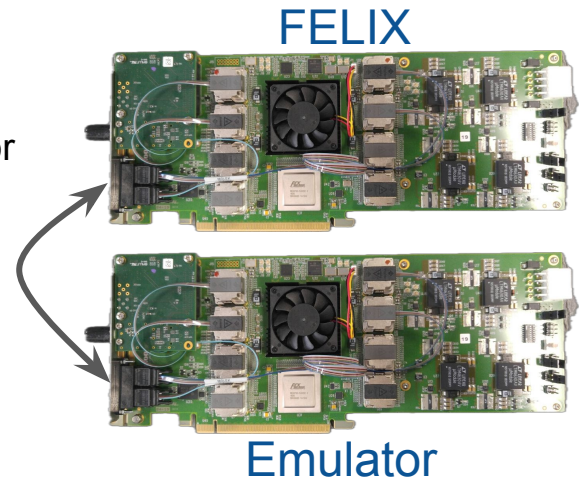
- Emulate frontend chip (ITkPix) and aggregator (lpGBT)
- Mandatory for high-rate tests (lack of real hardware/flexible data generation)
- Useful for DAQ system development

Originally custom platform, now successfully targeted Phase-I FELIX card

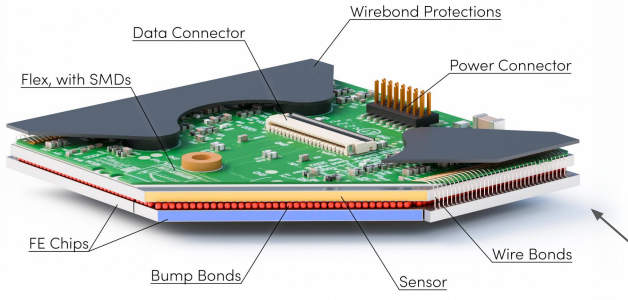


=>

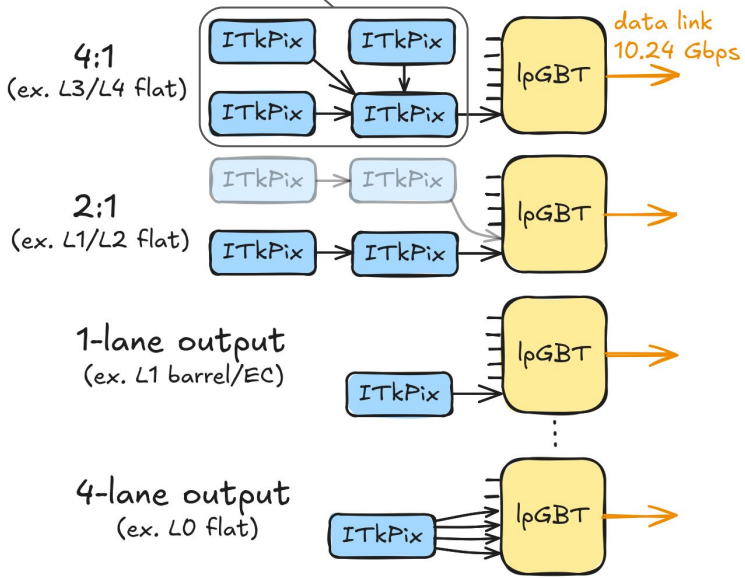
- Integrate into emulator platform from FELIX developers
  →Pixel flavour
  (also exists for Strips, ...)
- Card widely available



ITk-Pixel Link Layout



ITkPix is used in 6 different electrical link configurations
=> All supported by ITkPix emulator and emulator platform

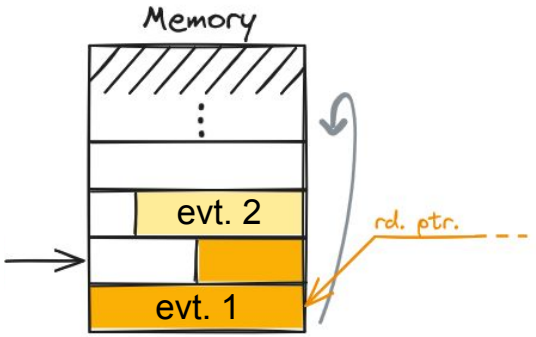


- 576 frontends/PCIe card
- 0.32 Gbps/frontend

- 36 frontends/PCIe card
- 5.12 Gbps/frontend

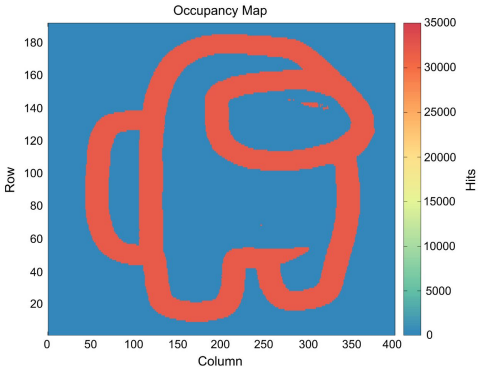
Emulator Setup

- ITkPix emulator instances use precomputed events generated in software
  - Adding trigger/runtime information dynamically
- Fixed capacity per instance (4 kB)
- Can store any number of events up until capacity is exhausted
  - Repeated from start once last is reached



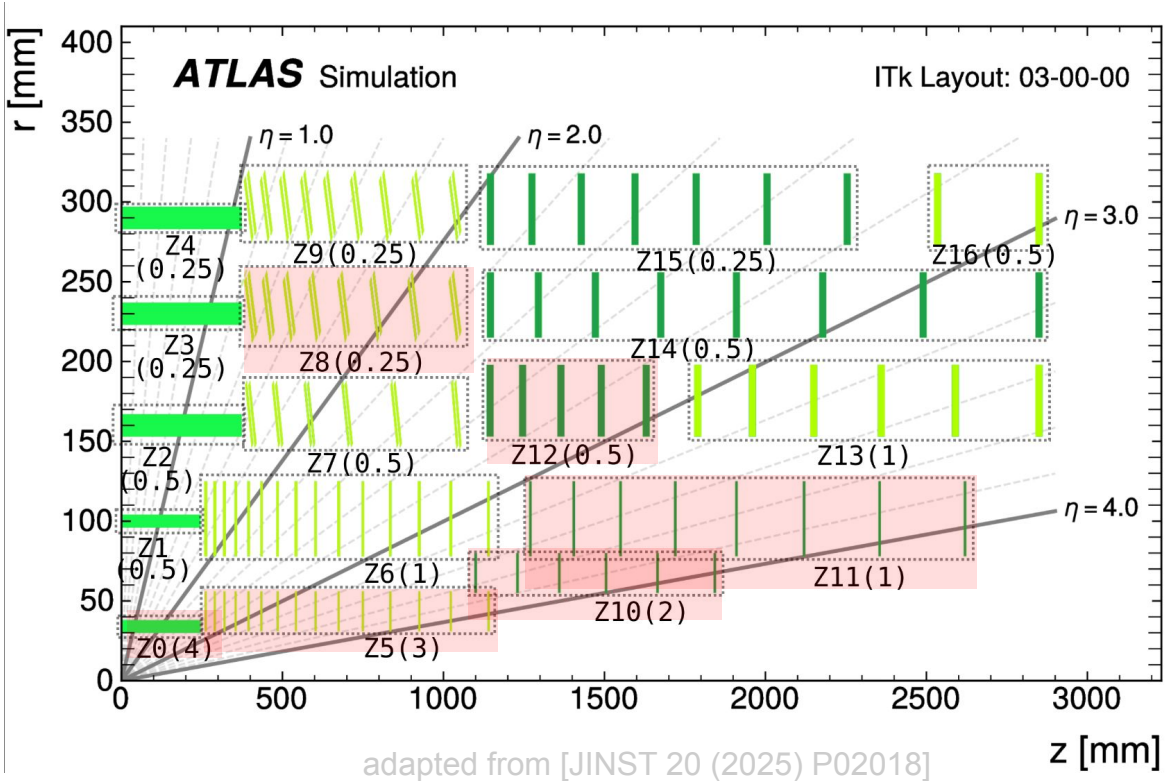
=> Define emulator response at will (up to max. size)

- Software tools developed to generate/encode events
- ITkPix encoding/decoding library used in other parts of ITk DAQ and offline software



(from RD53A emulator)

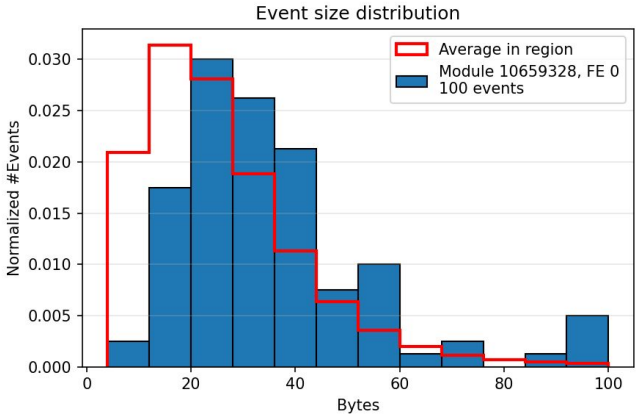
Test Data



adapted from [JINST 20 (2025) P02018]

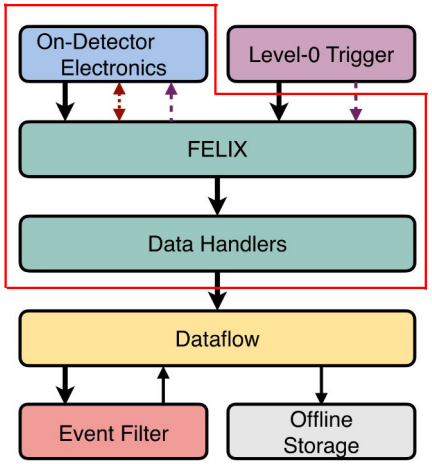
- Emulator memory allows using realistic events in high-rate tests
- Based on 100 simulated $t\bar{t}$ events at <μ> = 200

=> Test events from most demanding modules per configuration
=> Sample event size distribution



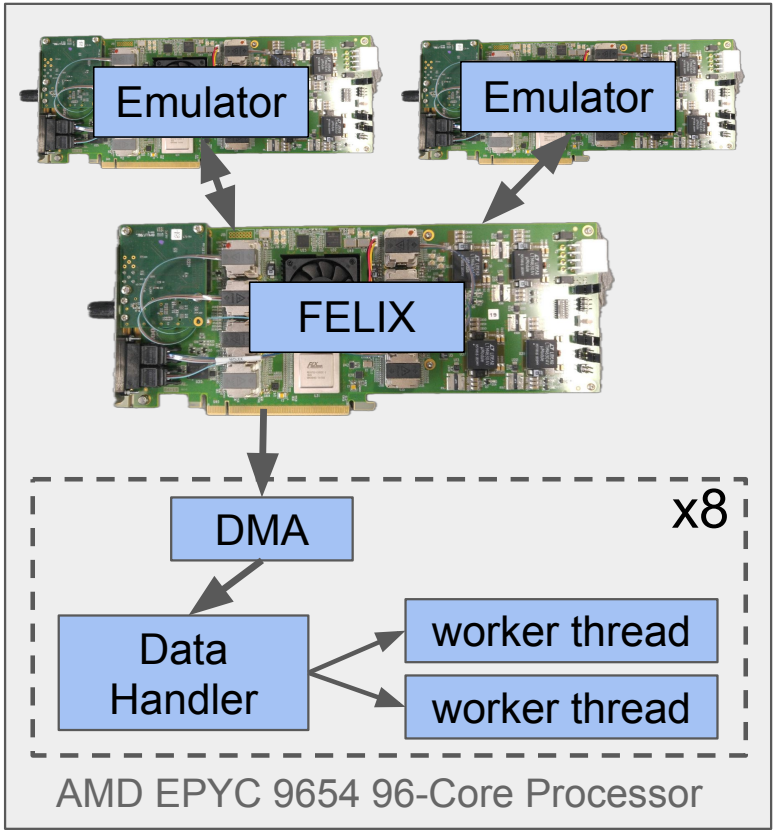
Current Test Results

- Test chain up until Data Handler
  - FELIX-internal trigger generator (fixed frequency)
  - Run on TDAQ testbed
- Test 1 to 4 lane frontend output
  - Link sharing under investigation from FELIX side
- Check matching of trigger information to data



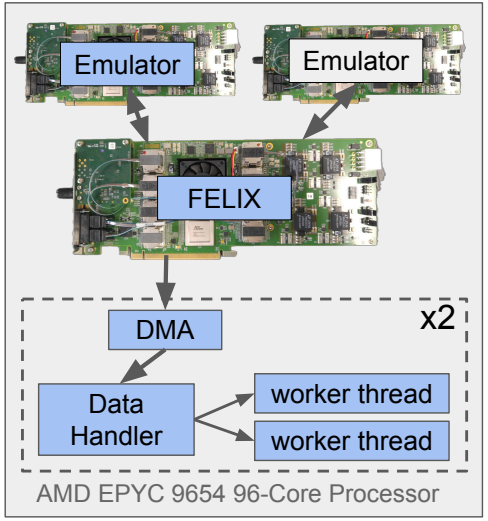
- 8 DMA buffers to relay event data
- 1 Data Handler per DMA

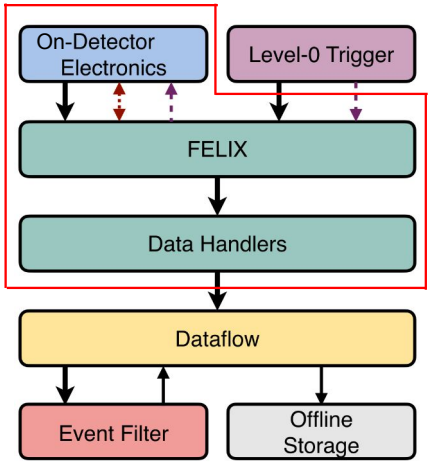
=> 3 links per Data Handler



Current Test Results

- Test chain up until Data Handler
  - FELIX-internal trigger generator (fixed frequency)
  - Run on TDAQ testbed
- Test 1 to 4 lane frontend output
  - Link sharing under investigation from FELIX side
- Check matching of trigger information to data
- Using 2 Data Handlers (6 opt. links)





Test maximum fixed size events:

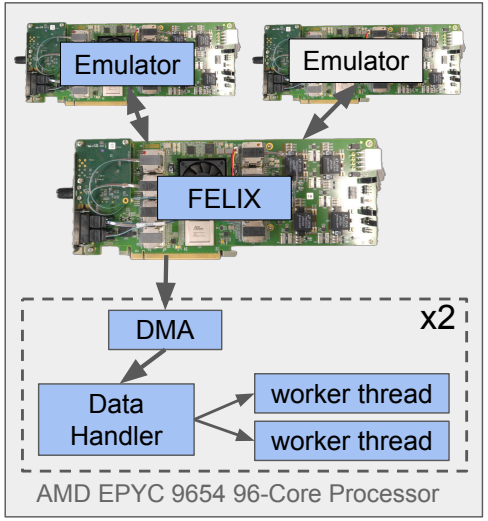
Lanes	Event size [B]	Max. trigger frequency
1	152	1 MHz
2	304	1 MHz
3	456	1 MHz
4	616	750 kHz

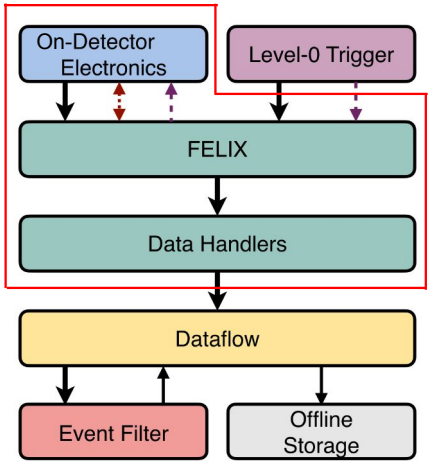
1-lane example:
Link bandwidth = 1241 Mbps
152 B × 1 MHz = 1216 Mbps ✓
160 B × 1 MHz = 1280 Mbps ✗

=> 1 MHz target reached for 1-3 lane output
=> Identify 4-lane output bottleneck in implementation

Current Test Results

- Test chain up until Data Handler
  - FELIX-internal trigger generator (fixed frequency)
  - Run on TDAQ testbed
- Test 1 to 4 lane frontend output
  - Link sharing under investigation from FELIX side
- Check matching of trigger information to data
- Using 1-2 Data Handlers (3-6 opt. links)





Simulated events:

Lanes	Zone	Max. rate	3 opt. links	6 opt. links
1	Z11	1.08 MHz	1.05 MHz	1 MHz
2	Z10	1.38 MHz	1.33 MHz	1.25 MHz
3	Z5	1.2 MHz	1.11 MHz	1.02 MHz
4	Z0	1.33 MHz	1.03 MHz	0.975 MHz

=> Reach 1 MHz target on 1-3 lane output

Conclusion/Outlook

- Created emulator platform for ITk-Pixel DAQ development
  - ITkPix emulator + software for controlling/preparing test data
  - Integrated into FELIX emulation project
- Use simulated collision events to test online software
  - Sample event size distribution by subset of events
  - Limited by FPGA memory size
- Encoding/decoding package shared with ITk online/offline software
- FELIX fit for HL-LHC readout of up to 6 opt. links for 1-3 frontend output lanes

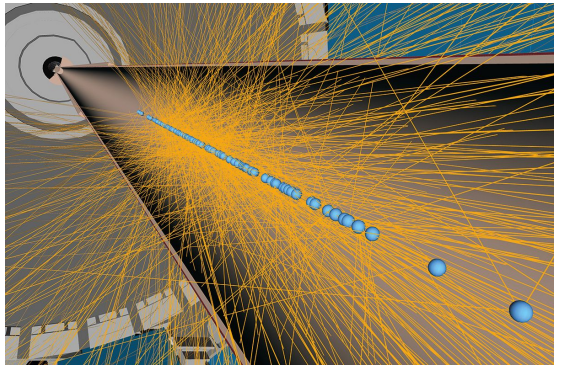
Next:

- Investigate 2:1 and 4:1 link sharing scenarios
  => Emulator helps with development
- Scale to full FELIX card (being debugged)
- Include further components in tests (Trigger Interface, Event Filter)

Thank you for your attention!

Backup

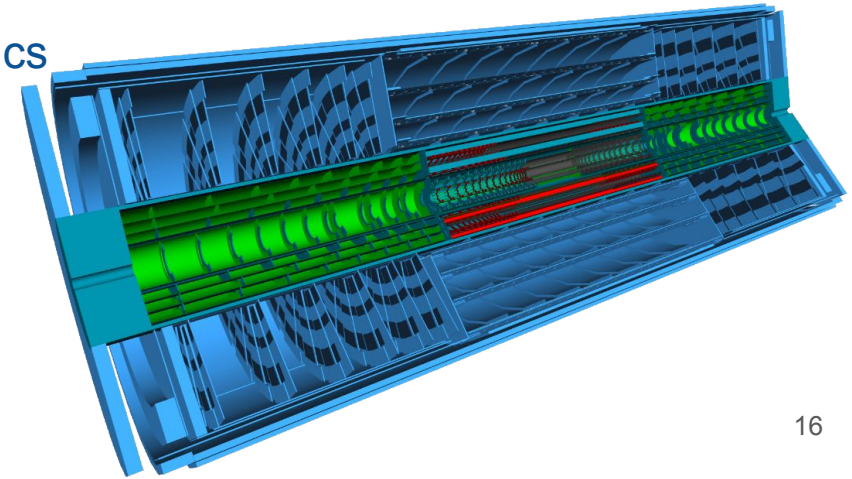
Phase-II ATLAS



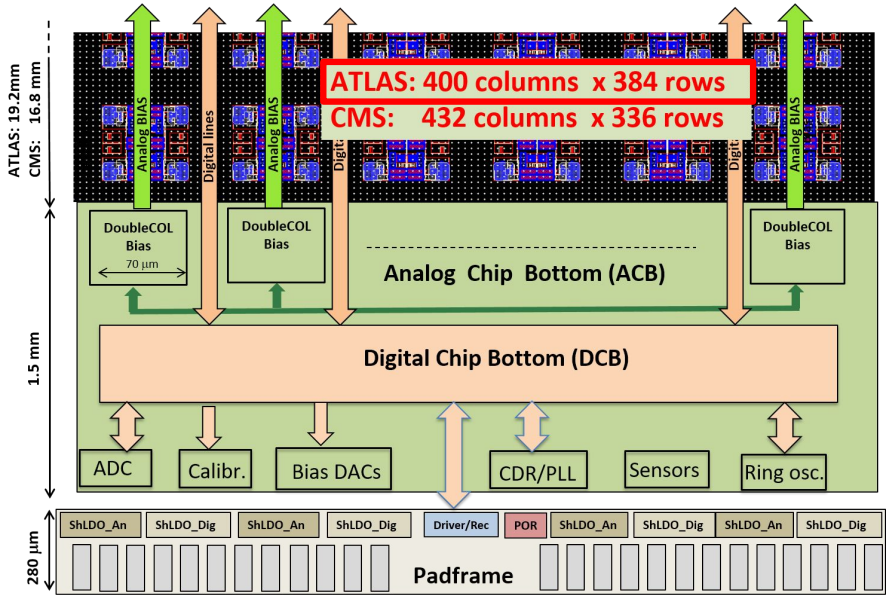
- Harsh operating conditions at HL-LHC
  - Pileup <μ> = 60 (LHC) → <μ> = 200 (HL-LHC)
    → 1 MHz trigger rate (currently 100 kHz)
  - Large radiation damage (500 Mrad / 2×10^{16} n_{eq}/cm^2)
  - 64 hits/cm^2 hit density in innermost layer

=> Phase-II ATLAS upgrade

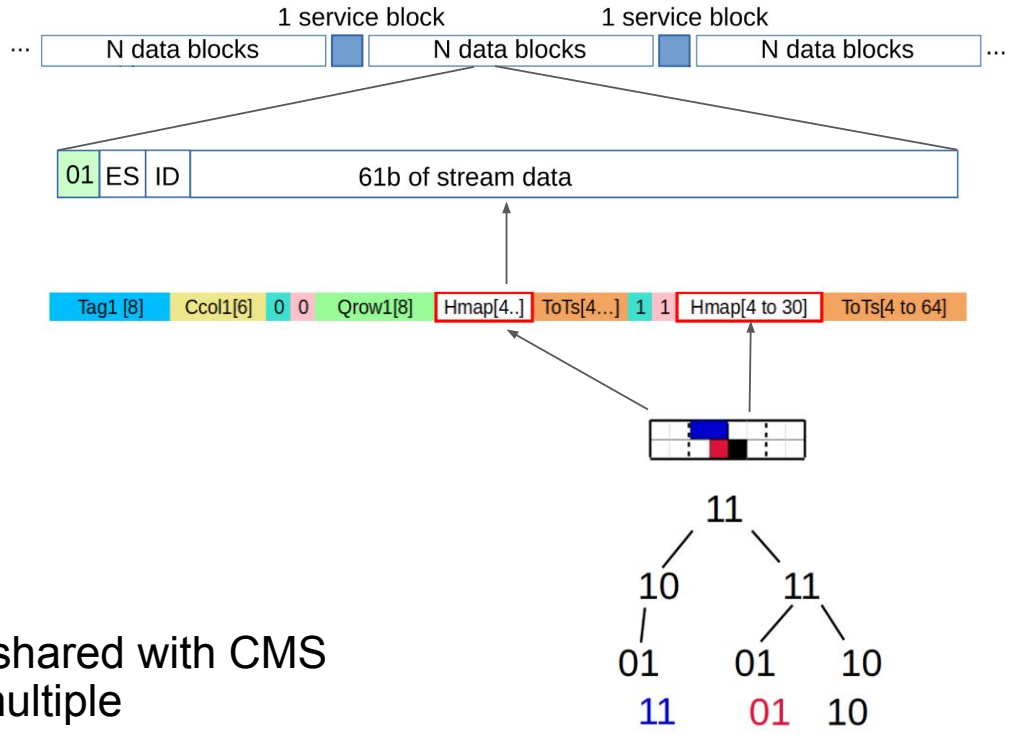
- Upgrade calorimeter/muon system electronics
- High-Granularity Timing Detector (HGTD)
- New Trigger and Data Acquisition (TDAQ) system
- New Inner Tracker (ITk)



ITkPix frontend chip



Event protocol (based on Aurora 64b/66b)



ITk-Pixel frontend chip: ITkPix(V2)

- Designed by RD53 collaboration → shared with CMS
- Bitstream-based event format with multiple levels of compression

Current Test Results

- Data reception test (no checks)
  - Run in local lab.
- Test 1 to 4 lane output
  - Link sharing under investigation from FELIX side
- Using 23/24 links on all DMA buffers

Using simulated events:

Lanes	Theoretical limit	Obs. max trigger rate	Total rate
1	0.95 MHz	0.73 MHz	98 Gbps
2	1.38 MHz	0.975 MHz	103 Gbps
3	1.2 MHz	0.8 MHz	105 Gbps
4	1.33 MHz	0.86 MHz	101 Gbps

- Trigger rate seems limited by total rate of ~105 Gbps
- Possibly related to PCIe Gen3 limit of 126.4 Gbps
  → increased with Phase-II cards