

Upgrade of the Front-End Electronics of the RPC Detector Stack at TIFR

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- Operation of TIFR RPC Stack
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Introduction

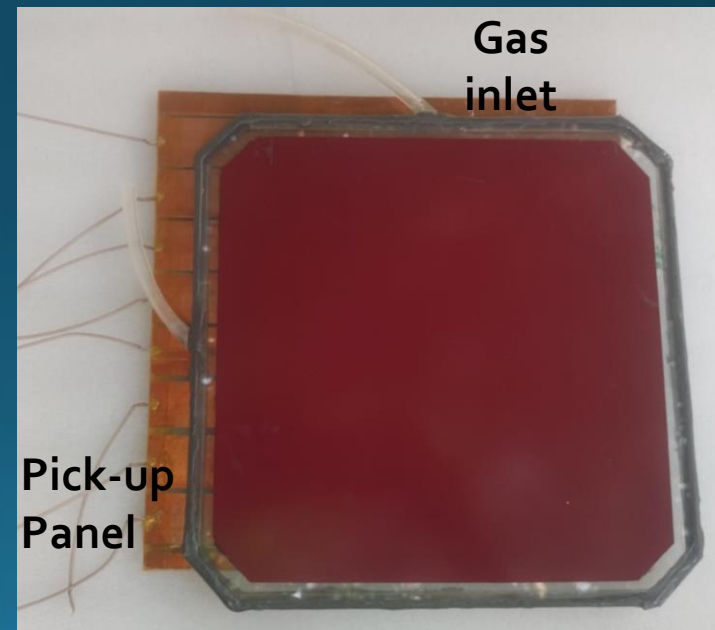
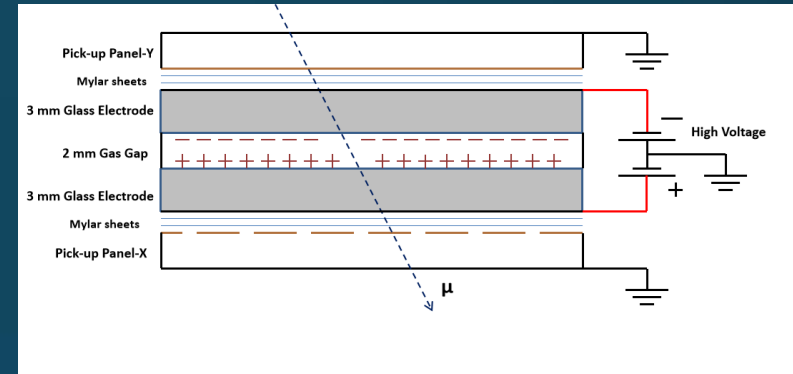
- RPC stack in TIFR is in operation since 2007
- Number of Layers:12
- Active detector element:
1 mtr x 1 mtr RPC
- Mode of Operation:
Avalanche Mode
- Gas Mixture:
R134a:Isobutane:SF6 ::
95.2%:4.5%:0.3%



TIFR 1 m × 1m RPC Stack

Resistive Plate Chamber (RPC)

- 2 glass electrodes
- 3mm thick
- 2 mm Gas Gap
- Pickup Panels for signal Readout
- Operating Voltage about 9.8KV
- Current drawn about 100-200 nA.



DAQ System

- Preamplifiers
- Analog Front End Board (AFE)
- Digital Front End Board (DFE)
- Control and Data Router board (CDR)
- Trigger and TDC Router board (TTR)
- Control Module
- Readout Module
- VME Backend

DAQ System Components

HMC Based Preamplifiers

8 in 1 board

2 stage Cascaded Pre amplifier of gain: 70

No. of Boards in Used: 96



Analog Front End Board (AFE)

16 Channel Discriminator

ECL logic level

16 1F signals

4 Level_0 Signals

No. of Boards in Used: 48

Vth: -1 mV to -1 V



Digital Front End (DFE)

32 ECL input signals

8 ECL level Zero Signals

CPLD based logic

No. of Boards in Used: 24



DAQ System Components ...

Control and Data Router (CDR)

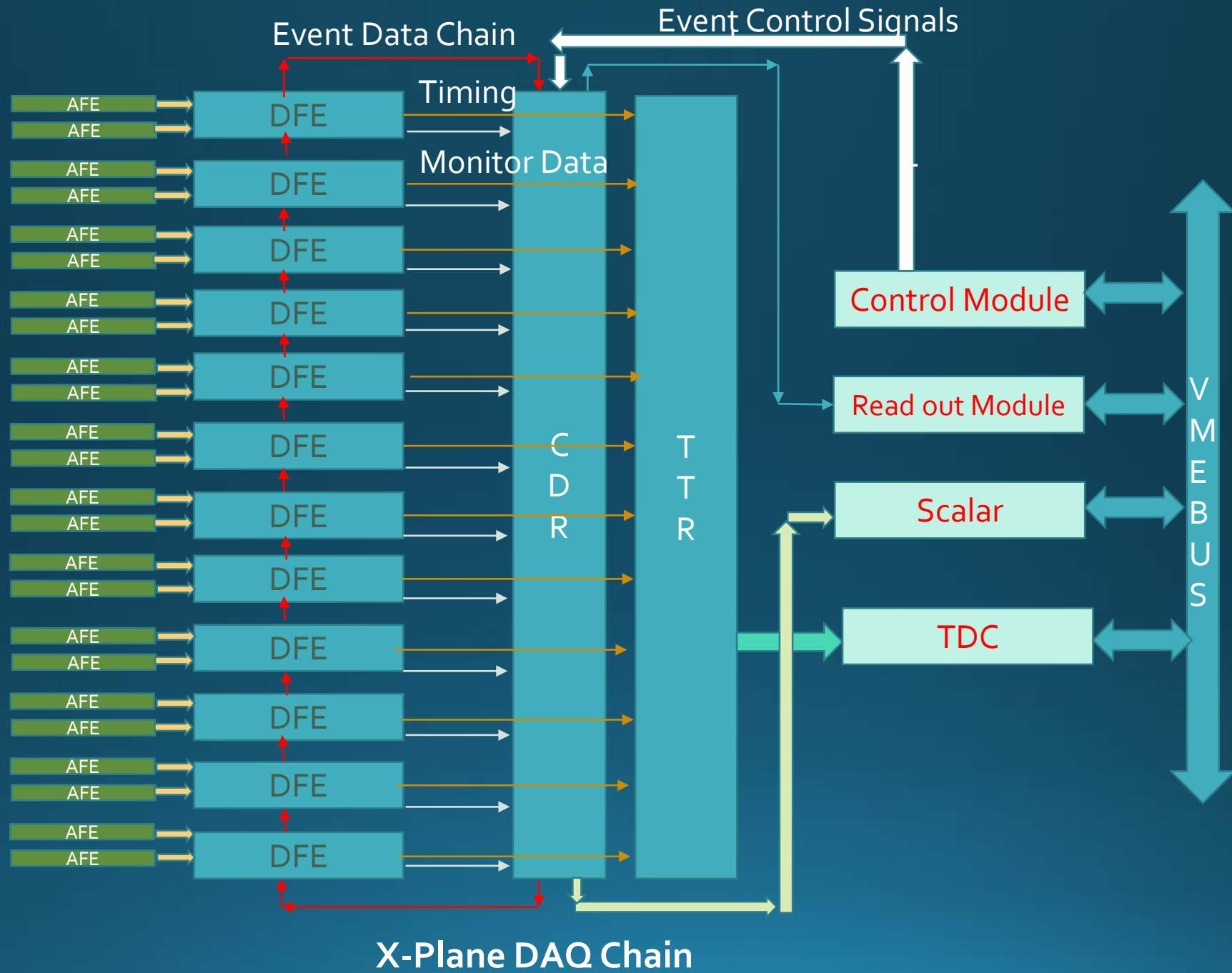
- Control signals from Control module
- Send Control, Event and Monitoring signals to X and Y plane
- Receive the Event and Mon signals
- Transmit it to Readout Module

Trigger and TDC Router (TTR)

- Level one signals from DFE boards
- Segregation of 1F, 2F, 3F and 4F signals
- 1 Fold signals for Timing
- Fold signals in LVDS to Trigger system

Control and Readout Module

- Generate Control Signals for event and Mon data Readout
- Receive the Event data
- Monitoring data to Scalar



X-Plane DAQ Chain

Motivation of Upgradation

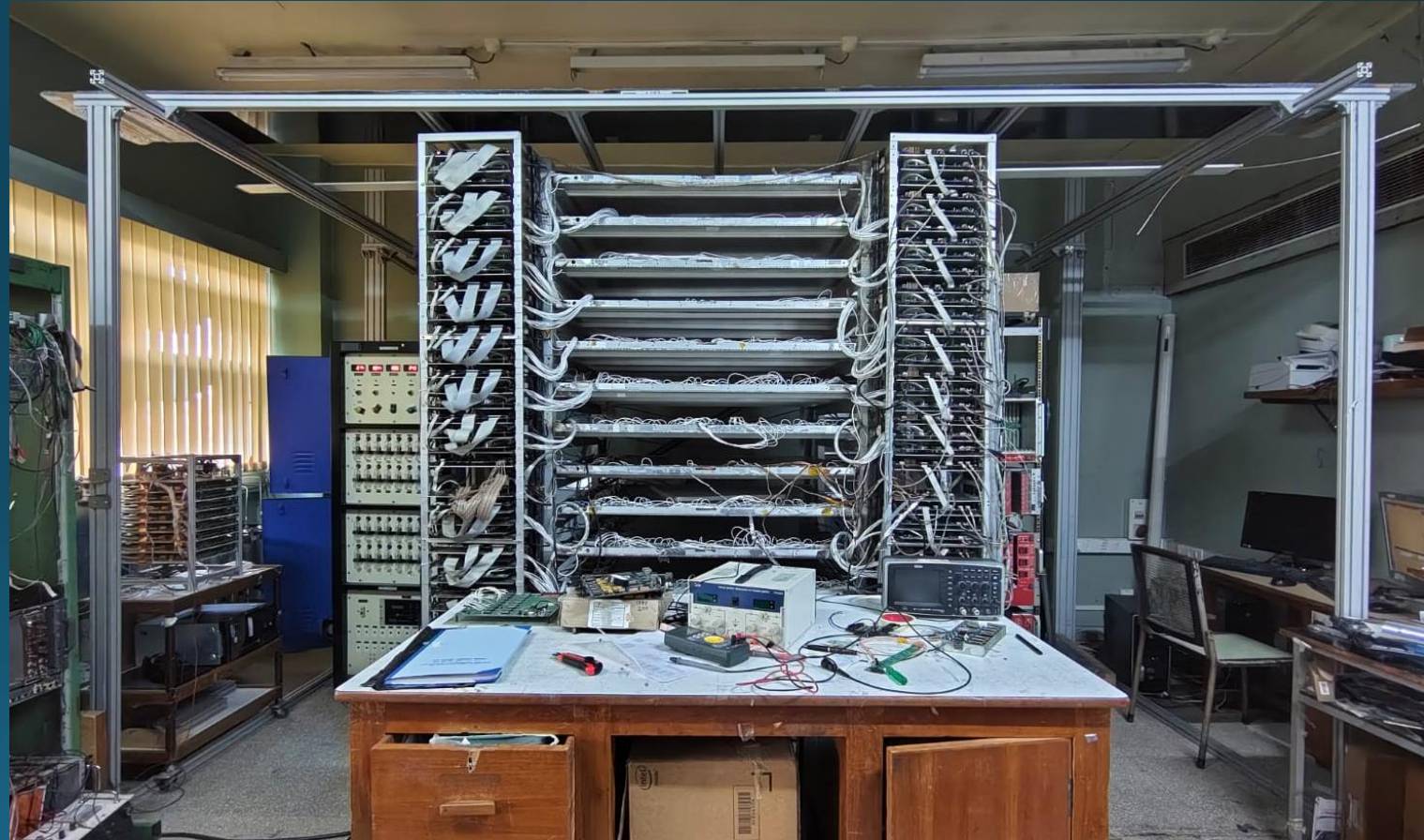
Plan of installation of Cosmic Muon Veto detector (CMVD) at TIFR

Problems faced:

- Electronic Noise Pick-up
- Instability of the Pre-amps
- High Power consumption – HMC & AFEs' power consumption: 56 watt/Layer

Solution:

- Differential signal transmission to reduce the noise
- Use of available NINO 8 in 1 amplifier cum discriminator boards



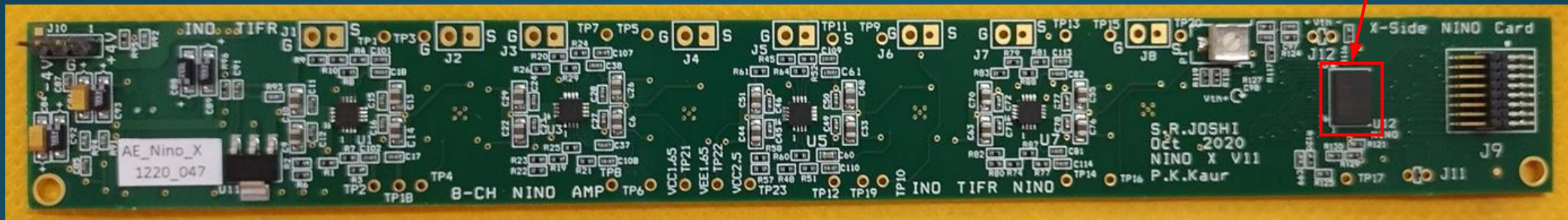
Implementation

- Replacement of HMC based Preamplifiers with NINO Preamplifier
- Replacement of 2 AFE boards with 1 NINO DFE adaptor board
- Patch boards to provide LVDS inputs to DFE
- DC Power distribution
- High Density signal wires routing
- Data collection and analysis

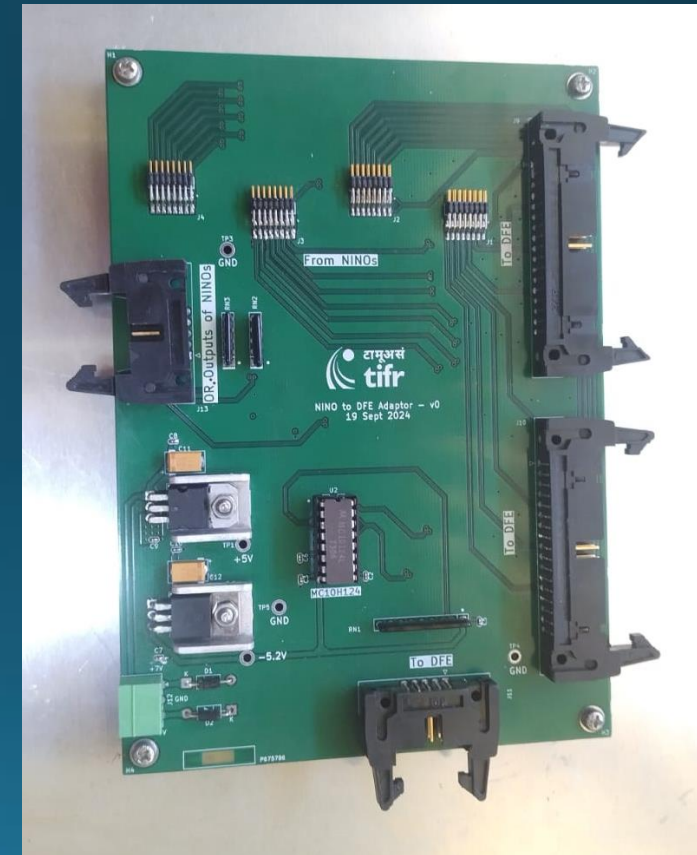
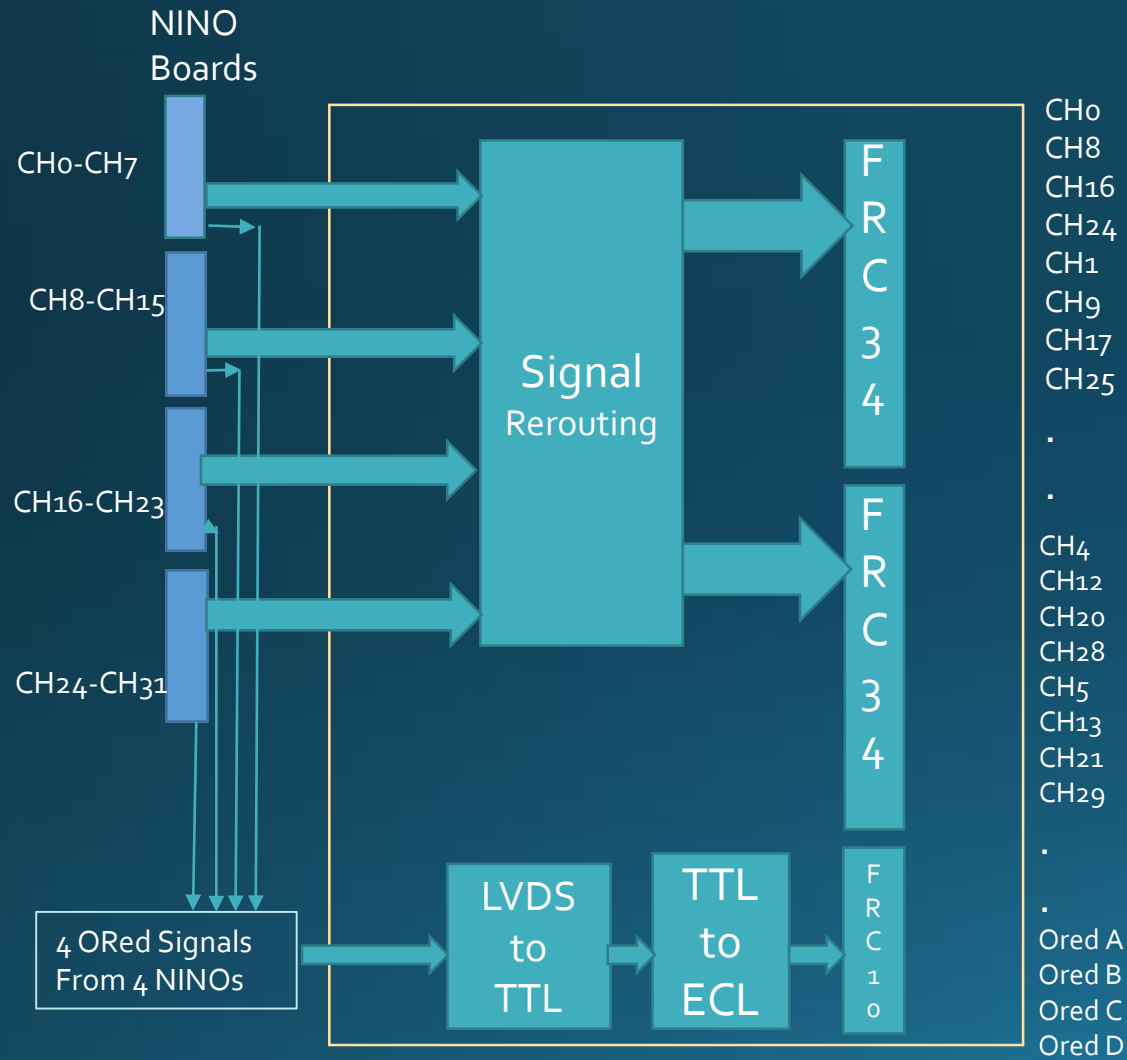
NINO Preamplifier Board

- Custom designed board made using the fast amplifier cum discriminator ASIC – NINO from the ALICE TOF experiment
- 8 individual single-ended inputs
- Operating Voltage 2.5V
- Common Threshold: 10fC to 100 fC
- LVDS signal outputs
- 8 Channel OR-ed LVDS Output

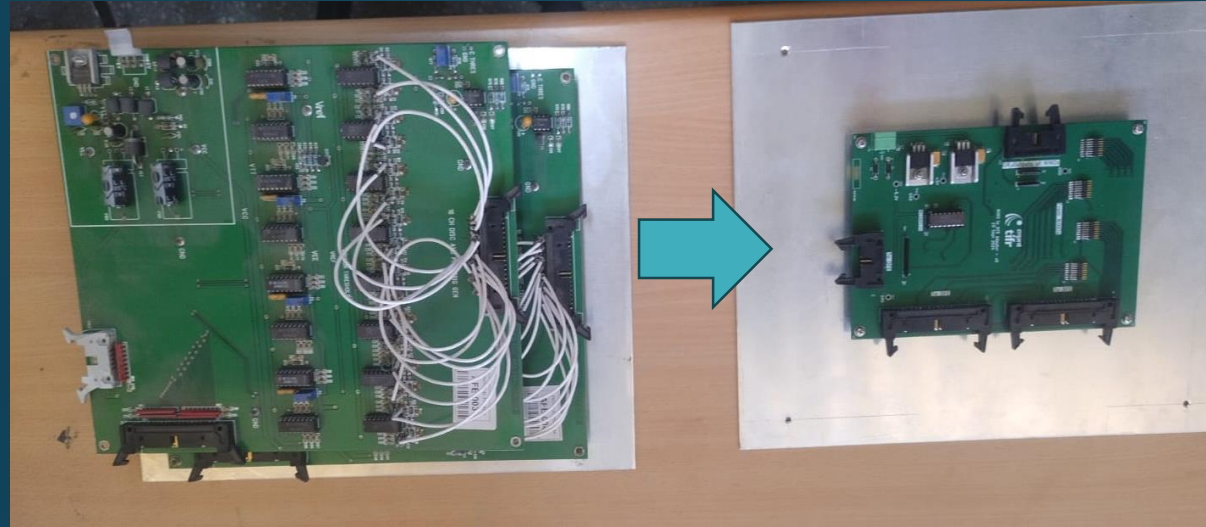
The NINO ASIC



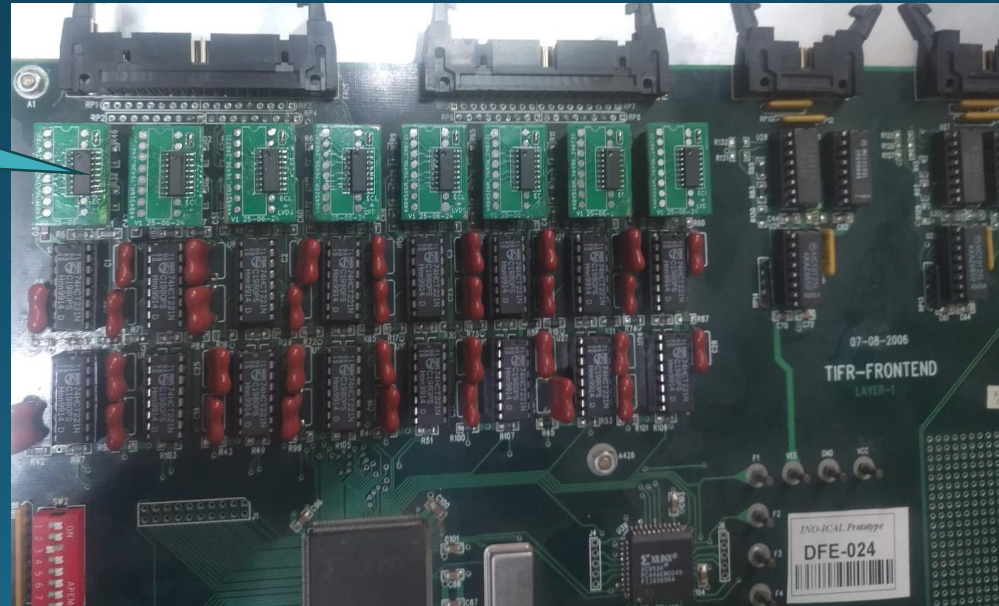
NINO Adaptor Board



Implementation



LVDS-
TTL IC
adaptor



Test Bench



NINO boards

Location

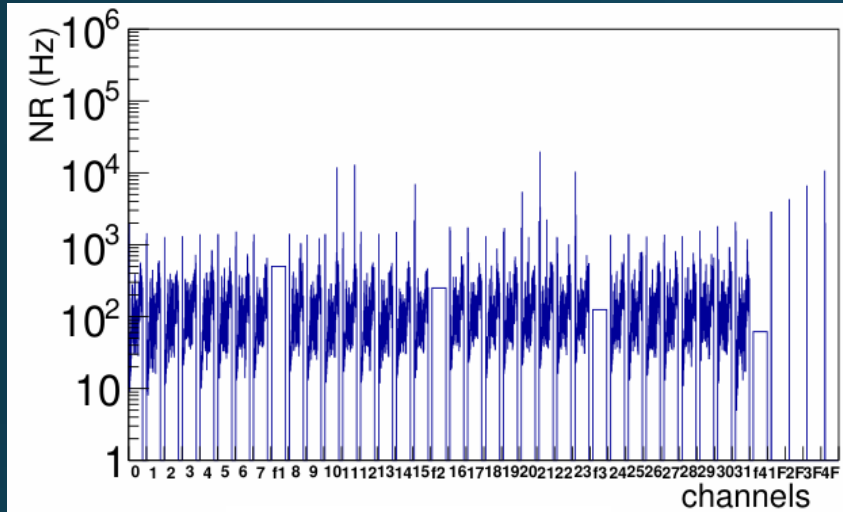
DFE

Adaptor Board

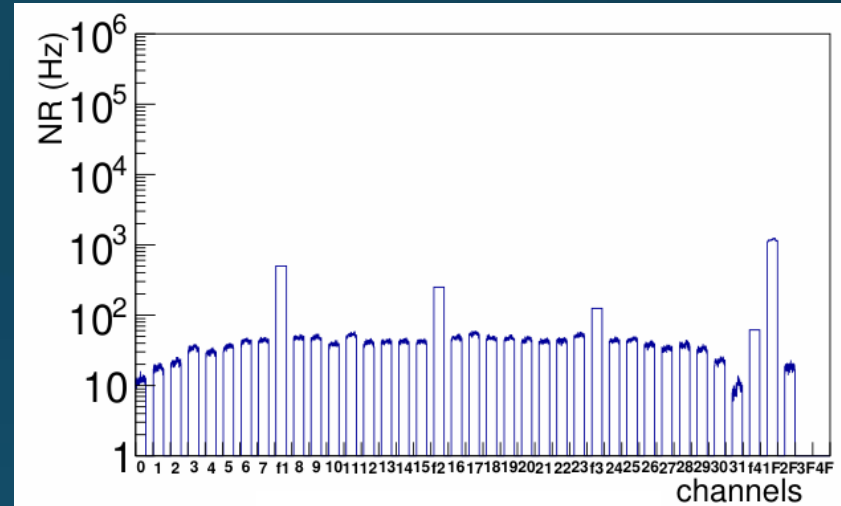
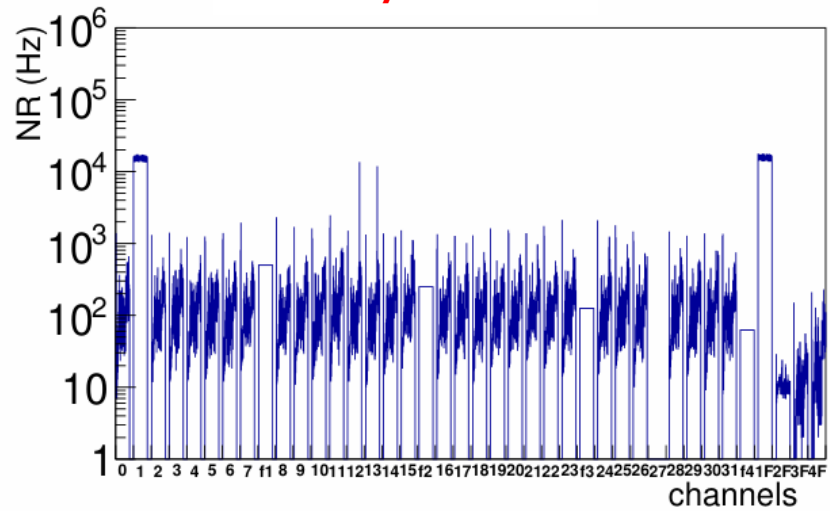
Noise problem and Solution

- Noise pick-up in all layers
- System was highly unstable
- Noisy layers were affecting the stack performance
- Various tests were carried out to find the source of noise
- Change of cables, improvement in ground loop connections
- Finally root cause has been found out
- Old NINO boards does not have ground connections to its mounting holes.
- After externally connecting LV ground to the mounting holes, chassis got LV ground
- Implemented in all layers.
- System is absolutely stable now.

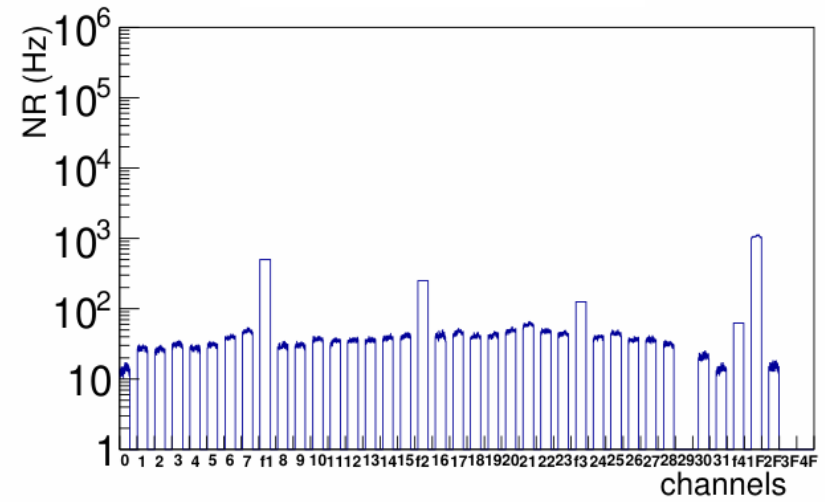
Noise before and after



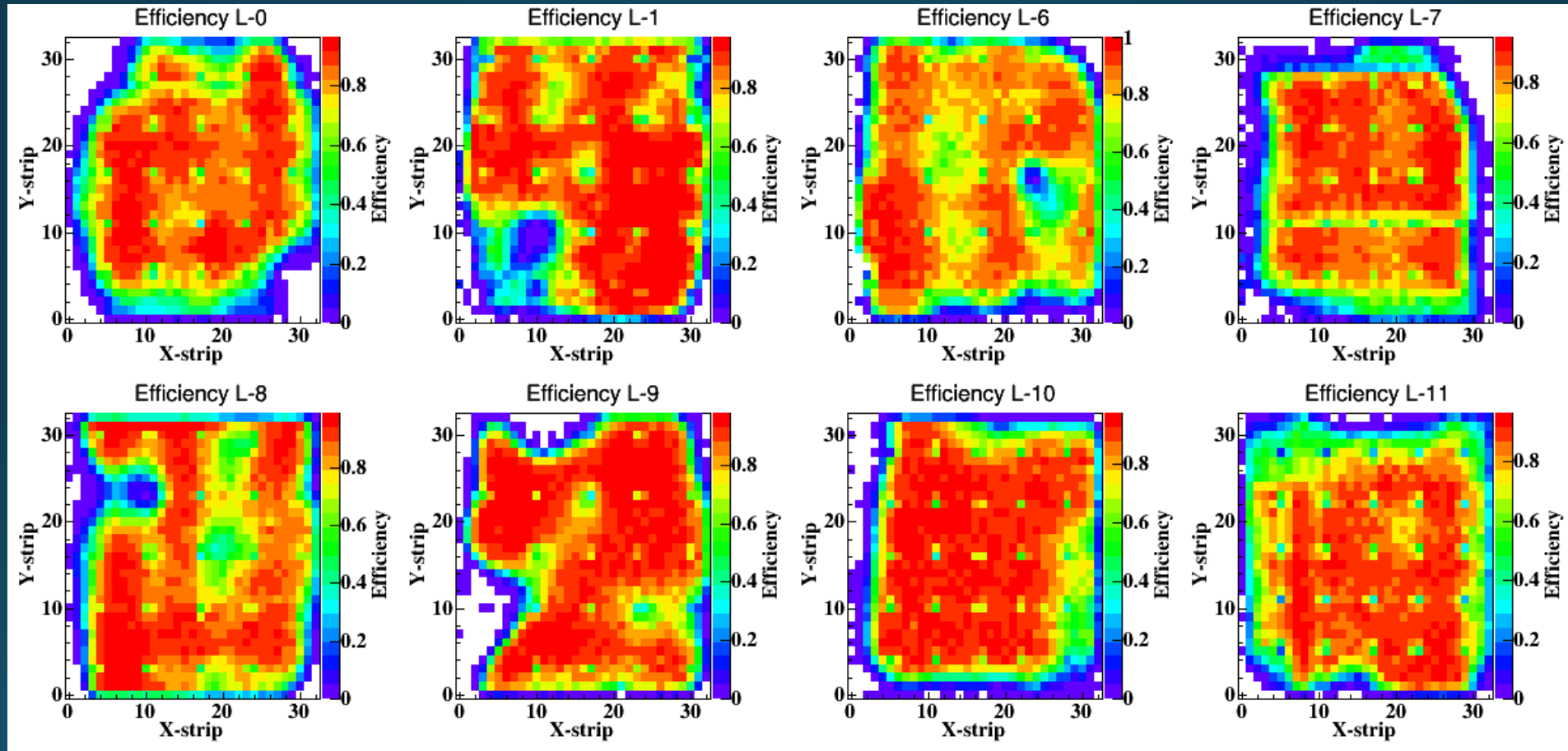
Older system



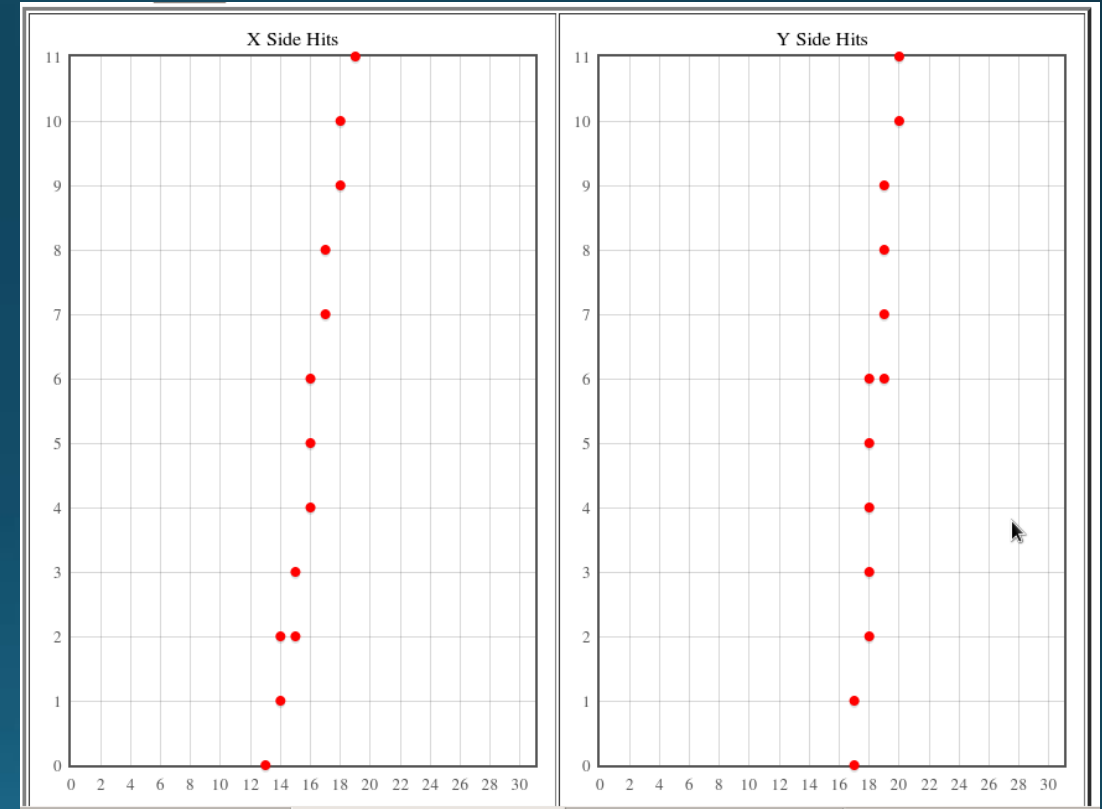
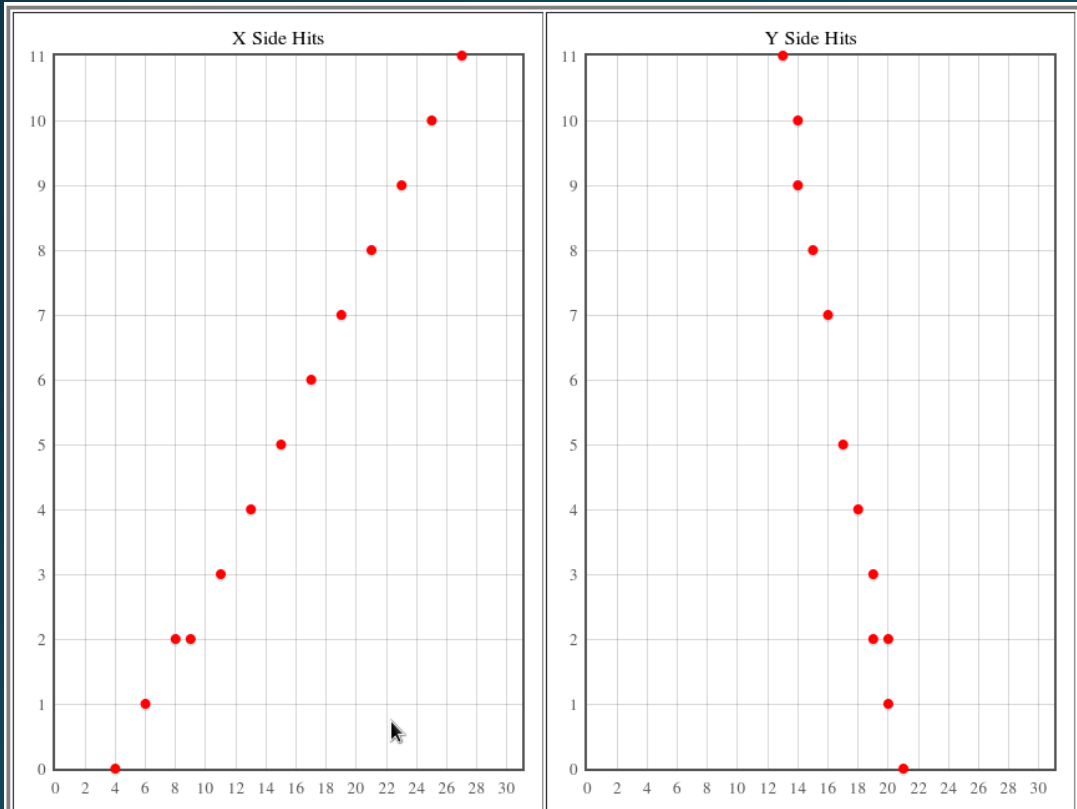
Upgraded system



Efficiency



Muon Tracks



Summary

- All 12 layers have been upgraded with NINO electronics
- Power saving analog front end: power reduced from **56 watt/layer** to **11 watt/layer**
- There is substantial reduction in Noise pick-up
- RPCs with low efficiencies need to be replaced
- RPC stack is ready for CMVD experiment.

Future plan

- Replacement of RPCs having low efficiency
- Testing of CMVD electronics with RPC stack trigger

Acknowledgement

- Shri. Piyush Verma, Shri. S.S. Chavan, Shri. V.V.Asgolkar, Smt. Darshana Gonji, Shri. G.K. Ghodke, Shri. Pramod Pathare, Shri. Ramdas Deshmukh, Rohitsingh Solanki, Prathamesh Narnawre
- Internship students: Adithyan Rajan, Prachi Dighe, Mithilesh Shinde, Shreya Ambadagatti, Manasi Deshmukh

Thank you for your attention

You are welcome to visit our lab at Room number C217, TIFR main building

Pre-Trigger signals

Trigger level 0: Here digital signals with a gap of 8 are ORed to get S1,S2..S8 signals as shown below.

01	02	03	04	05	06	07	08
+	+	+	+	+	+	+	+
09	10	11	12	13	14	15	16
+	+	+	+	+	+	+	+
17	18	19	20	21	22	23	24
+	+	+	+	+	+	+	+
25	26	27	28	29	30	31	32
↓	↓	↓	↓	↓	↓	↓	↓
S1	S2	S3	S4	S5	S6	S7	S8

Level 1 Trigger signals

$$S1 + S2 + S3 + \dots + S8 = 1F$$

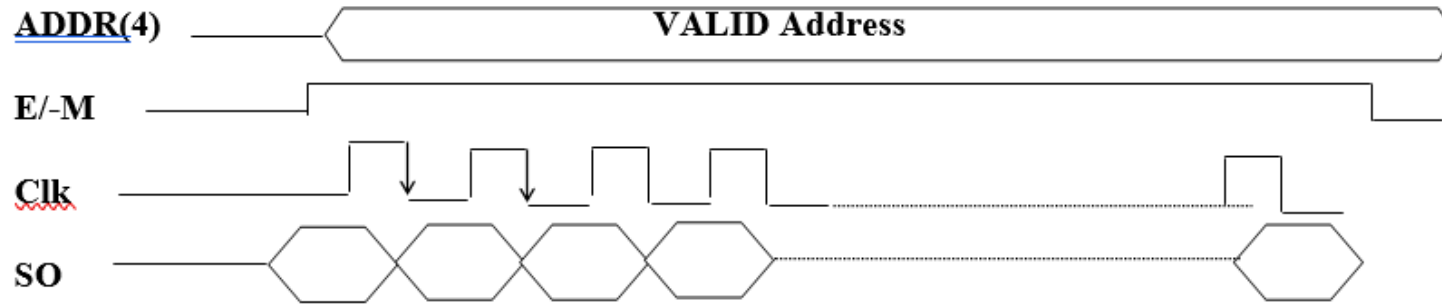
$$S1.S2 + S2.S3 + \dots + S7.S8 + S8.S1 = 2F$$

$$S1.S2.S3 + S2.S3.S4 + \dots + S7.S8.S9 + S8.S9.S1 = 3F$$

$$S1.S2.S3.S4 + S2.S3.S4.S5 + \dots + S6.S7.S8.S9 + S7.S8.S9.S1 = 4F$$

Event and monitoring cycle

EVENT READ OUT CYCLE:



MONITOR CYCLE:

