

Upgrade of the Belle II Vertex Detector with Depleted Monolithic CMOS Active Pixel Sensors

Vindhyawasini Prasad

(On behalf of the Belle II VTX Collaboration)

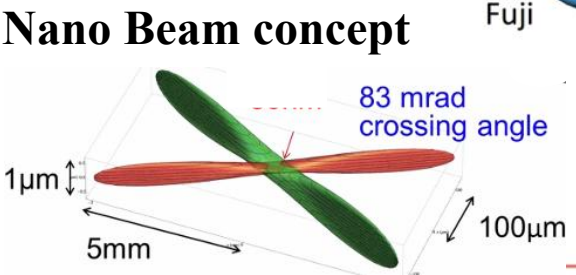
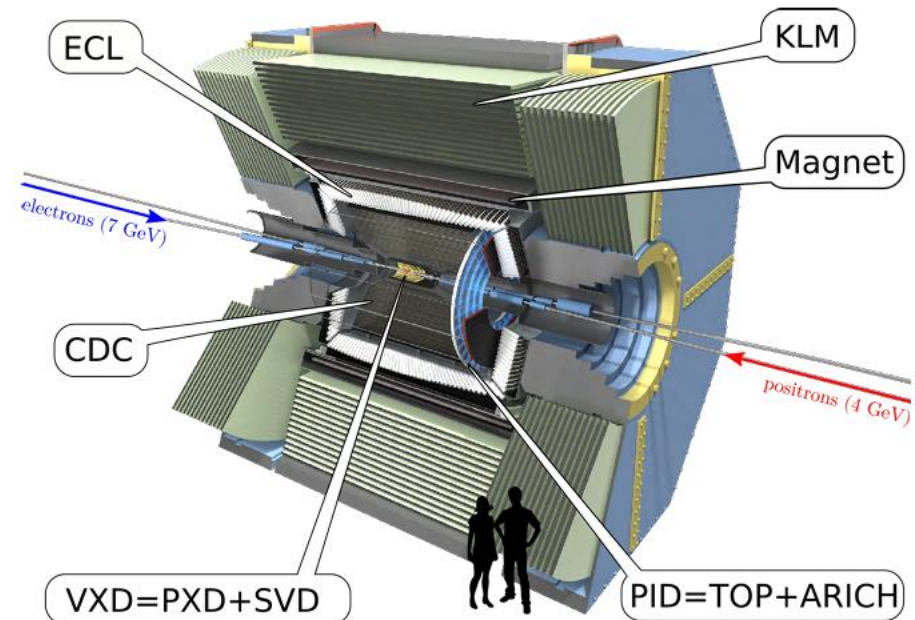
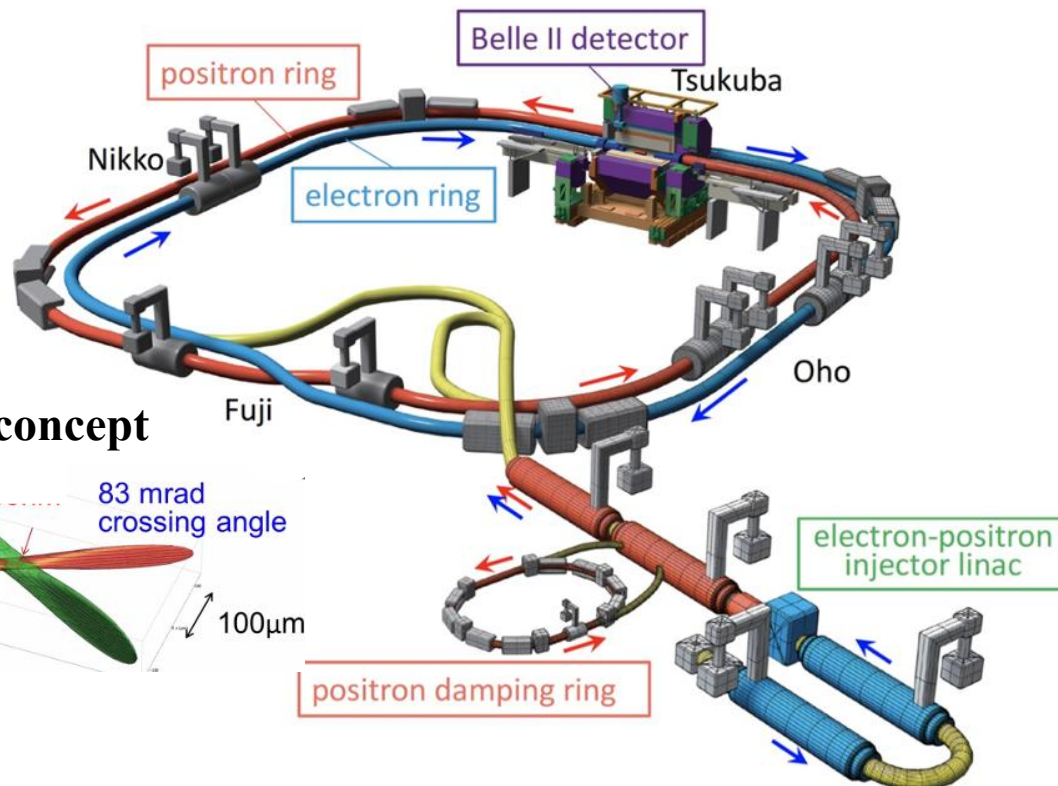
Email: vindy@jlu.edu.cn

College of Physics

Jilin University, Changchun, China



Belle II Experiment



SuperKEKB and Belle II: Located at KEK, Tsukuba, Japan

SuperKEKB: asymmetric e^+ (4 GeV) e^- (7 GeV) collider

✓ High beam-currents and nano-beam schemes to achieve high luminosity with a cost of challenging BKG conditions

Belle II: Flavor physics experiment at SuperKEKB

- Successor of KEKB, Belle operated during 1999-2010
- Verified the Kobayashi and Maskawa theory in study of the CP-violation in the B meson system

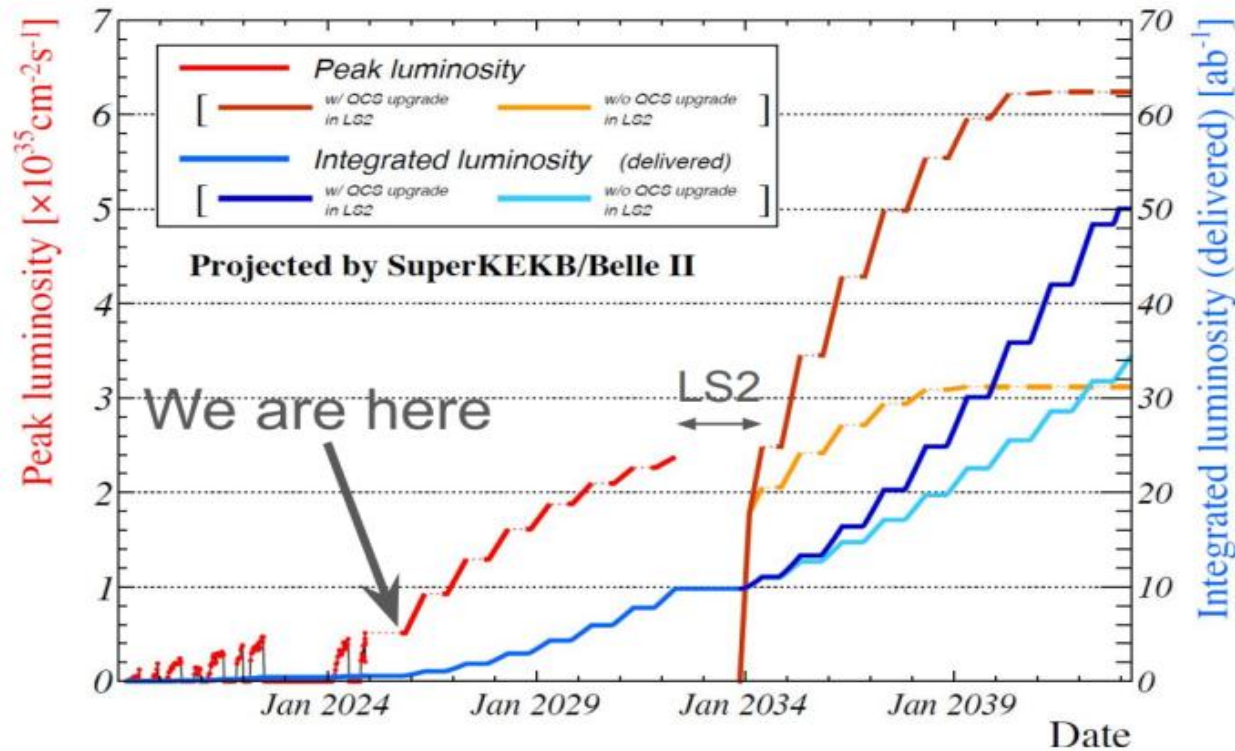
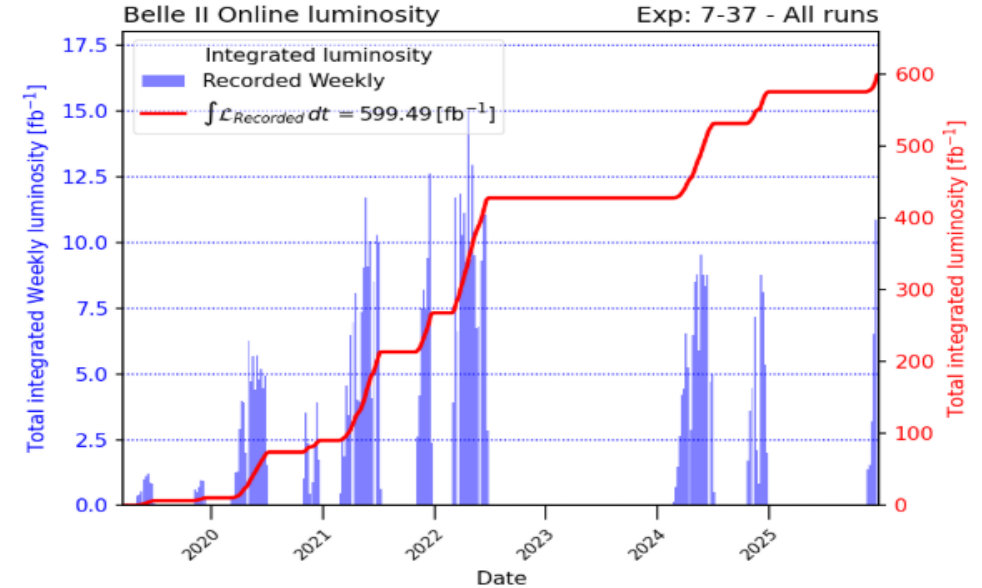


Kobayashi and Maskawa (2008 Nobel Price)

Current Belle II status and possible upgrades

- First collision in 2019
- LS1 (~2023): new collimators, 2-layer PXD, IR improvements
- Run 2 ongoing since 2024 after the long shutdown (LS1) in 2022/23
- Achieved an integrated luminosity 600 fb^{-1} with a peak luminosity of $5.2 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ (world record)
- Target luminosity: 50 ab^{-1} , $6.0 \times 10^{35} \text{ cm}^{-2}\text{s}^{-1}$

With the existing accelerator complex, SuperKEKB is expected to achieve only about $2.0 \times 10^{35} \text{ cm}^{-2}\text{s}^{-1}$ in 2032 [arXiv:2406.19421 \(2024\)](#)



Impact of increased Luminosity

- Both single-beam and luminosity backgrounds are expected to significantly increase [arXiv:2406.19421 \(2024\)](#)
- Expected beam background levels extrapolated to target luminosity (CDR BG V3), with large uncertainties due to scaling assumptions and planned IR changes:
 - PXD Layer-1: $\sim 2\%$ and SVD Layer-3: $\sim 8\%$
- Sub-detector hit rate: CDC ($\sim 300 \text{ kHz/wire}$) and TOP ALD ($\sim 14 \text{ MHz/PMT}$)

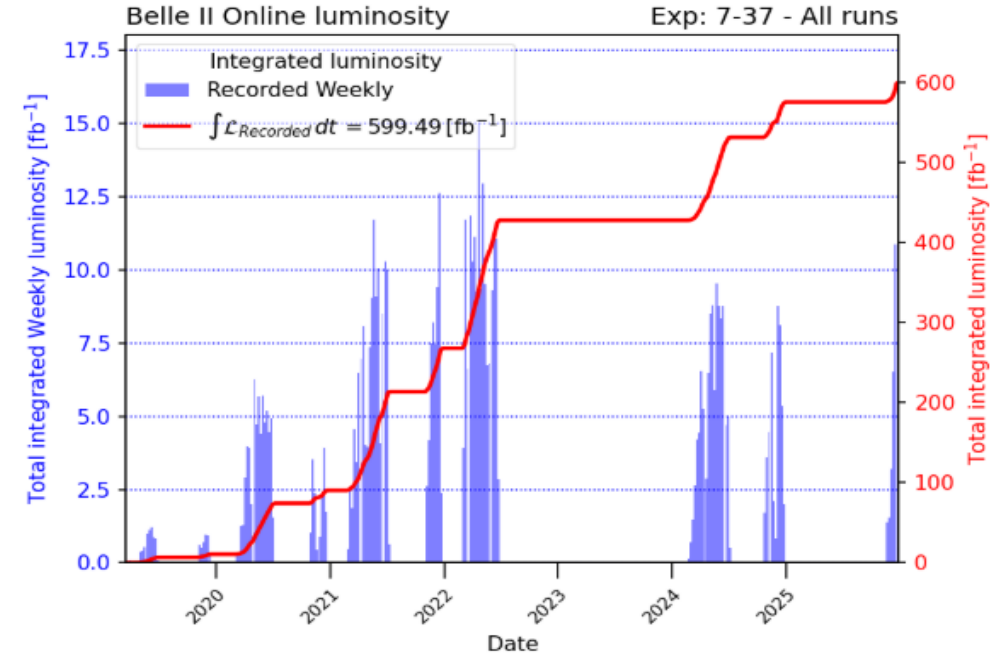
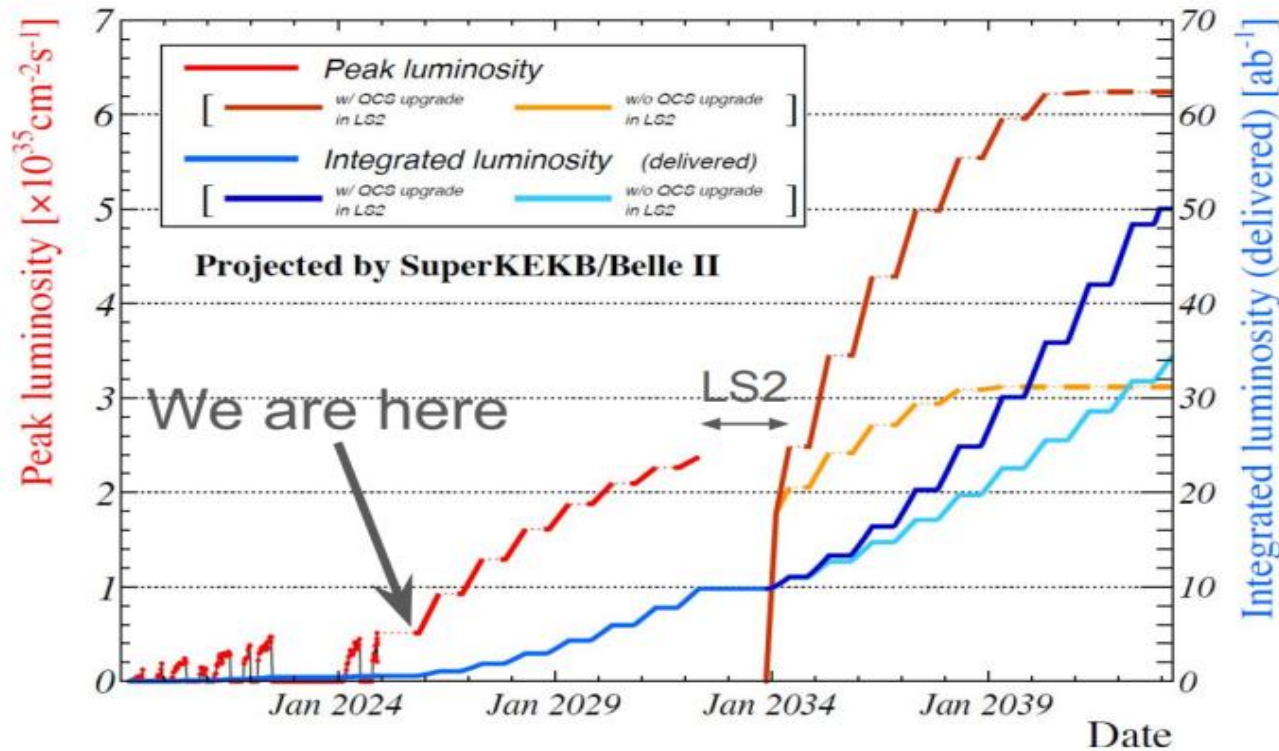
Motivates a major upgrade during LS2 to maintain performance at high luminosity

Current Belle II status and possible upgrades

- First collision in 2019
- LS1 (~2023): new collimators, 2-layer PXD, IR improvements
- Run 2 ongoing since 2024 after the long shutdown (LS1) in 2022/23
- Achieved an integrated luminosity 600 fb^{-1} with a peak luminosity of $5.2 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ (world record)
- **Target luminosity: 50 ab^{-1} , $6.0 \times 10^{35} \text{ cm}^{-2}\text{s}^{-1}$**

With the existing accelerator complex, SuperKEKB is expected to achieve only about $2.0 \times 10^{35} \text{ cm}^{-2}\text{s}^{-1}$ in 2032

arXiv:2406.19421 (2024)



LS2 planned for a major upgrade: 2032

- Achieve target luminosity: $6.0 \times 10^{35} \text{ cm}^{-2}\text{s}^{-1}$
- **Ultimate goal: 50 ab^{-1}**
- Upgrade & Redesign of the Interaction Region (IR) and QCS superconducting final focus
- Window for upgrades of the Belle II detector (including the inner tracking system)

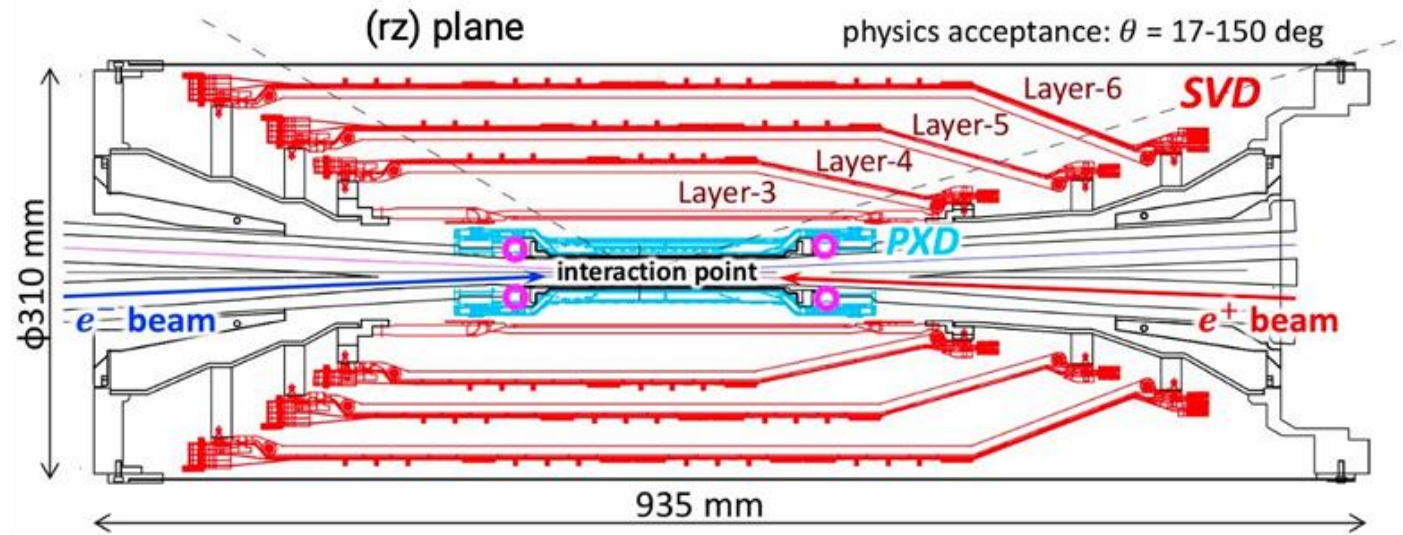
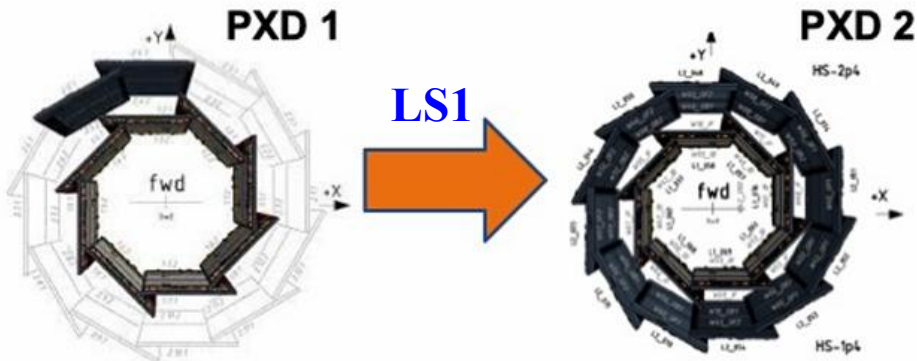
Current Vertex Detector

Belle II vertex detector (VXD): crucial for a precise measurement of decay vertices. It consists of

- Two layers of Pixel Detector (PXD)
 - Located very close to the interaction point.
 - Employs pixel sensors based on DEPFET technology
 - Featuring a pitch of 50-70 μm
 - An integration time of 20 μs
- Four layers of Silicon Vertex Detector (SVD)
 - Utilizes double-sided strip detectors (DSSD)
 - Relatively longer strip lengths of 6 cm
 - Time resolution of 20 ns

VXD total Material budget: 3.5% X/X_0

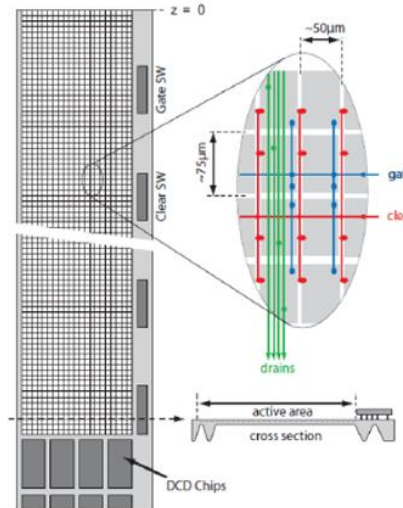
Excellent tracking capabilities but has limitation in handling the high BKG rates from beam BKG extrapolation



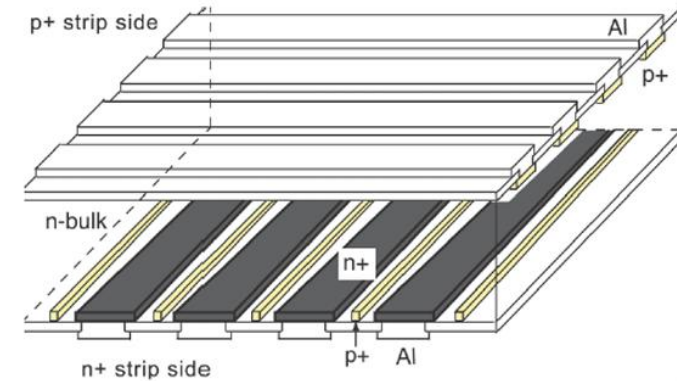
[See Alice Gabrielli's talk for SVD](#)

PXD(Pixel detector)

SVD(Silicon Vertex detector)

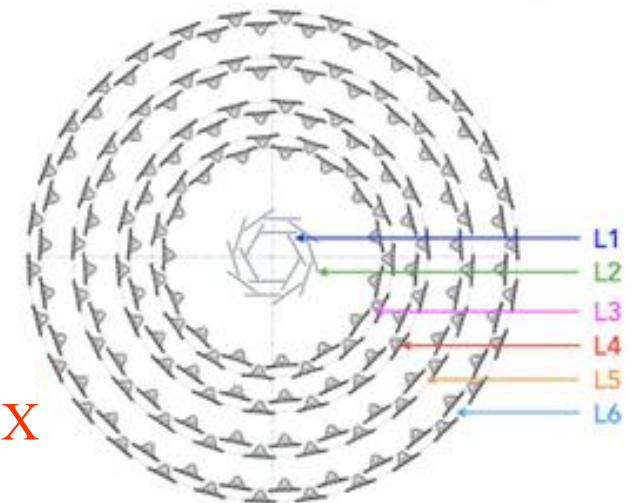
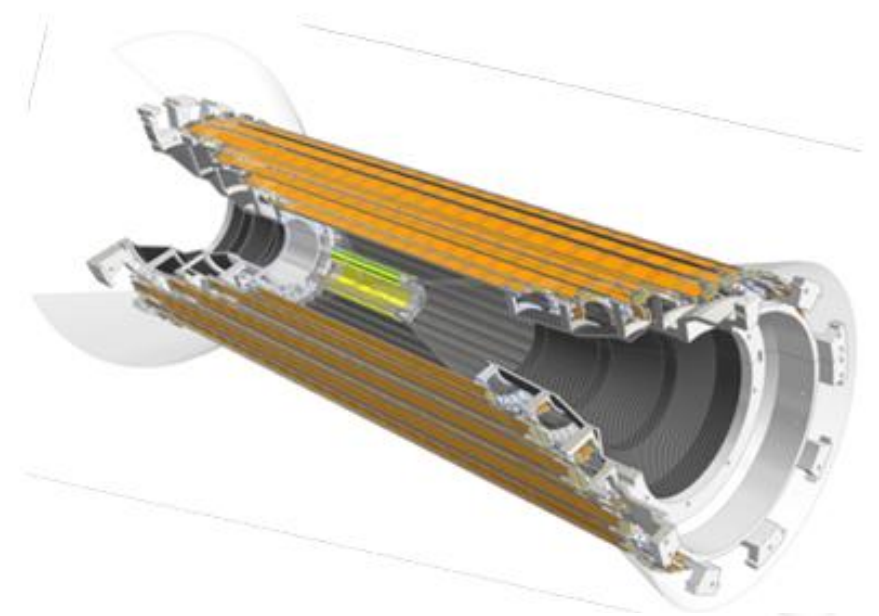


Double Sided Silicon Strip detector (DSSD)



Vertex Upgrade Proposal

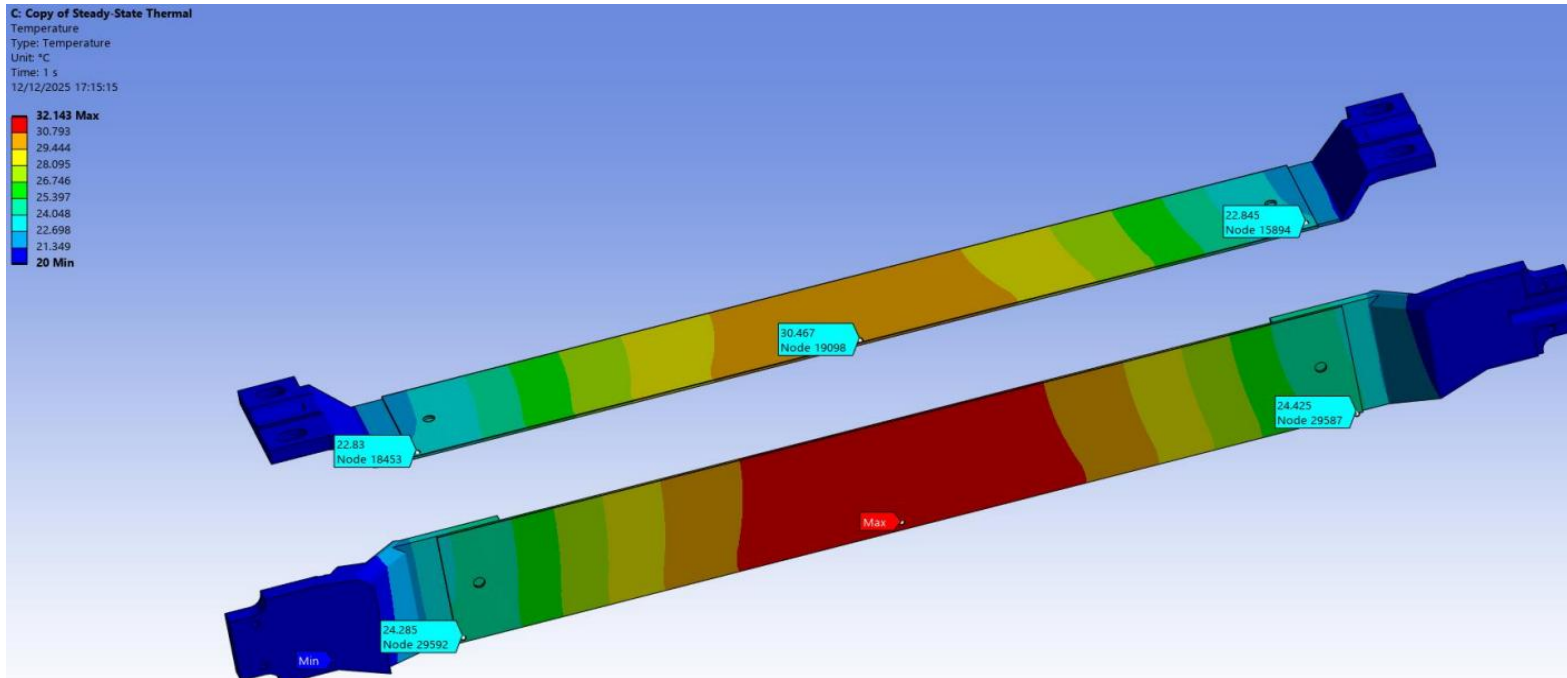
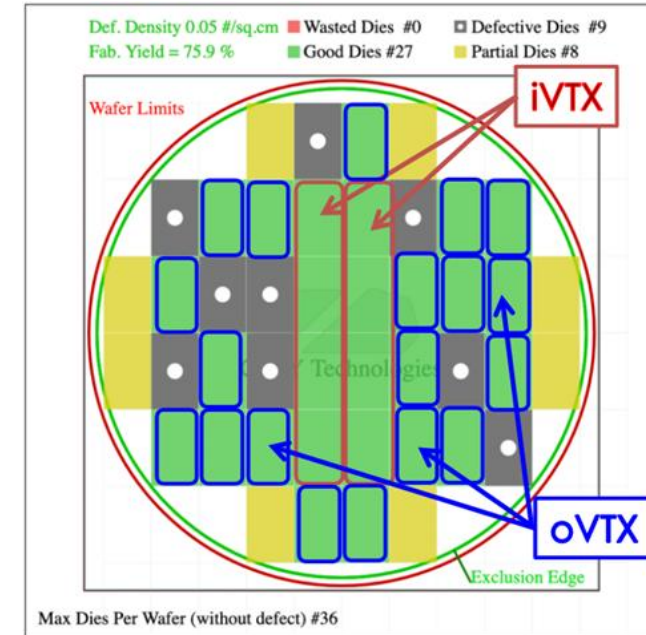
- PXD + SVD \Rightarrow new VTX
- Key performance requirements for the upgrade:
 - Higher spatial and time granularity to cope with the harsh background conditions
 - Spatial resolution: better than $15\ \mu\text{m}$
 - Target for total material budget around $3\% X/X_0$
 - Hit rate capability with trigger: as high as $120\ \text{MHz}/\text{cm}^2$
 - Radiation tolerance: total ionizing dose (TID) up to $100\ \text{Mrad}$ and non-ionizing energy loss (NIEL) fluence of $5 \times 10^{14}\ \text{n}_{\text{eq}}/\text{cm}^2$ in the innermost layer.
 - Power dissipation: target to about $200\ \text{mW}/\text{cm}^2$ to minimize material budget
- A depleted monolithic active pixel sensor (DMAPS) vertex detector
 - Baseline: 6 layers
 - Radius: $14\ \text{mm} \sim 140\ \text{mm}$
 - Improve low-momentum tracking and impact parameter resolution



6-layer VTX
baseline

iVTX: VTX inner layers

- iVTX consists of 2 inner layers
 - Radii: 14 and 22 mm, length ~120 mm
 - Silicon-based ladder concept with post-processed redistribution layers (RDL) for interconnections
 - Target material budget ~0.3% X/X0 per layer
 - Ladder assembly starting from four adjacent OBELIX chips from the same wafer
 - Post-process RDL used for interconnections among chips



- Cooling system is under development
 - Passive conduction cooling using highly conductive thermal material (TPG)
 - Design requirement: ladder temperature below 40 °C

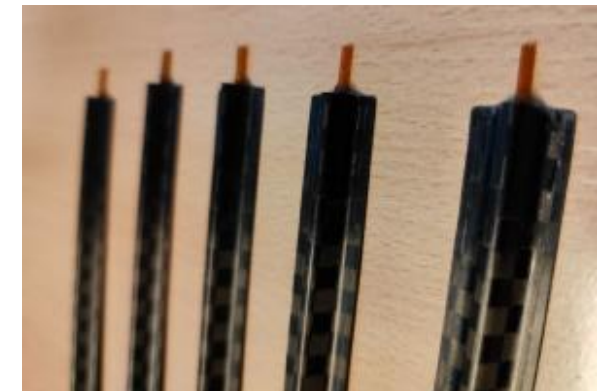
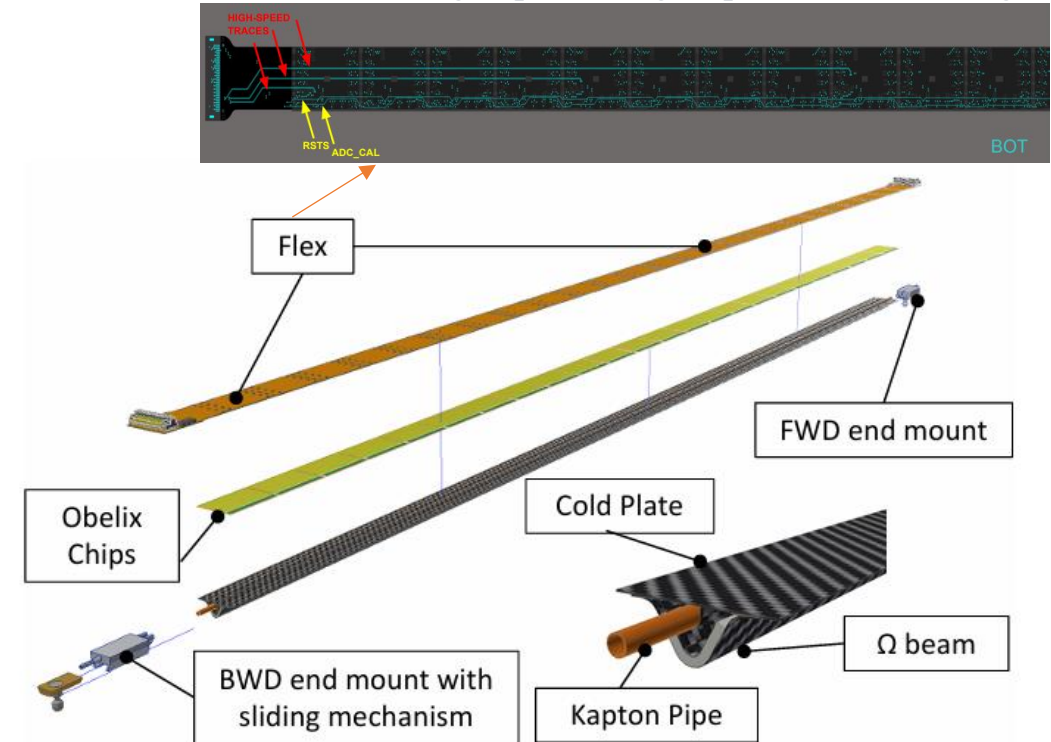
oVTX: Outer VTX layer design

- oVTX will span up to 140 mm with 3 or 4 additional layers
- It is based on a conventional ladder design inspired by the ALICE ITS.
- Each ladder consists of an omega-shaped carbon-fiber structure with Airex foam as core material.
- Material budget $\sim 0.6\%$ X/X0 per layer
- Flex circuits connect up to 12 OBLIX chips to a module, which supplied and read out from the end of the ladder.
- A 70 cm long prototype ladder has been mechanically and thermally characterized, showing performance well within specifications.

New Layer 6 Ladder Prototype (Reinforced Omega + Cold Plate,
Length: 730 mm)

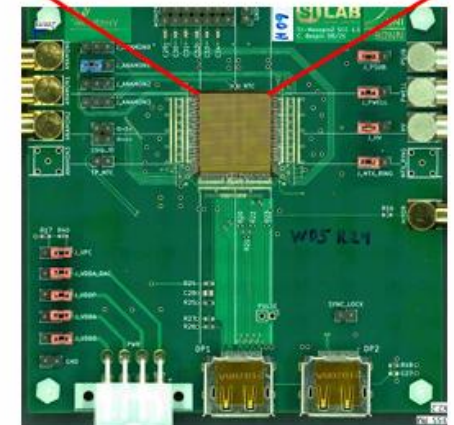
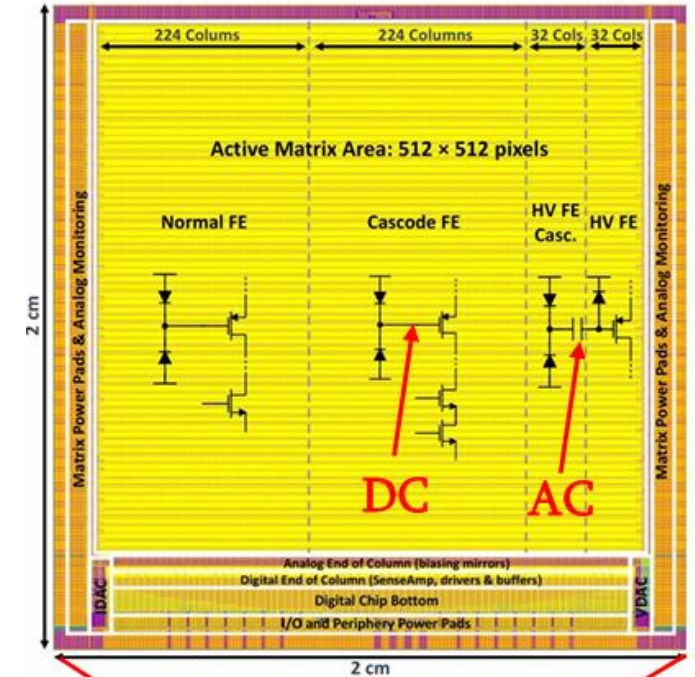


L6 Al-flex design update: High-Speed Trace Routing



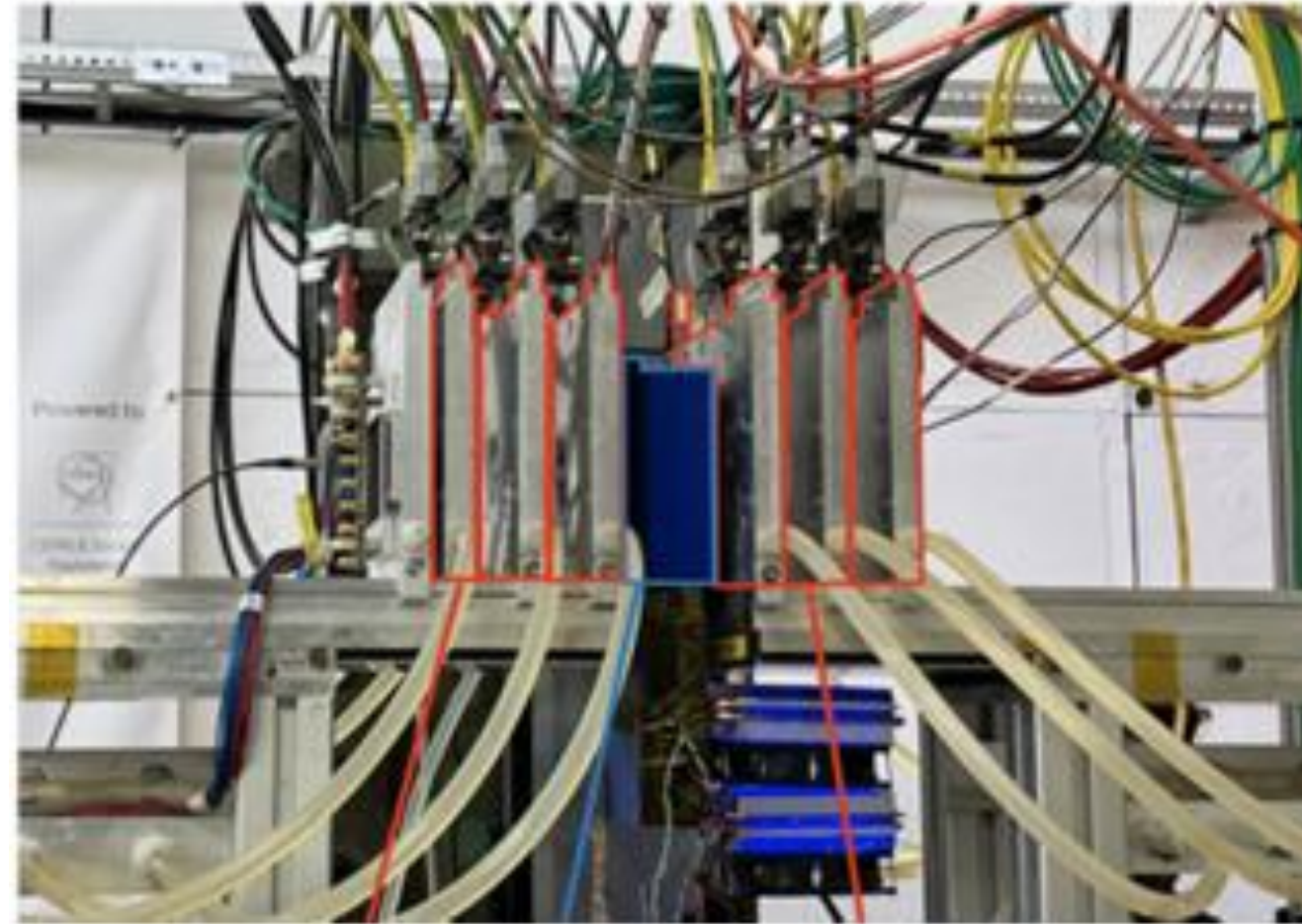
TJ-Monopix2 as a prototype

- TJ-Monopix2 is a Depleted Monolithic Active Pixel Sensor (DMAPS) developed for ATLAS ITk in the Tower 180 nm imaging process
- Matches main specifications for VTX upgrade:
 - Hit-rate capability >100 MHz per square centimeter
 - Timing resolution of 25 ns (VTX requirement: 50 ns)
- R&D chip with 4 front-end flavors
 - Different biasing mechanism and coupling schemes (DC or AC) between sensor and amplifier
- Square pixels with $33.04 \mu\text{m}$ pitch, large matrix (512×512 pixels $\Rightarrow 2 \times 2 \text{ cm}^2$)
- 7-bit Time-over-Threshold information
- Fast readout operated in triggerless mode
- DAQ system: BDAQ53, based on RD53 chip readout
- Radiation tolerance previously demonstrated at negative temperature; current tests aim to demonstrate radiation tolerance at room temperature



Test beam studies: TJ-Monopix2

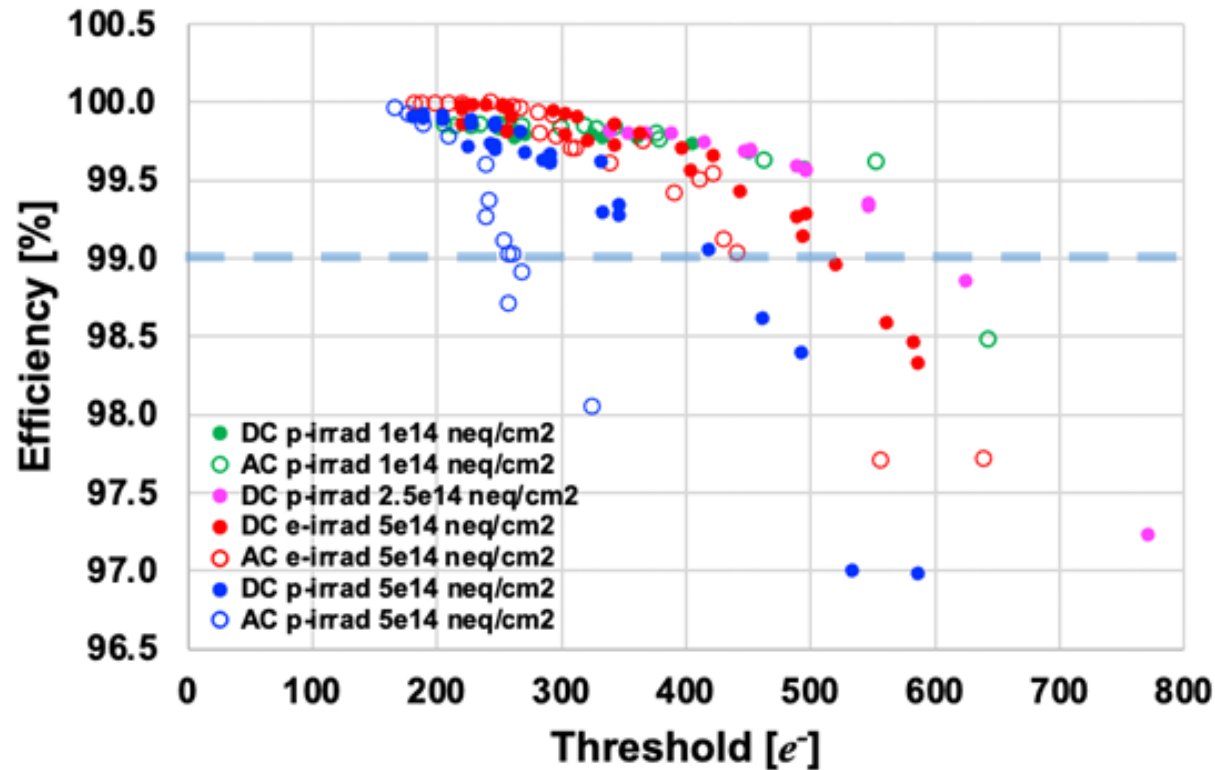
- Used a 4.2 GeV e^- beam, generated from the DESY II ring
- Telescope composed of 6 layers of MIMOSA26 (3 upstream and 3 downstream) and a Telepix sensor for timing measurements
- Used a dedicated cooling setup with a copper plate in contact with a Peltier cell to set the sensor temperature
 - Operating T_{NTC} between 10 and 50 °C
 - T_{NTC} is about 7 °C lower than the actual sensor temperature (T_{sensor})
 - Opening in the copper at the chip position



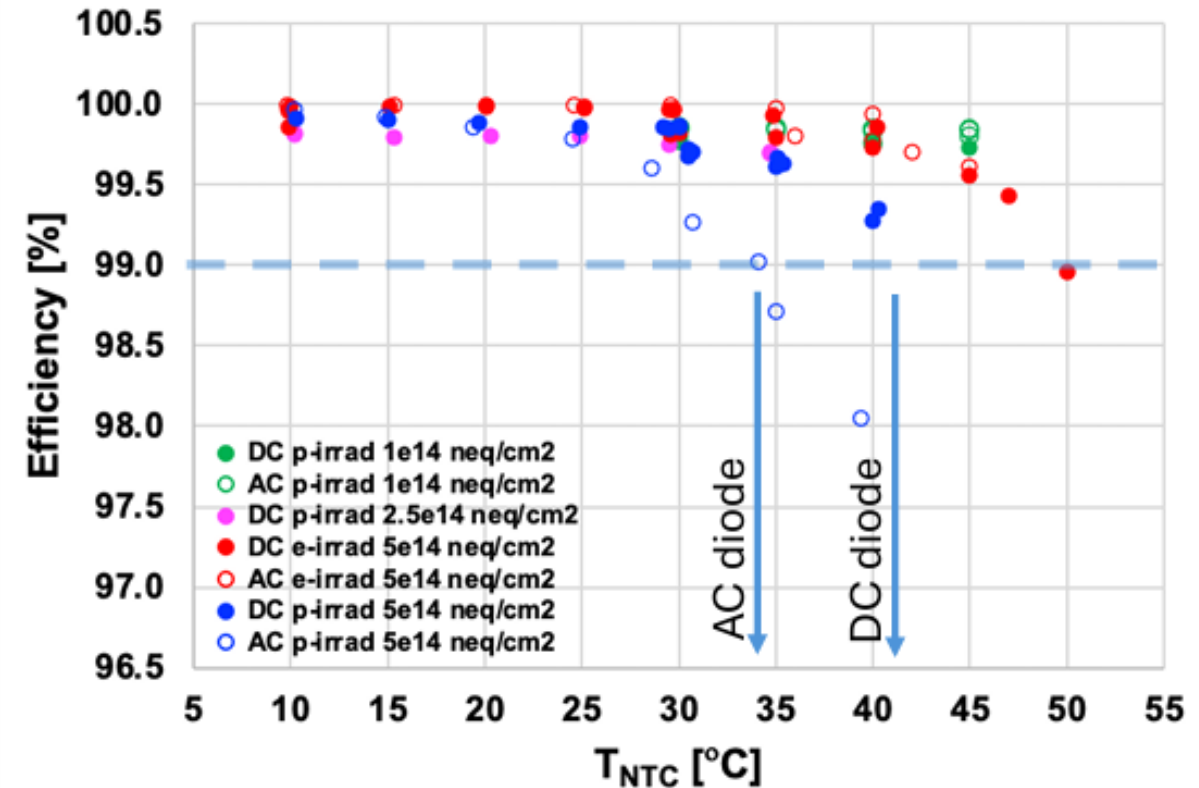
The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)

Test beam studies: TJ-Monopix2

Efficiency vs Threshold - Max bias



Efficiency vs T_{NTC} - Max bias

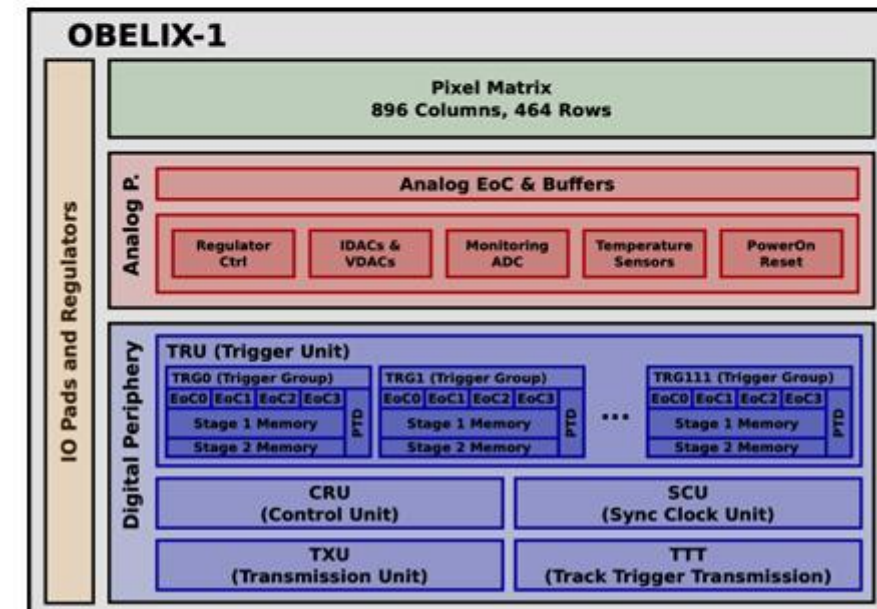
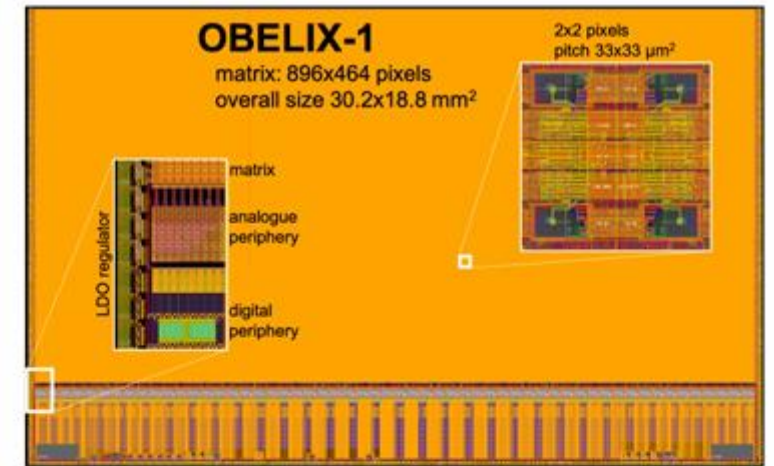


Key observations:

- Sensors irradiated with higher NIEL fluences show lower efficiency (as expected)
- DC coupled sensor performs better than the AC coupled
- AC efficiency < 99% at THR > 250 e^- (steep drop) / DC efficiency < 99% at THR > 400 e^-
- DC allows higher max operating temperature than AC sensor
- **Operating sensor temperature should stay below 40° C after irradiation to $5 \times 10^{14} n_{eq}/cm^2$**

Optimized Belle II pixel sensor

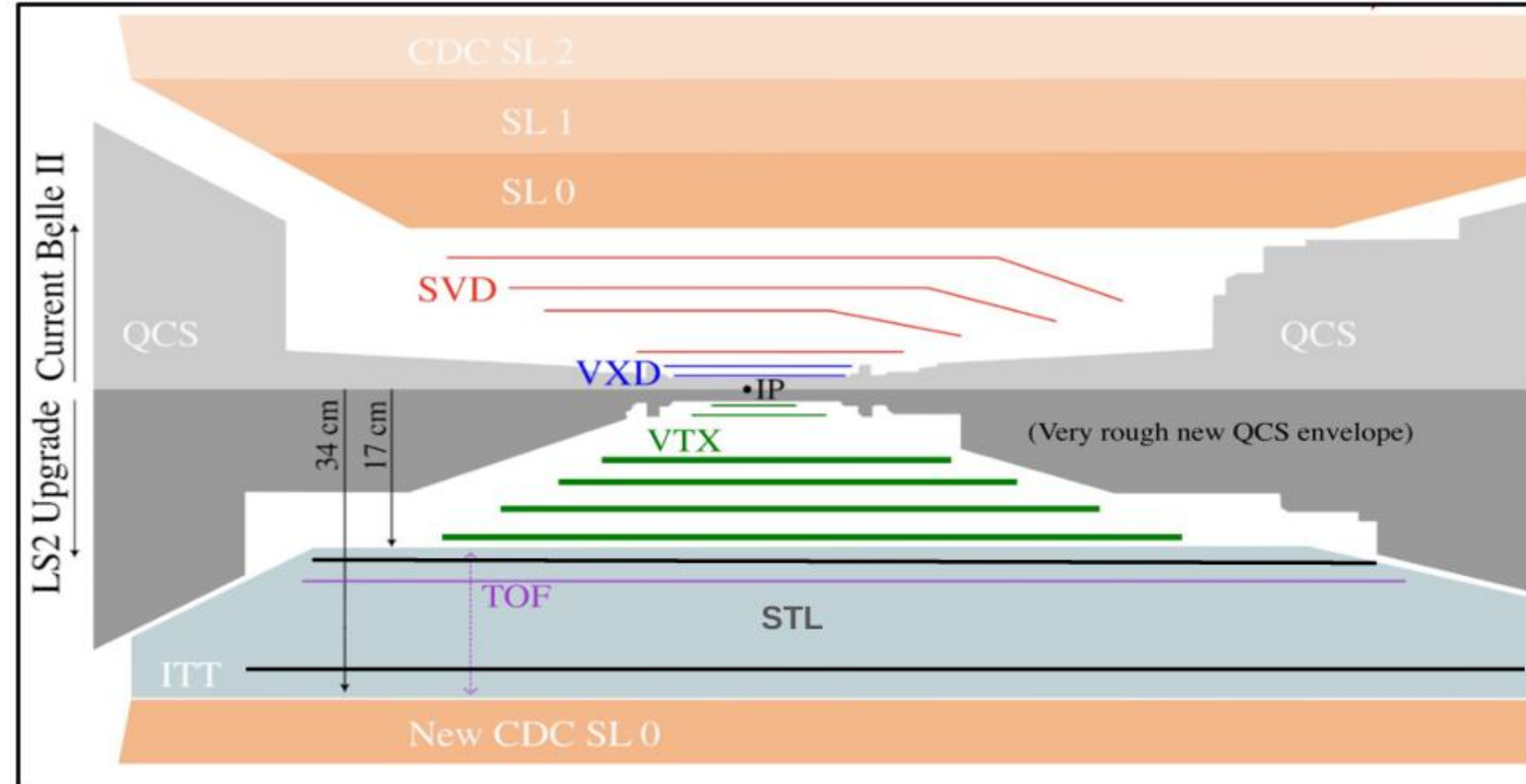
- OBELIX chip is being developed to fulfil the requirements of its application in Belle II vertex detector.
 - The chip will inherit the analog design and column readout architecture of the TJ-Monopix2
 - Will feature the DC-coupled cascade front-end.
- Specifications:
 - Chip size: 30 x 19 mm²
 - Pixel: 33 x 33 μm² / 464 rows, 896 columns
 - Time stamping: 50 to 100 ns
 - PTD: Fine time stamping ~5ns (for hit rate < 10 kHz/cm²)
 - Allows ~10 μs trigger latency at 30kHz
 - TTT: Low-latency trigger readout ~200 ns
 - Hit rates up to 120 MHz/cm²
 - **Submission plan: March 2026**



A new Inner Time Tracker region between VTX and CDC

(Conceptual layout – work in progress)

Under consideration



- A gap between the VTX and the new CDC (after removing the CDC inner layer) may leave tracks in this region uncovered
- Particularly impacts low-momentum tracks

Physics Goals:

- Improve tracking efficiency in the VTX-CDC transition region
- Provide additional pion-muon separation at low momentum region

Inner Timing Tracker (ITT): ongoing R&D options

- Fast Timing Layer (FTL): fast timing information for PID and background rejection
- Silicon Transition Layer (STL): precise silicon space points to ensure tracking continuity

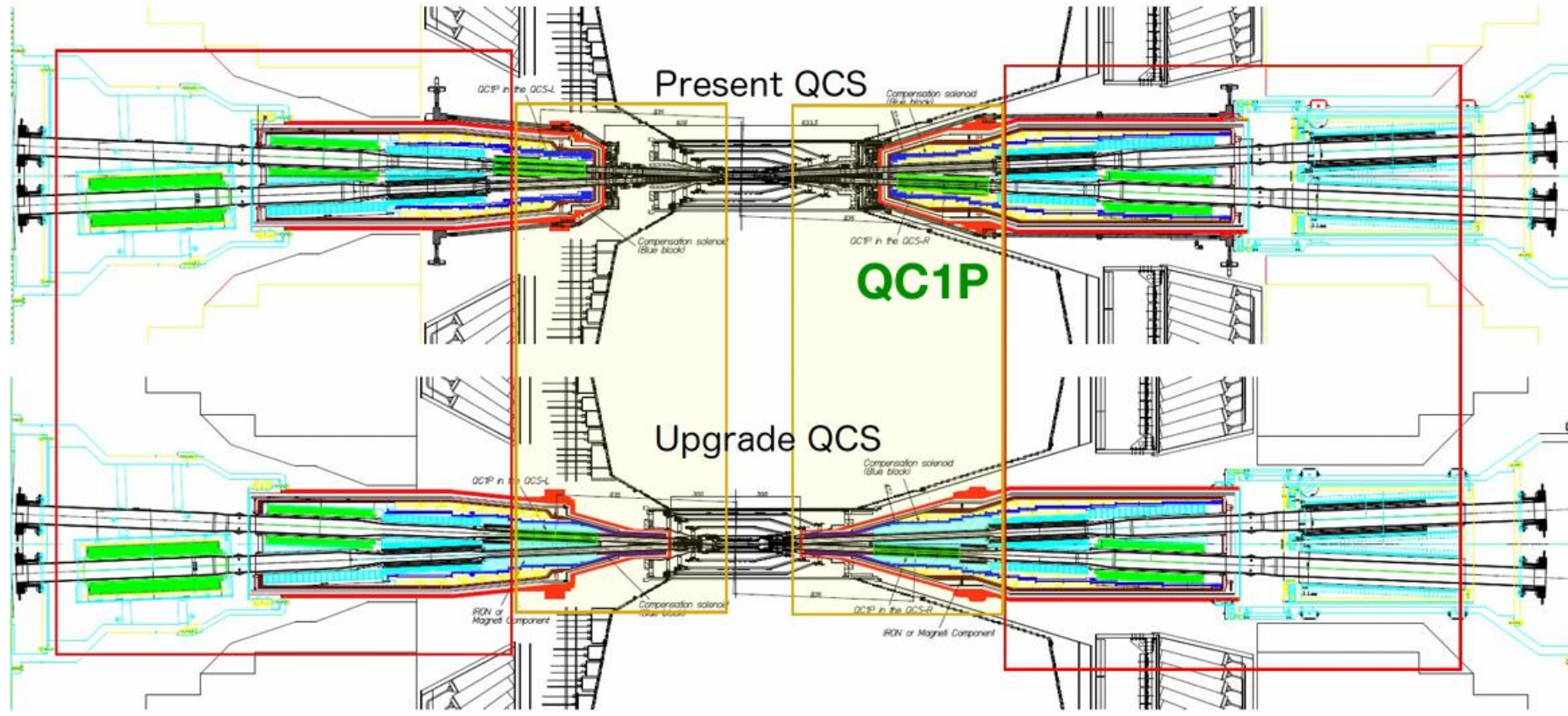
Summary

- The Belle II VTX upgrade is driven by high background occupancy, radiation damage, and need to operate safely at designed luminosity.
- The proposed DMAPS-based vertex detector meets the required Belle II performance.
 - iVTX: employs a self-supporting silicon ladder with redistribution-layer (RDL) routing and high thermal conductivity sheet for cooling.
 - oVTX: based on an omega-shaped carbon-fiber structure with Airex foam as core material.
- TJ-Monopix2 results strongly support the OBELIX design.
- OBELIX integrates multiple on-chip functionalities, including:
 - Trigger logic with $\sim 10 \mu\text{s}$ latency
 - High-precision timing circuitry
 - Fast data transmission for trigger contribution
- A global study of future Belle II tracking devices, including the VTX, a possibly modified drift chamber, and additional silicon sensors optimized for light tracking and fast timing for PID, is ongoing.

Thanks!

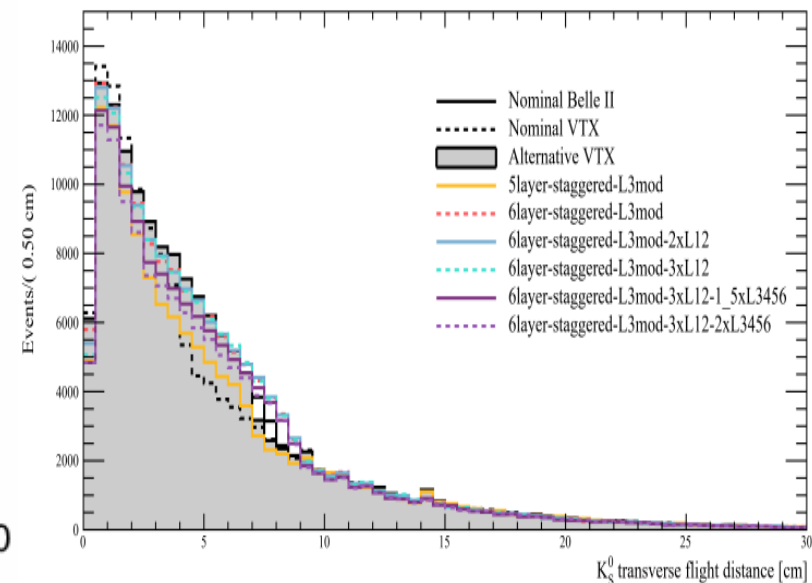
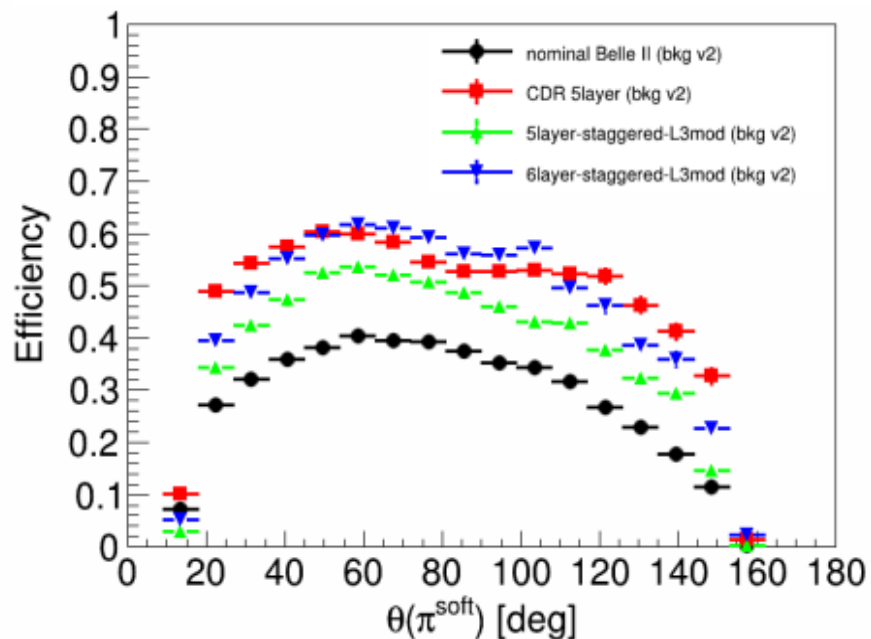
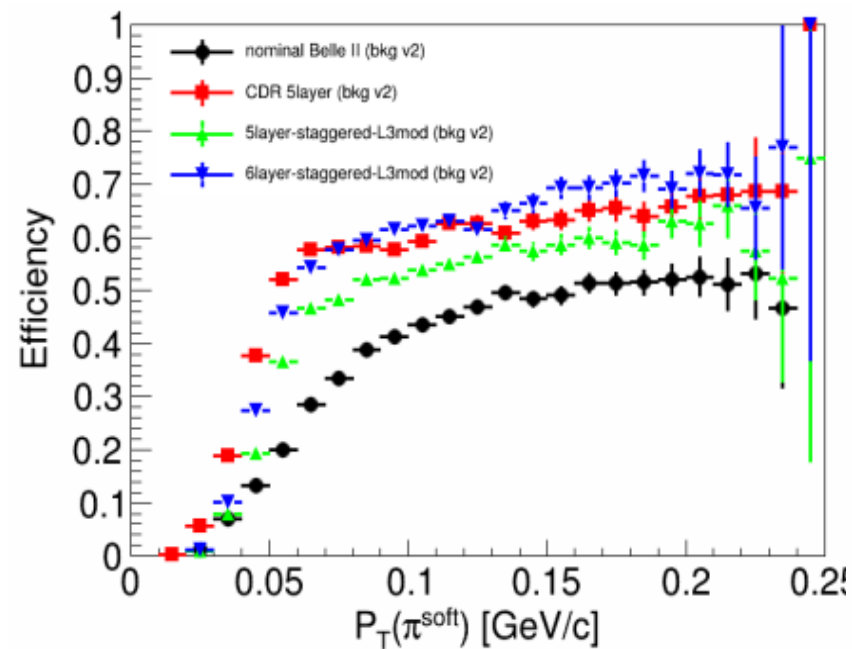
Back-up slide

SuperKEKB IR Upgrade



- A new QC1 Magnet
 - Move QC1P 100 mm closer to the IP
 - NbTi → Nb3Sn to support higher current
- Install a new compensation solenoid near the IP
- Minimize chromatic X-Y coupling between the IP and QC1

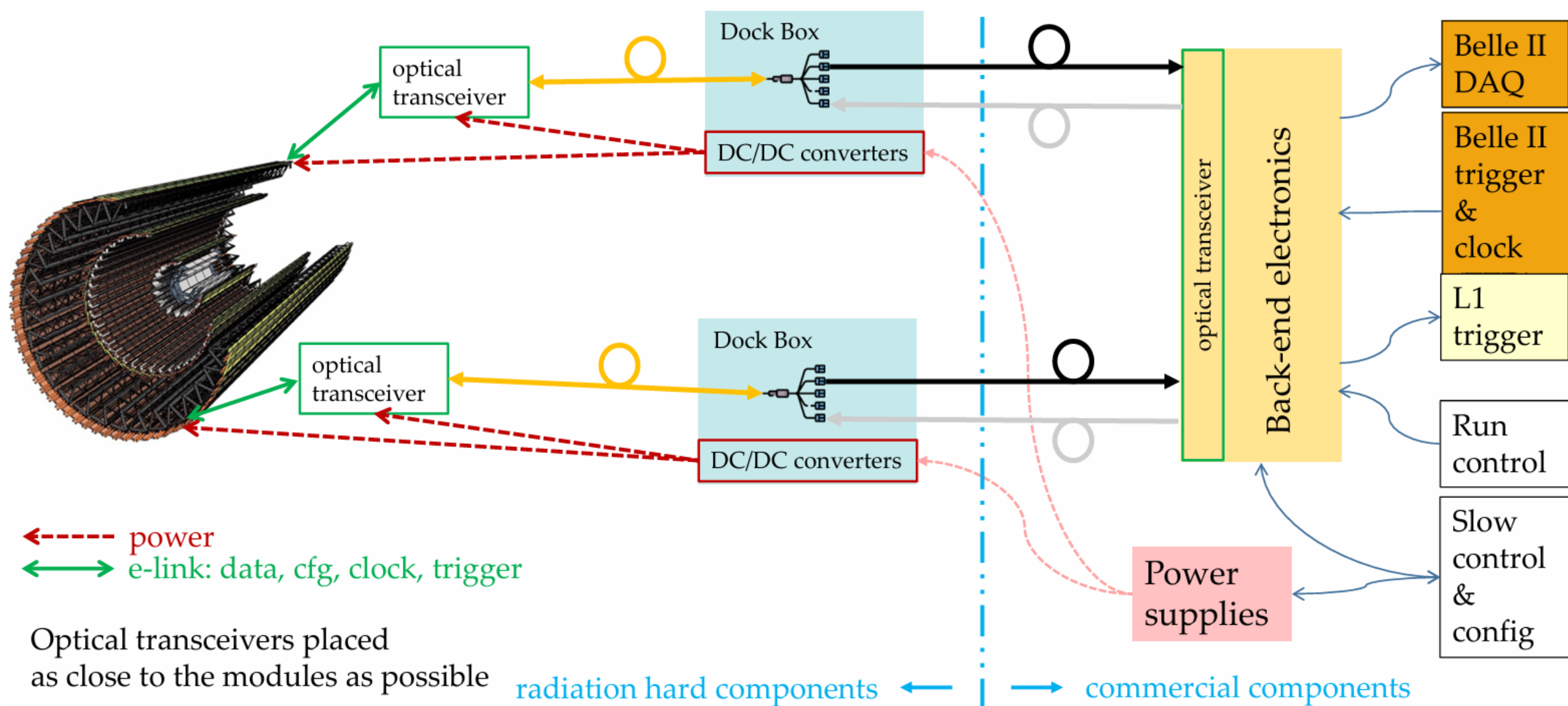
Physics performance with VTX upgrade



| | iVTX [% X_0] | iVTX [% X_0] |
|--------------------|-----------------|-----------------|
| Optimistic | 0.1 | 0.4 |
| Engineering design | 0.3 | 0.6 |
| Pessimistic | 0.3 | 0.8 |

| B_{sig} z vertex resolution [μm] | Bkg(v1) | Bkg(v2) | Bkg(v3) |
|--|---------|---------|---------|
| Belle II | 20.9 | 22.3 | 24.5 |
| Nominal VTX | 13.9 | 14.0 | 13.9 |
| Alternative VTX | 13.7 | 13.7 | 13.6 |
| 5-layers staggered | 16.7 | 16.1 | 16.4 |
| 6-layers optimistic | 16.1 | 16.1 | 16.1 |
| 6-layers engineering design | 19.0 | 19.0 | 19.0 |
| 6-layers pessimistic | 19.1 | 19.1 | 19.1 |

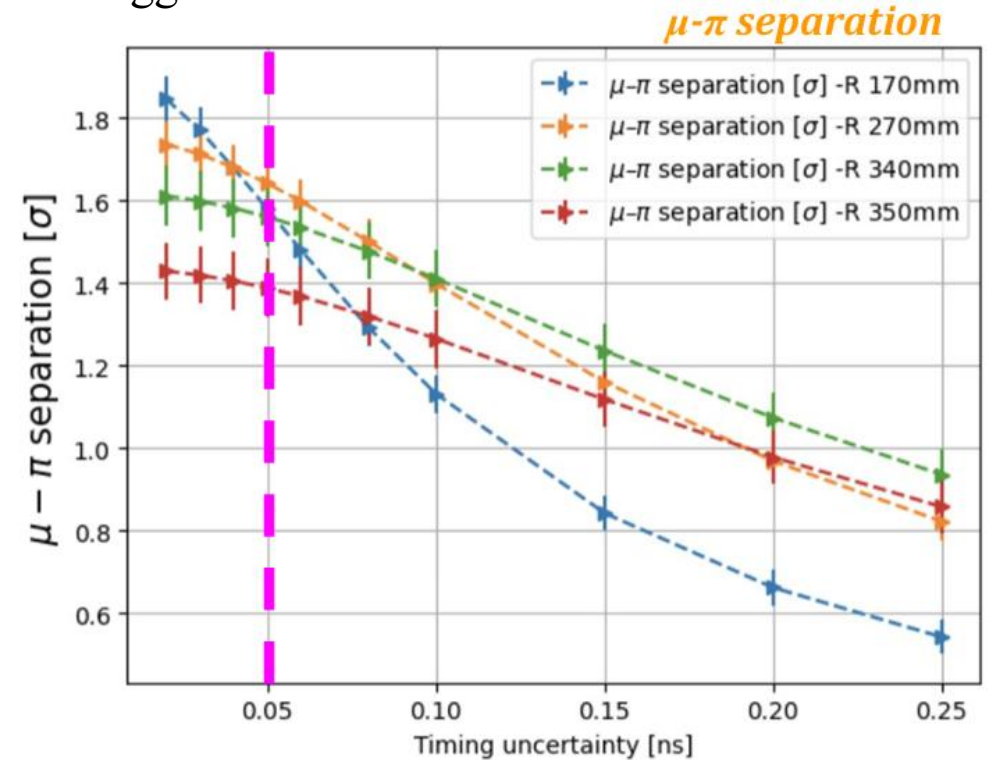
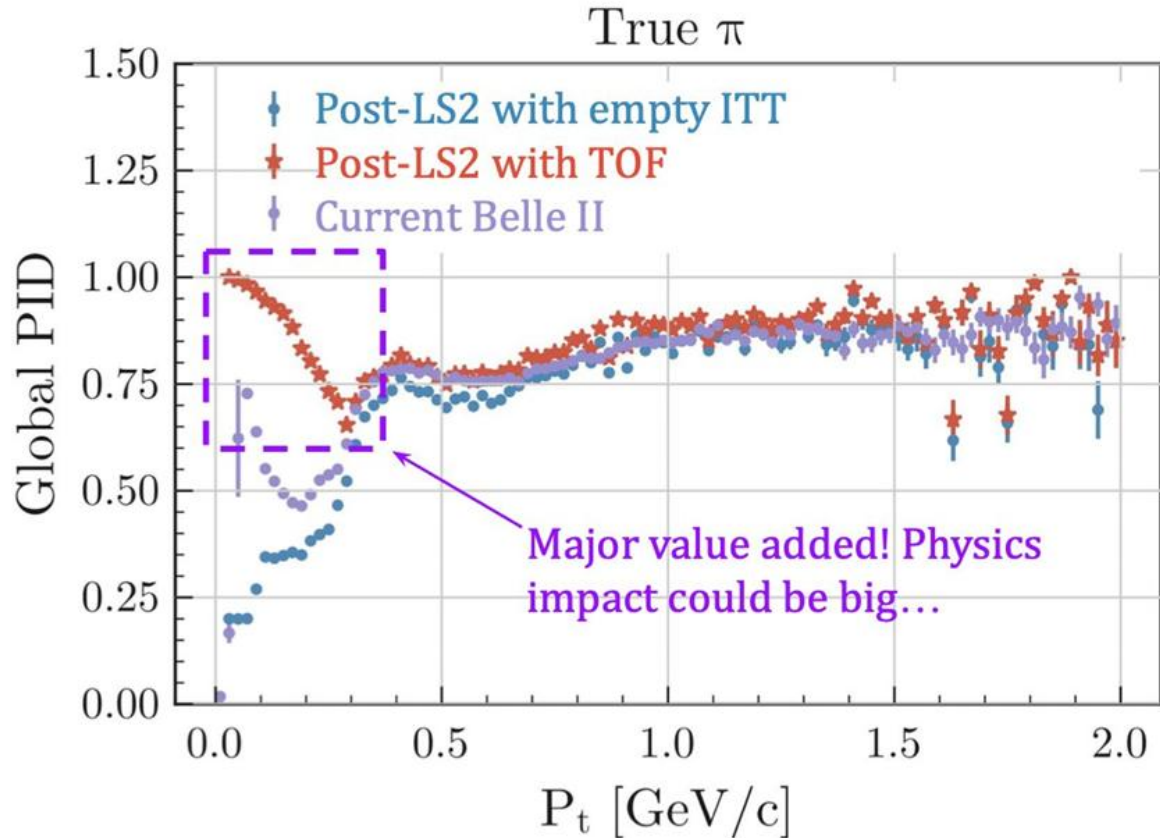
VTX Readout concept



A new Inner Time Tracker region between VTX and CDC

Preliminary studies have been done to understand the **potential benefits** and **requirements** to the actual technology:

- **Promising PID improvement:** TOF-based PID with 50ps timing resolution
- Further studies to be done to understand the contribution to tracking and trigger



Figures courtesy of [Yubo Han](#), FTCF 2025

Potential scenarios:

- TOF: LGAD is an attractive option for its timing performance and well-established technology
- Pure tracking layer