

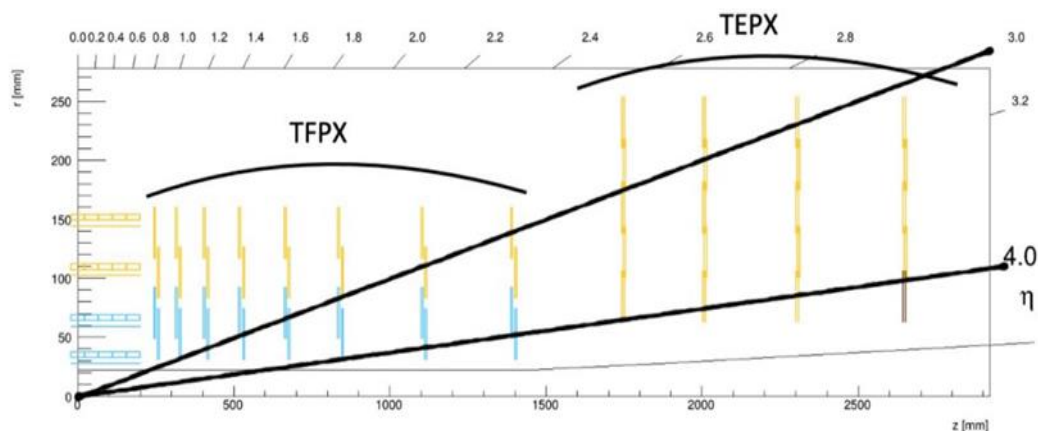
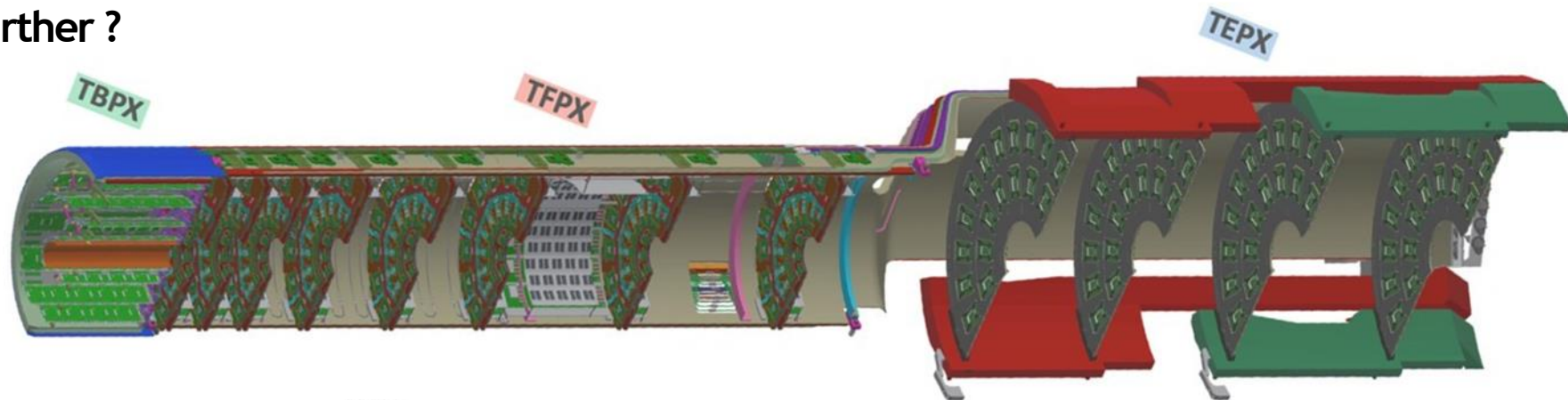
PSI Center for Neutron and
Muon Sciences

LIGHT01: A prototype LGAD pixel readout ASIC with ps timing resolution in 28 nm technology

Abderrahmane GHIMOUZ, On behalf of the HEP group
TIPP 2026, 05 Feb 2026

Need for timing

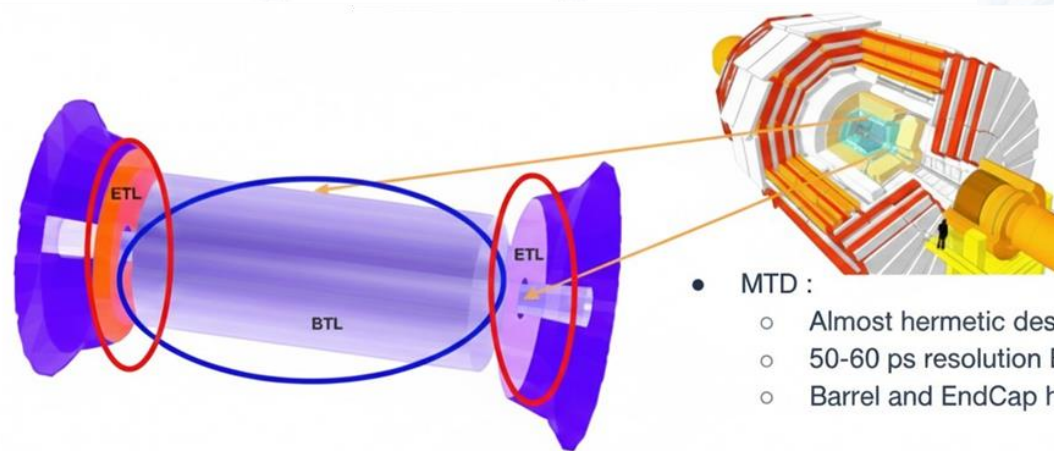
How to improve further ?



Credit : Dr. Wolfram Erdmann

- CMS 'Phase 2' timing covers region up $|\eta| \leq 3$

- Possible extension $|\eta| \approx 4$ in future upgrade replacing 1 or 2 TEPX pixel disks with LGAD pixels



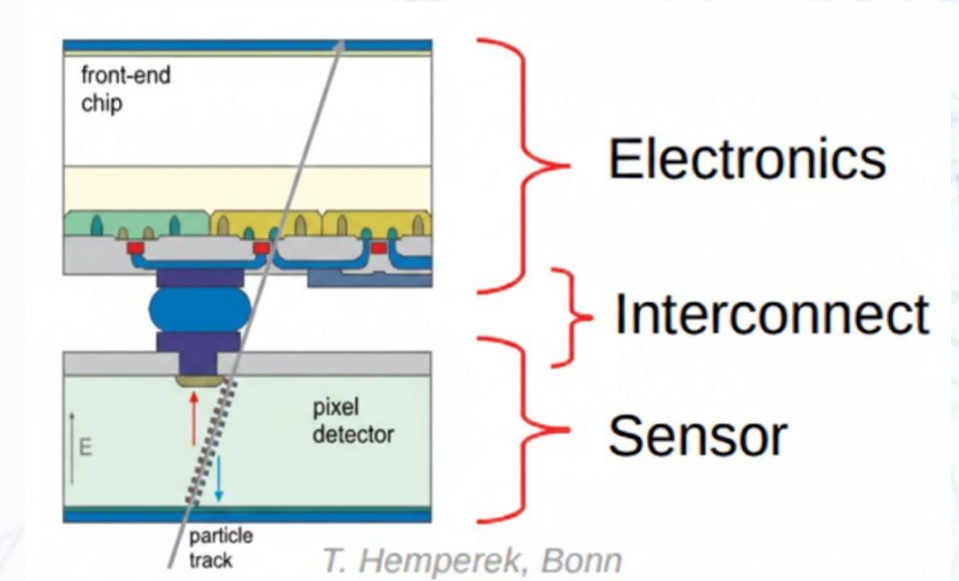
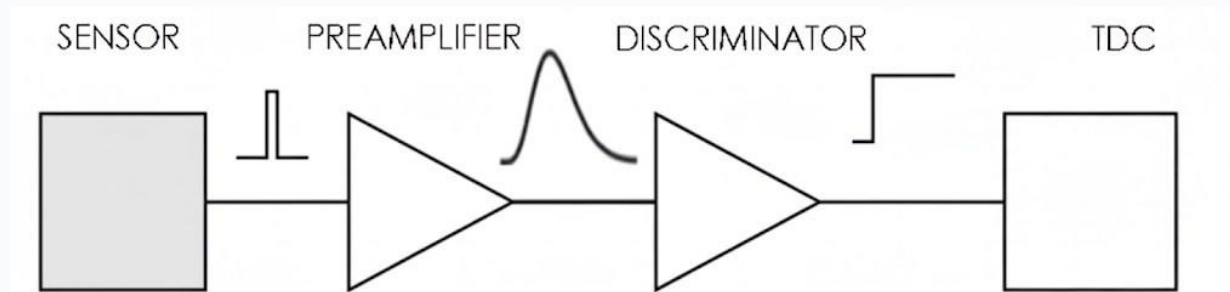
- **Barrel Timing Layer - BTL :**
 - Sensors: LYSO+SiPM
 - Inner radius: 1148 mm - 40
 - Length: ± 2.6 m
 - Fluence at $3000 \text{ fb}^{-1} \sim 1.7 \times 10^{14} n_{\text{eq}}/\text{cm}^2$
- **EndCap Timing Layer - ETL :**
 - Sensors: LGAD
 - Radius: $315 \text{ mm} < r < 1200 \text{ mm}$
 - z-position 3.0 m - 45 mm thick
 - Fluence at $3000 \text{ fb}^{-1} \sim 1.6 \times 10^{15} n_{\text{eq}}/\text{cm}^2$
- **MTD :**
 - Almost hermetic design, $|\eta| < 3.0$
 - 50-60 ps resolution EoL
 - Barrel and EndCap have different needs

Goal



To **design** a readout **ASIC** targeting a future **CMS** upgrade. It should be capable of operating with **pixel** detectors based on **LGAD** technology. It is designed in a **28 nm CMOS** technology, for **timing** measurements.

Timing equation



Time **resolution** of a timing measurement Front End Electronics (FEE)

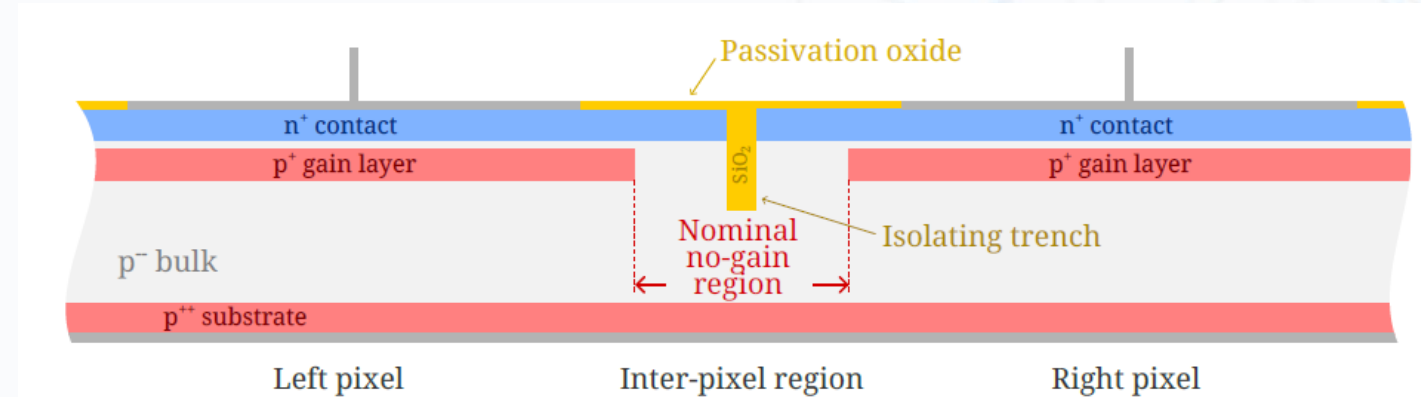
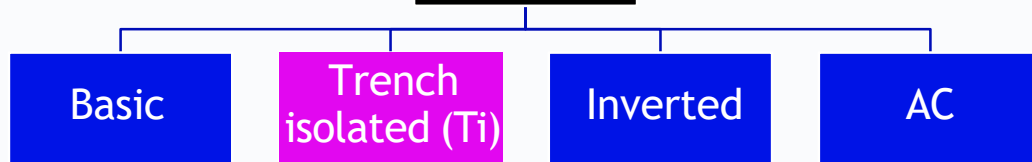
$$\sigma_t^2 = \underbrace{\sigma_{\text{Landau}}^2 + \sigma_{\text{Distortion}}^2}_{\text{To understand (characterization)}} + \underbrace{\sigma_{\text{Timewalk}}^2 + \sigma_{\text{TDC}}^2 + \sigma_{\text{Jitter}}^2}_{\text{To model and optimize (FEE architecture)}}$$

To understand (characterization)

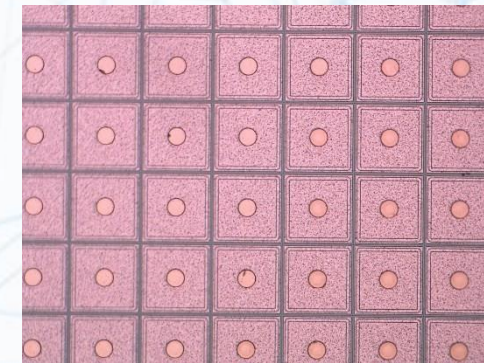
To model and optimize (FEE architecture)

Type of LGAD sensors : Ti-LGAD

Types of LGAD



Credit : Matias Senger



FBK@ AIDAInnova (DRD3)

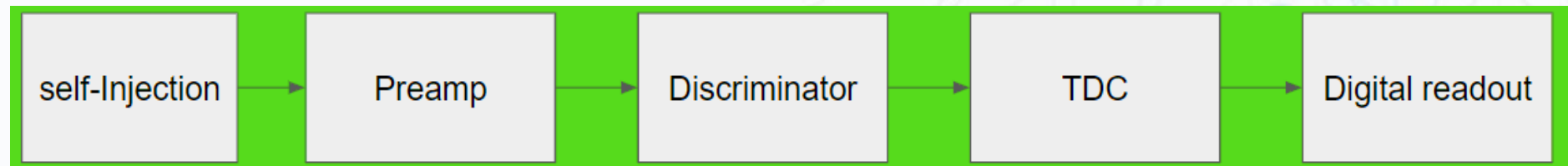
- Sensor configuration: 30x30 pixel array
- Pixel dimensions: 100 x 100 μm^2 $\rightarrow C_{det} \sim 0.12$ to 0.2 pF

Collaboration with the university of Zurich



System requirement

Property	Value
Pixel size	100 x 100 μm^2
Input capacitance	~ 0.2 pF (including parasitic)
Time res RMS	30 ps
Max dead time	< 250 ns
Total power density	1 W/cm²
Threshold level	< 2000 e⁻
Dynamic range (Q)	Equivalent 2000 e ⁻ to 150 Ke ⁻
Max hit rate per pixel	50 KHz



$$\sigma = \sqrt{20^2 + 5^2 + 20^2 + 10^2}$$

For a $\sigma \sim 30ps$ @MIP :

- 20ps : the jitter of the sensor*
 - 5ps : the clock jitter and the remaining disturbances
 - 20ps : the jitter of the FE
 - 10ps : the resolution of TDC
- } **Budget**

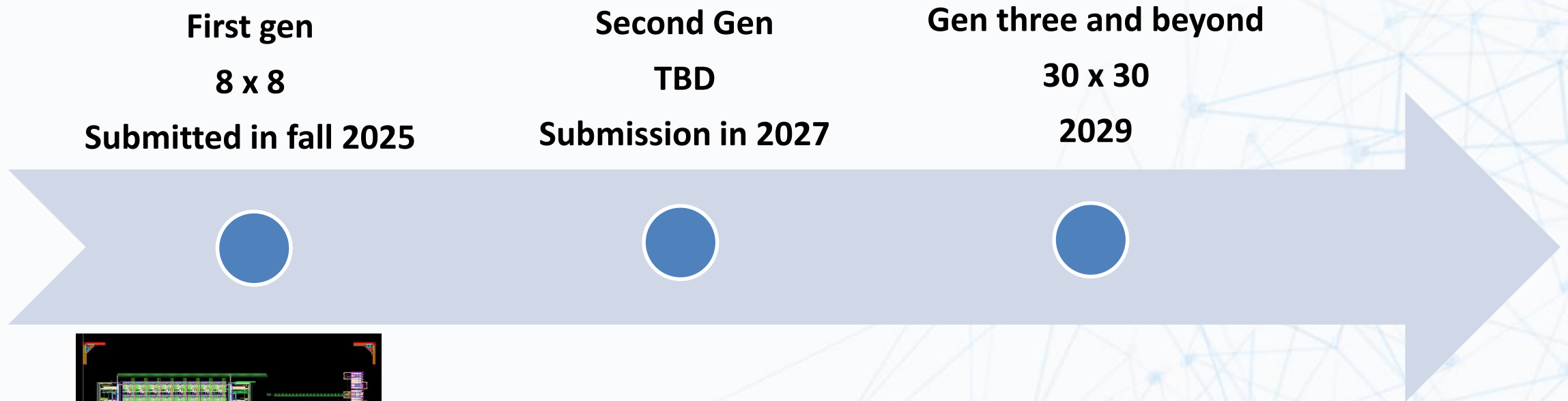
Specs of the first gen ASIC: LIGHT01



L_{GAD based} **I**_{ntegrated} **G**_{ranular} **H**_{ybrid} **T**_{iming} ASIC

- **64 Channels in 8x8 Pixel Array**
 - Different preamplifier topologies, optimized for minimum timing jitter
 - Per-pixel TDC
 - Integrated calibration system : TOT, RO frequency
 - Standalone test structures for critical blocks
 - SPI for programming and readout
 - Zero suppression readout
 - Use of specific IPs from the CERN 28nm forum library : Rad-Hard PADs, SLVS Drivers.
- **Bump-Bonding to Ti-LGAD Sensor**

Details about the ASIC (Future plan)



Demonstrator

- Scaling study
- Architectural refinement
- System Integration
- Experiment driven

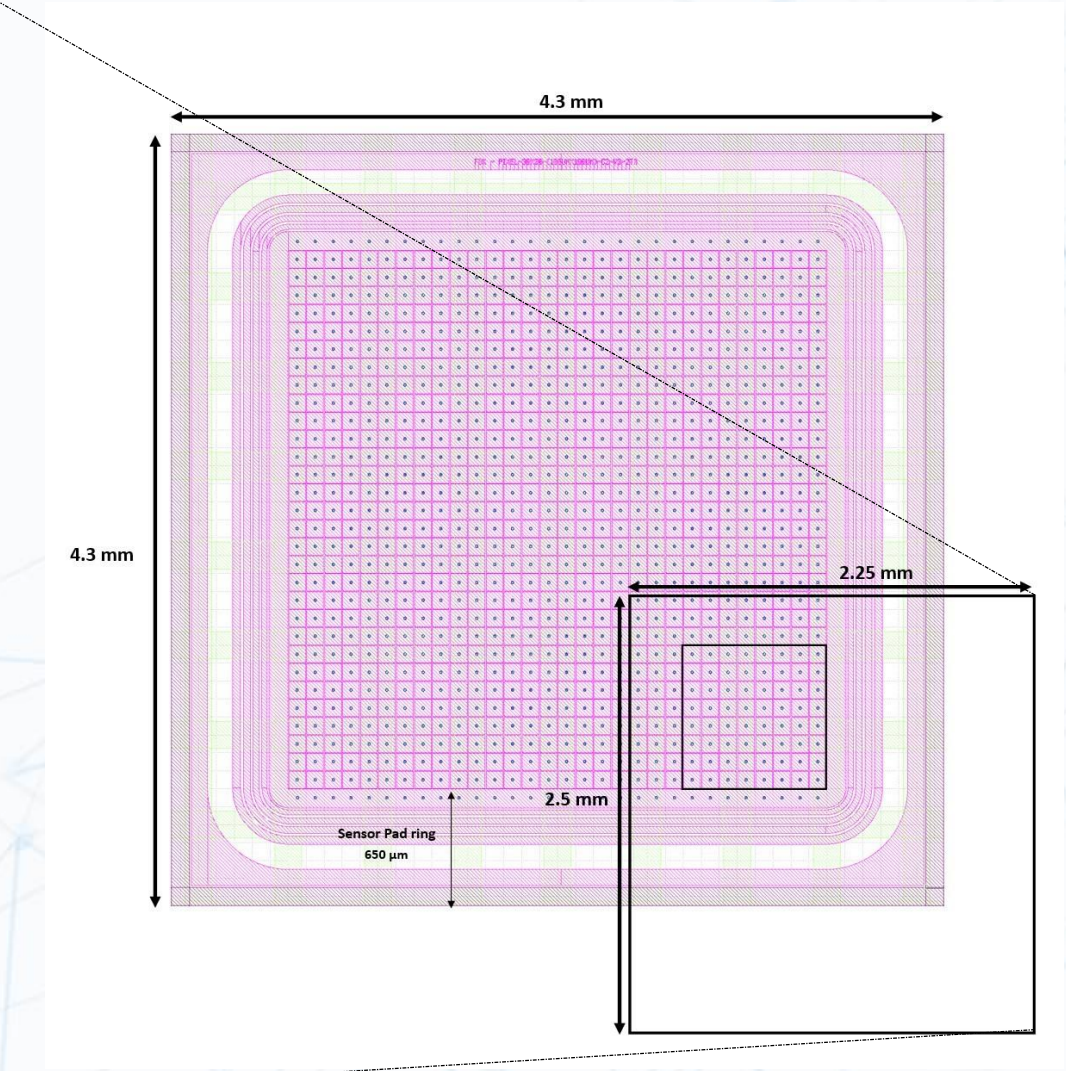
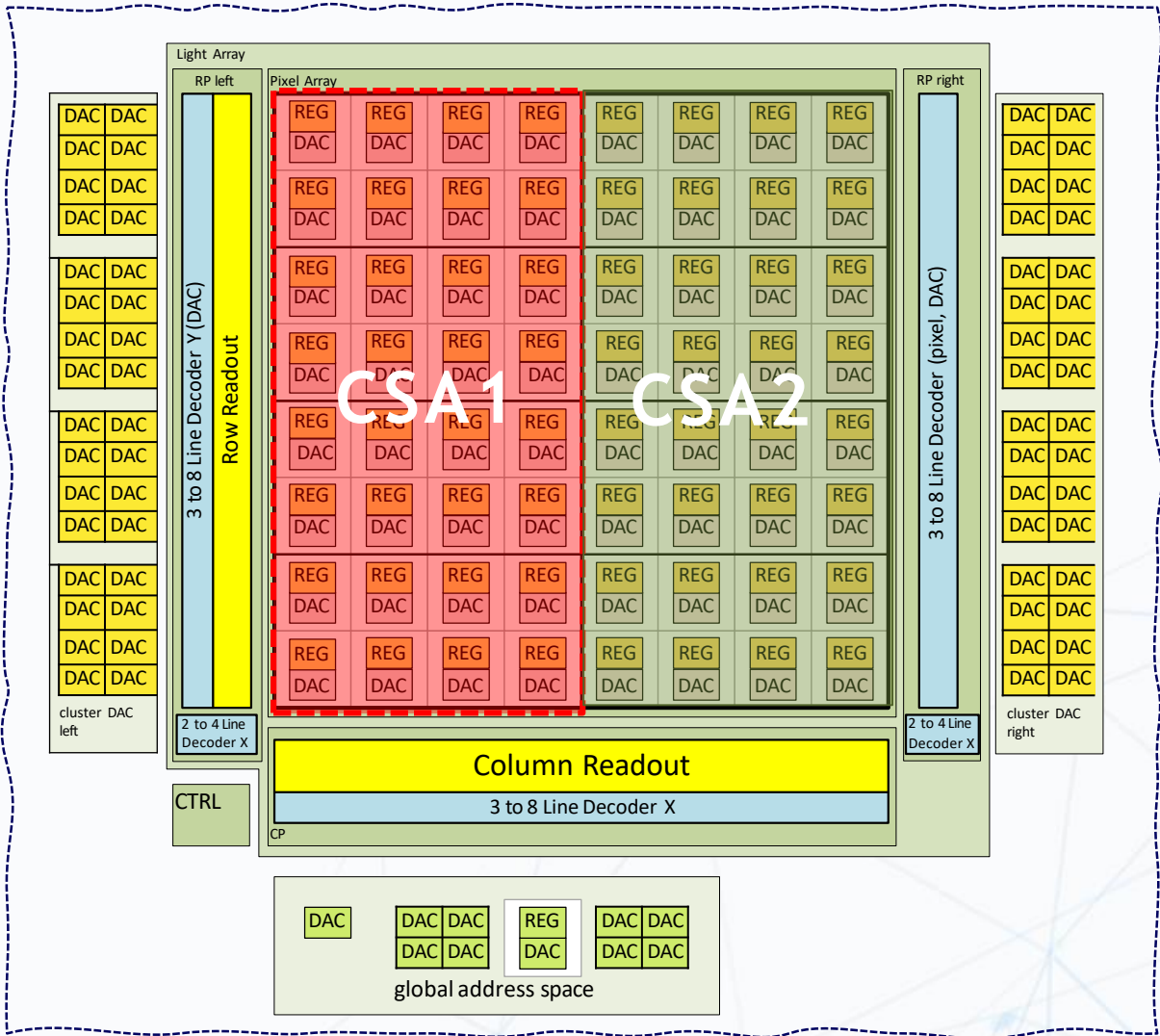


Join the collaboration !

Details about the first gen ASIC: LIGHT01

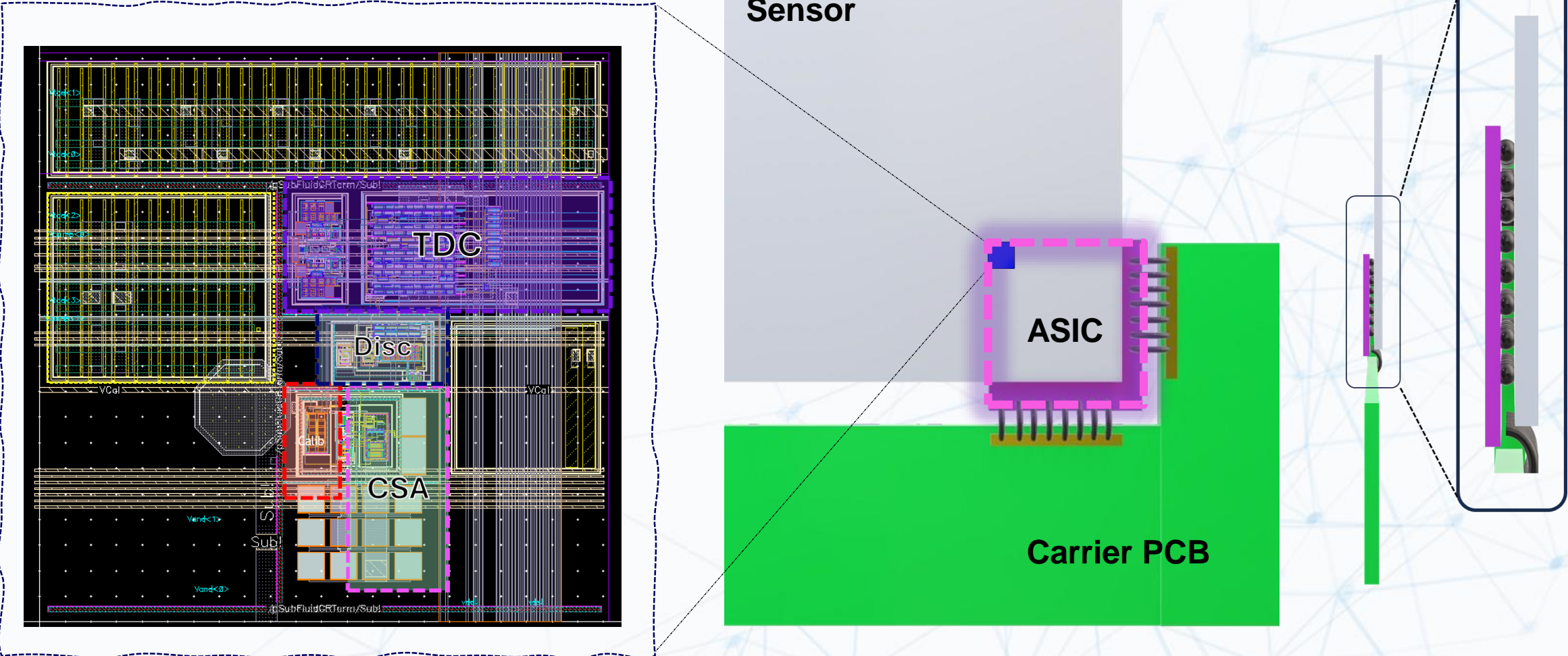


Structure



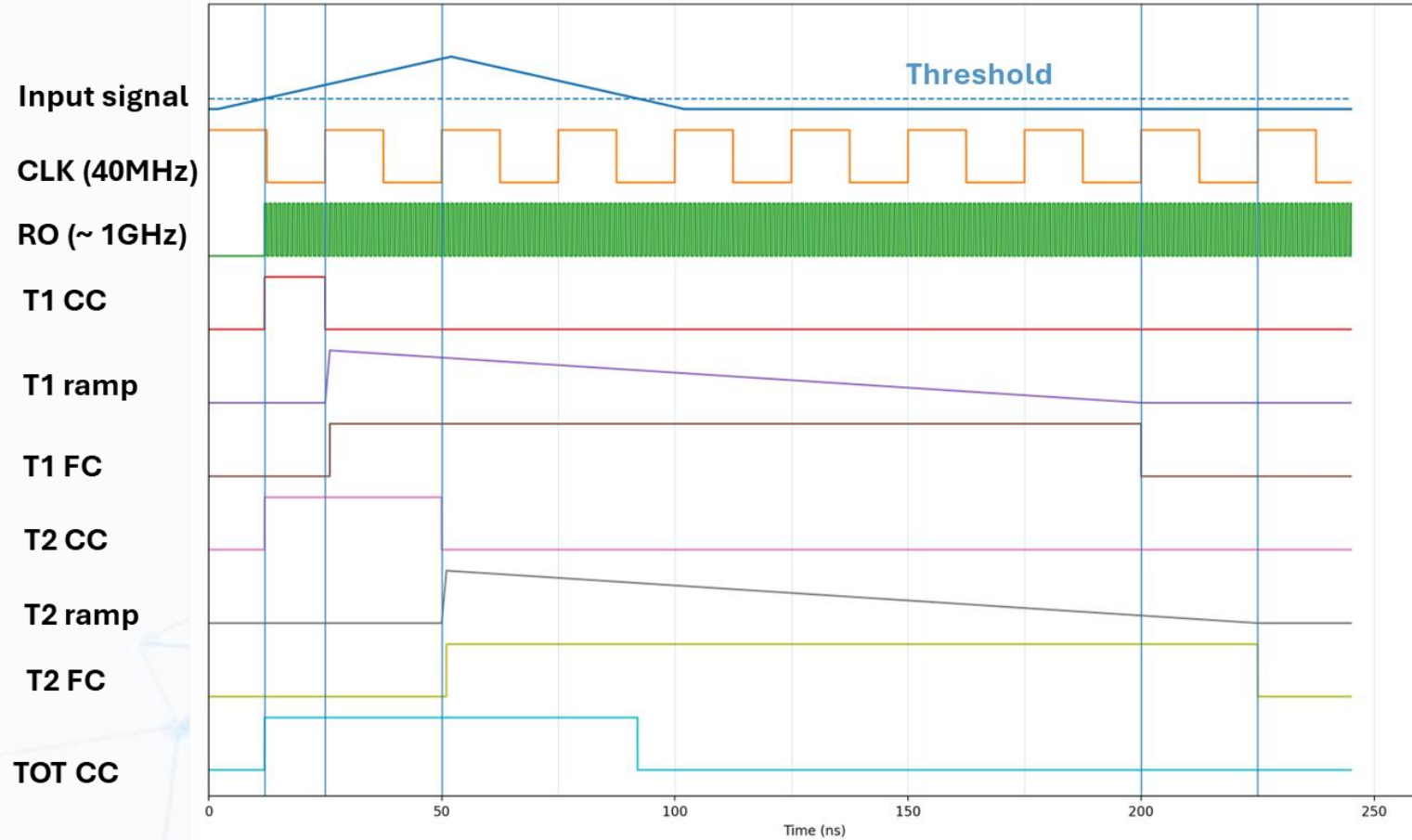
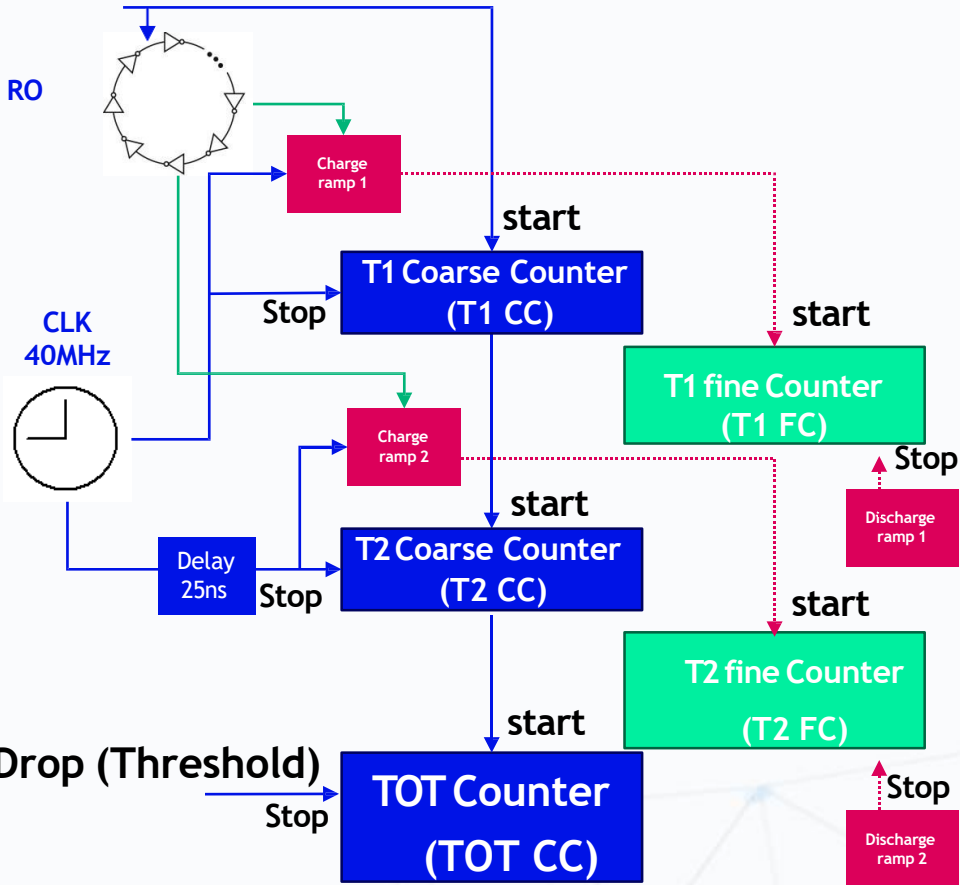
Details about the first gen ASIC: LIGHT01

Integration



TDC details

Hit (Threshold)



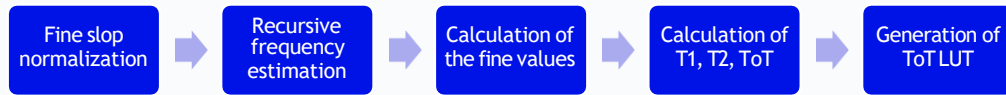
All counters are 8-bit

Estimated performance (Post-layout sims)

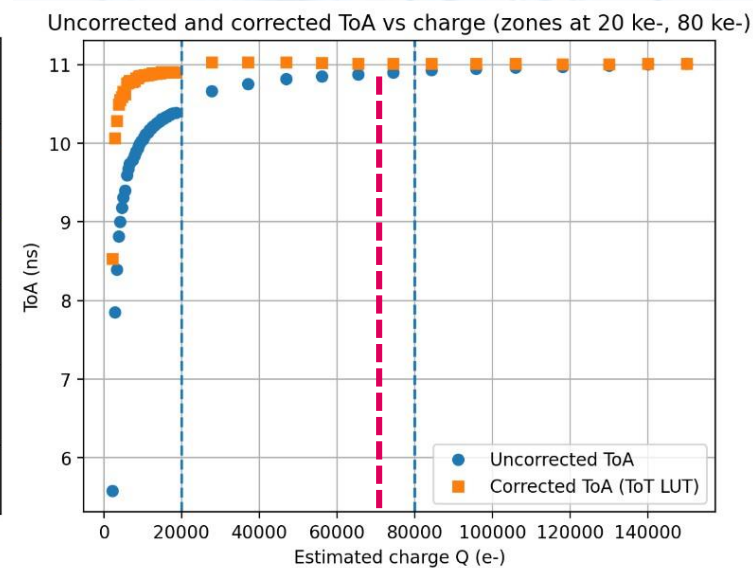
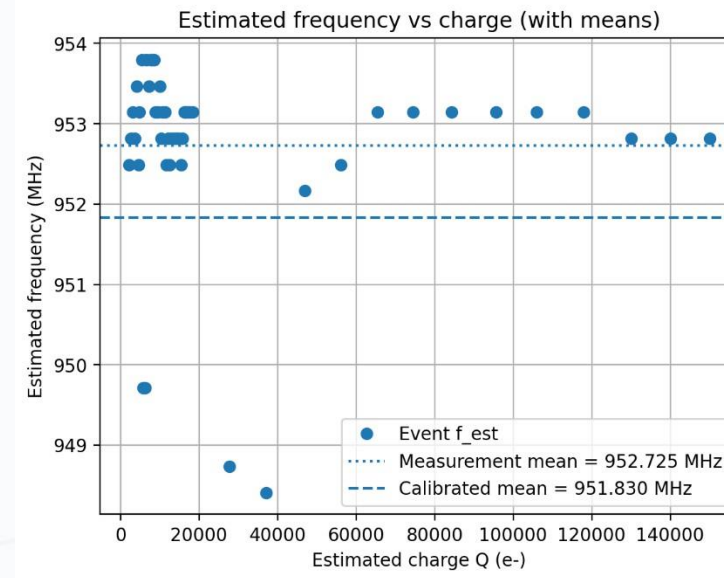
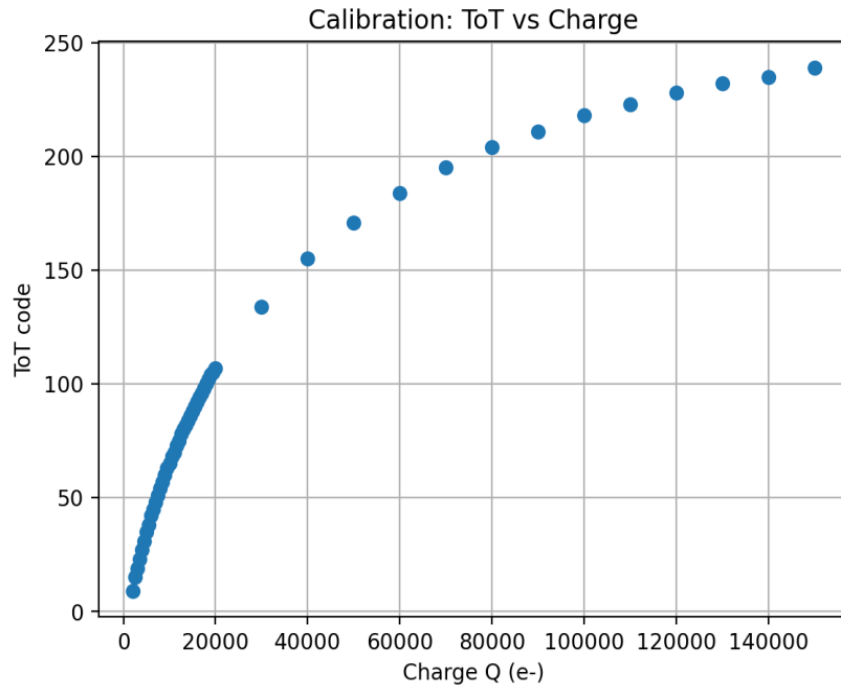
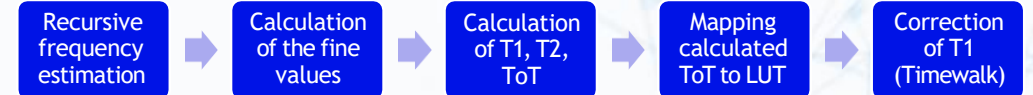


ToT correction

Calibration



Correction



MIP $\approx 70 Ke$

Fine LSB $\approx 8.57 ps$ \longrightarrow $\sigma_{TDC} \approx 2.5 ps$ $\sigma_{TOT correction} \approx 7.58 ps$

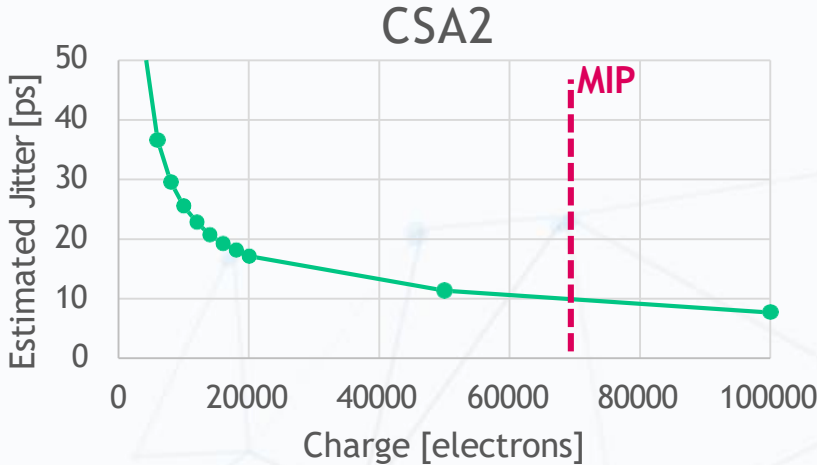
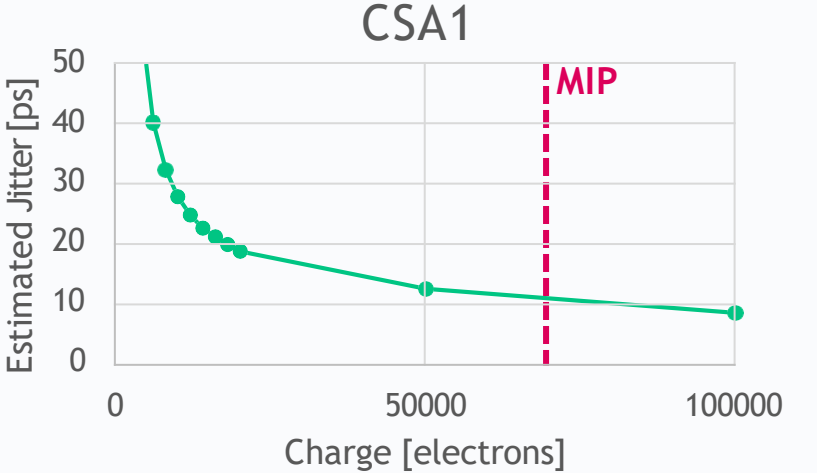
$\sigma_{TDC_{eff}} \approx 8 ps$

11

Estimated performance (Post-layout sims)



MIP $\approx 70 Ke$

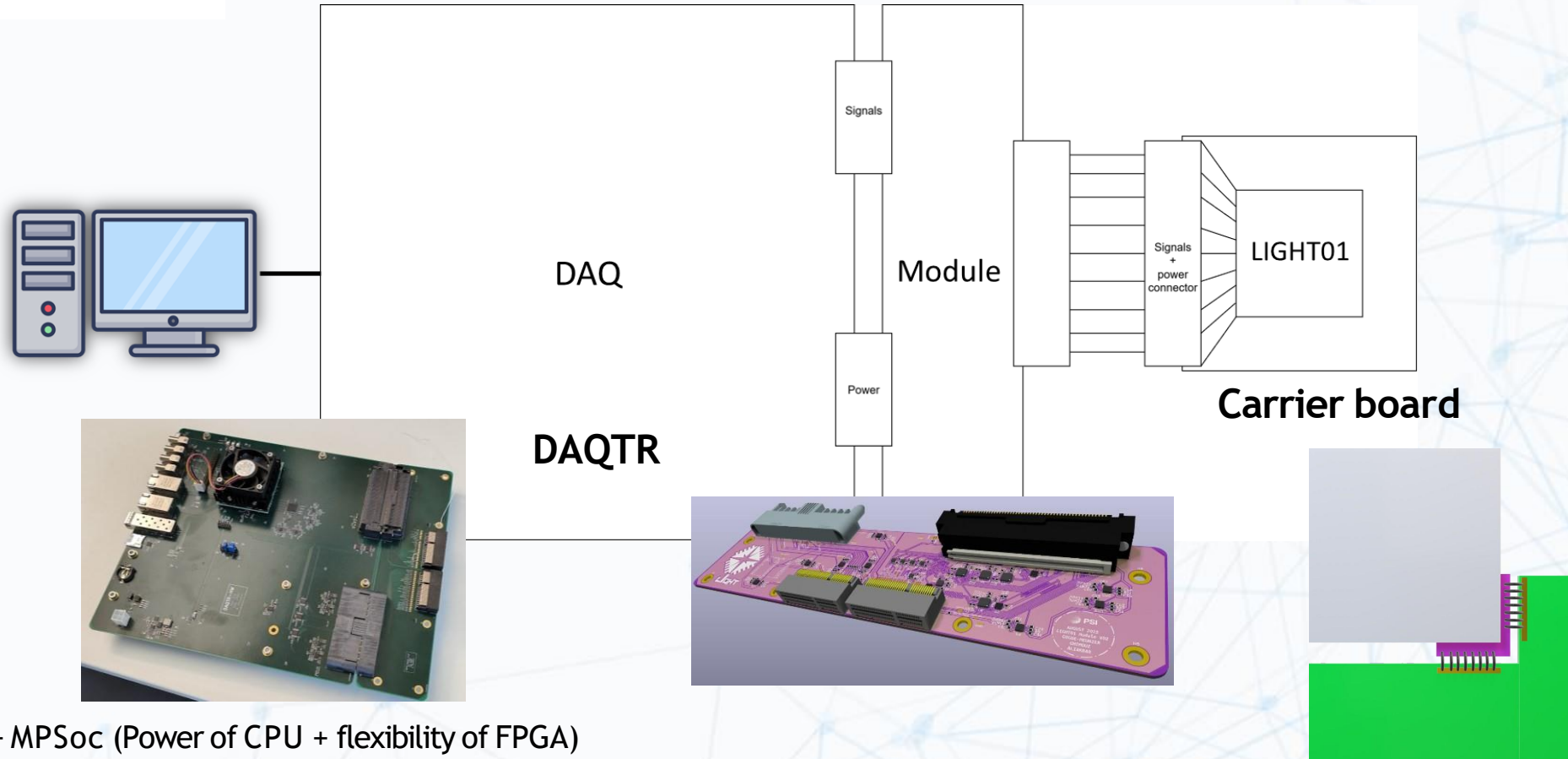
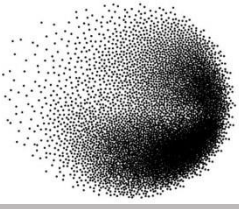


Results of the preliminary post-layout simulations (around the MIP):

- 20ps : the jitter of the sensor
- 5ps : the clock jitter and the remaining disturbances
- ~ 10 ps : the jitter of FEE
- ~11 ps : the resolution of the TDC

$$\sigma = \sqrt{20^2 + 5^2 + 10^2 + 8^2}$$

$\sigma \approx 24.3 ps < 30 ps$



- Zynq UltraScale+ MPSoc (Power of CPU + flexibility of FPGA)
- Provide multiple power domains
- Supports SPI protocol
- Supports Ethernet and Optical fibers
- Bank of DACs, ADCs and LDOs
- Variable clocks reaching 400 MHz

- Fully controllable delay line
- Covers the full 25ns window with 10 ps (4 ps after tuning) steps
- Adaptation of signals from/to DAQ
- Local LDOs for critical components

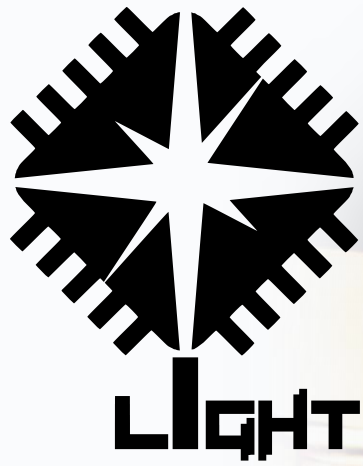
Conclusion



- **First generation of timing ASICs : LIGHT01** → Submitted in fall 2025.
- **The preliminary post-layout simulation results** indicates promising results.
- **ASIC/Sensor integration** → Bump bonding procedure is under development.
- **Test strategy** → New versatile DAQ board + custom module board for timing measurement was fabricated. Firmware development is progressing.

- **This project** carried out in collaboration between PSI, UZH, CERN 28nm Community and CERN DRD3/7 → Looking for more collaborators.

All we have to decide is what to do with the time that is given us.



TIPP 2026 International Conference on Technology
and Instrumentation in Particle Physics



Thank you
Questions are welcome

On the behalf of the HEP group

ABDERRAHMANE GHIMOUZ

5th Feb. 2026

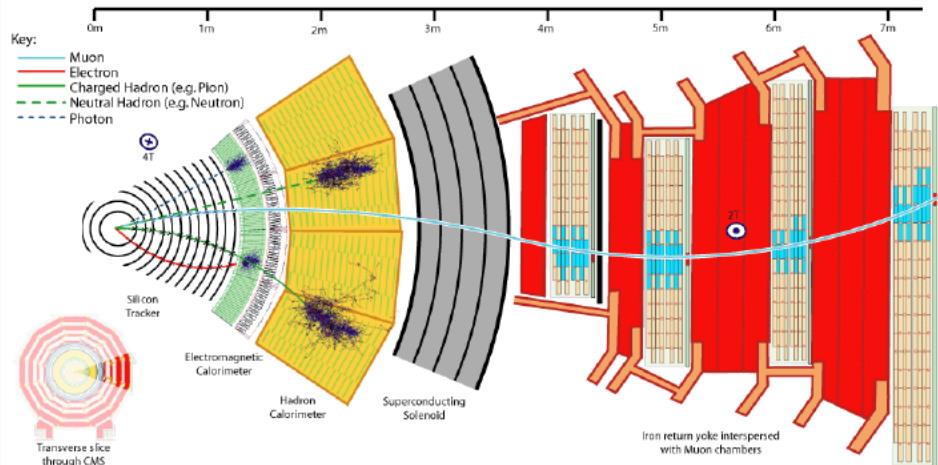


Join the collaboration !

ANNEXE

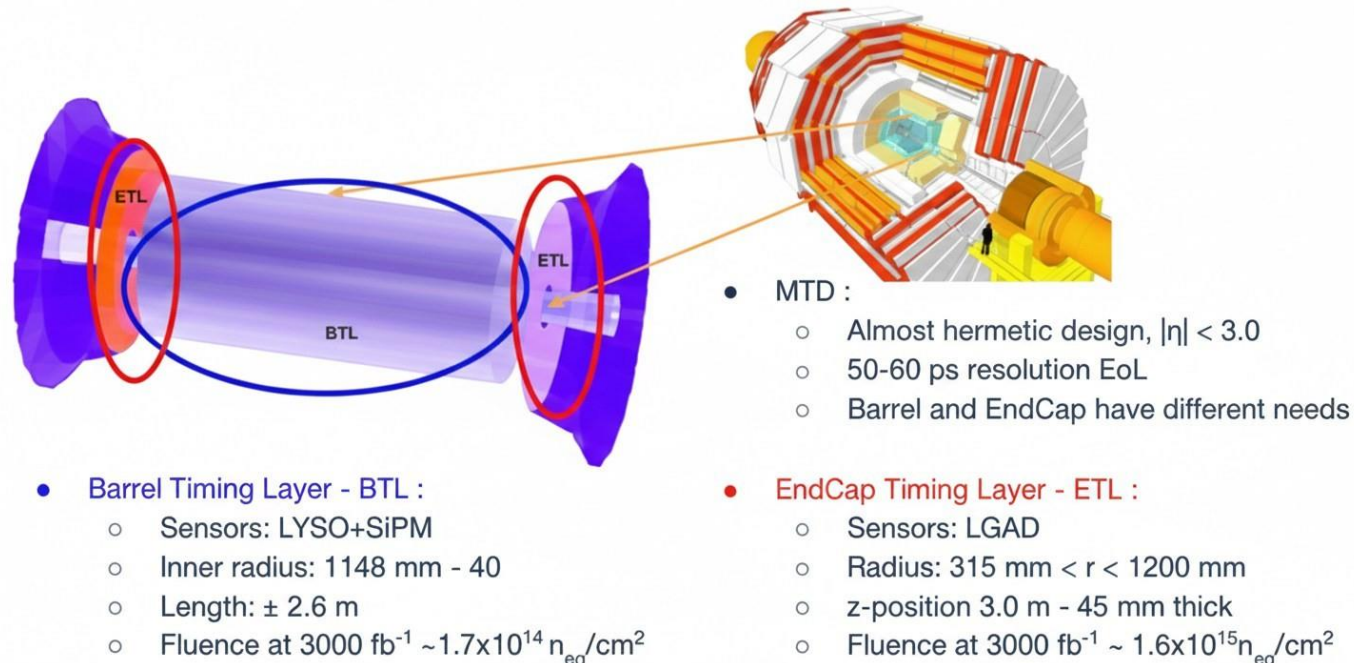
Need for timing

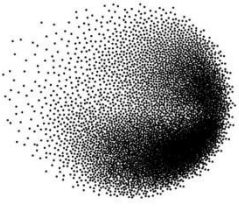
Current state



The need for timing measurement with the CMS detector for the HL-LHC upgrade:

- **Pile-Up Mitigation:** achieves 30-40 picoseconds resolution to separate up to 200 overlapping collisions.
- **Particle Identification:** utilizes precise timing to distinguish particles with speed differences as small as 0.1%.
- **New Physics Sensitivity:** improves detection capability for rare events and particles beyond the standard model.





PSI

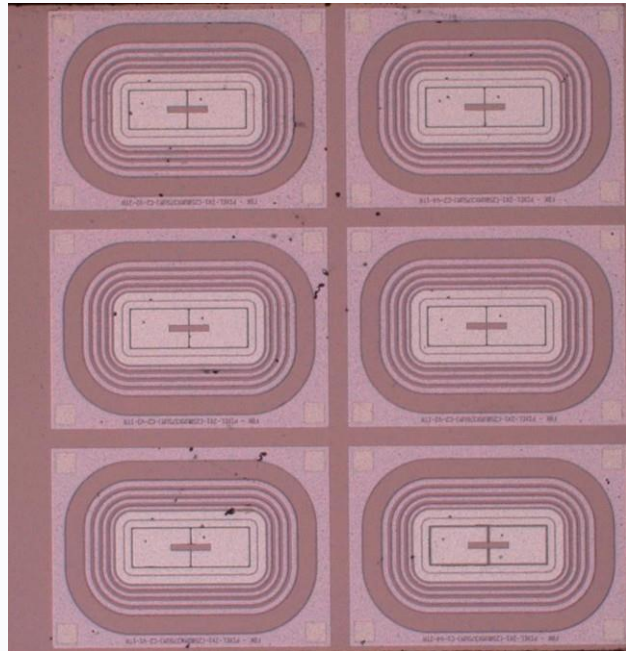
Part 1 LGAD Sensor



PSI

Characterization of Ti-LGAD sensors (setup)

ETHZ Student project (Fynn Hufler)

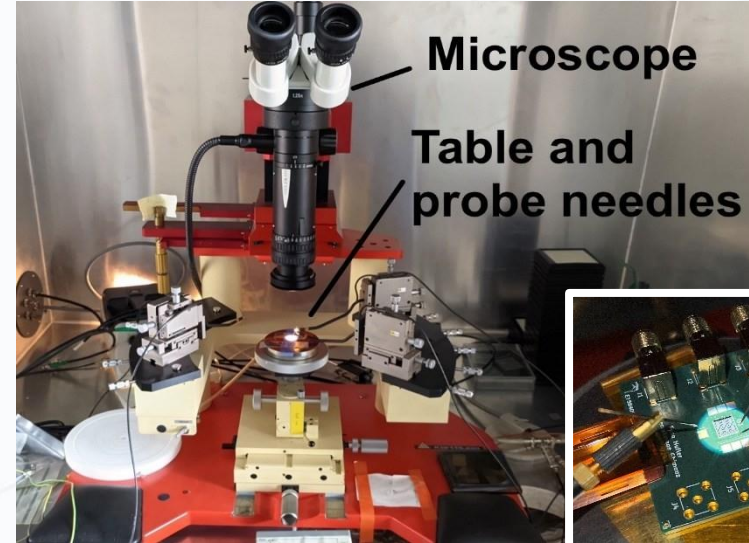
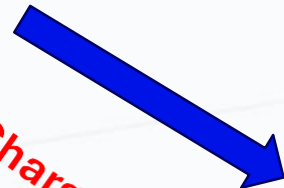


Ti-LGAD sensor **sample**
(Large pixels : $250 \times 375 \mu\text{m}^2$)

Capacitance
measurement

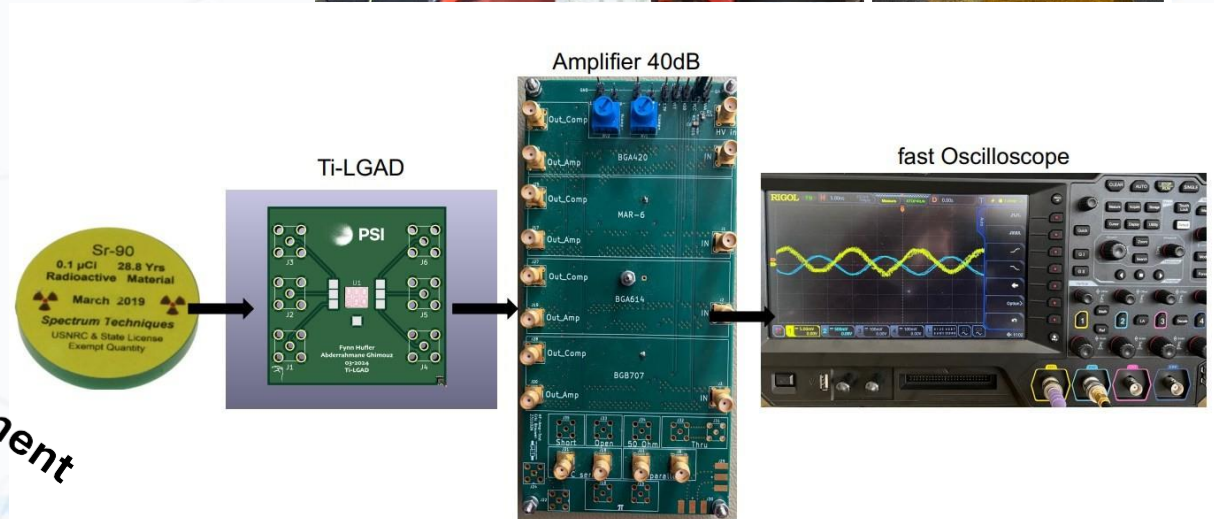
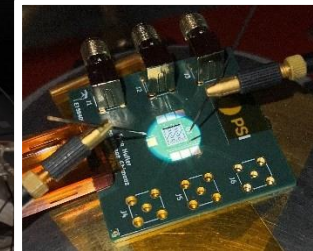


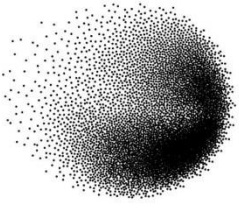
Charge measurement



Microscope

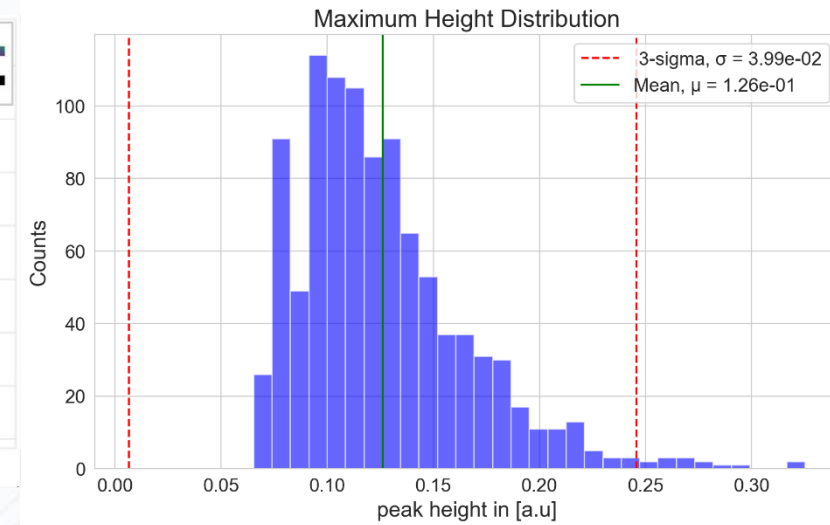
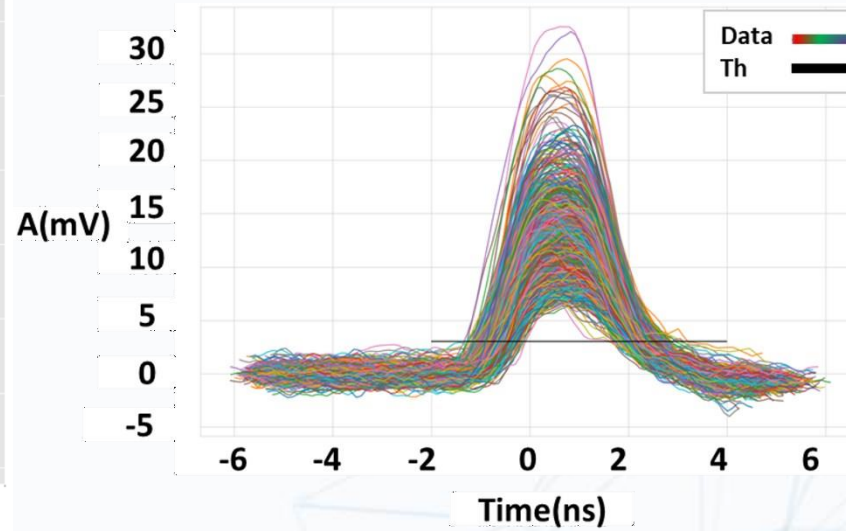
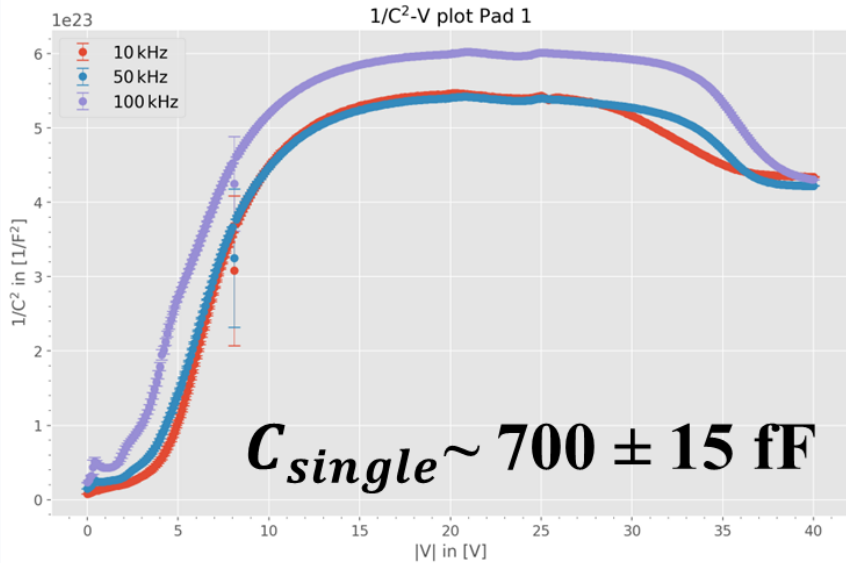
Table and
probe needles



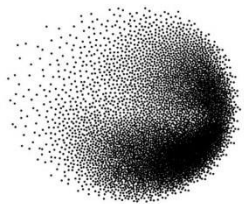


Characterization of Ti-LGAD sensors (results)

ETHZ Student project (Fynn Hufler)



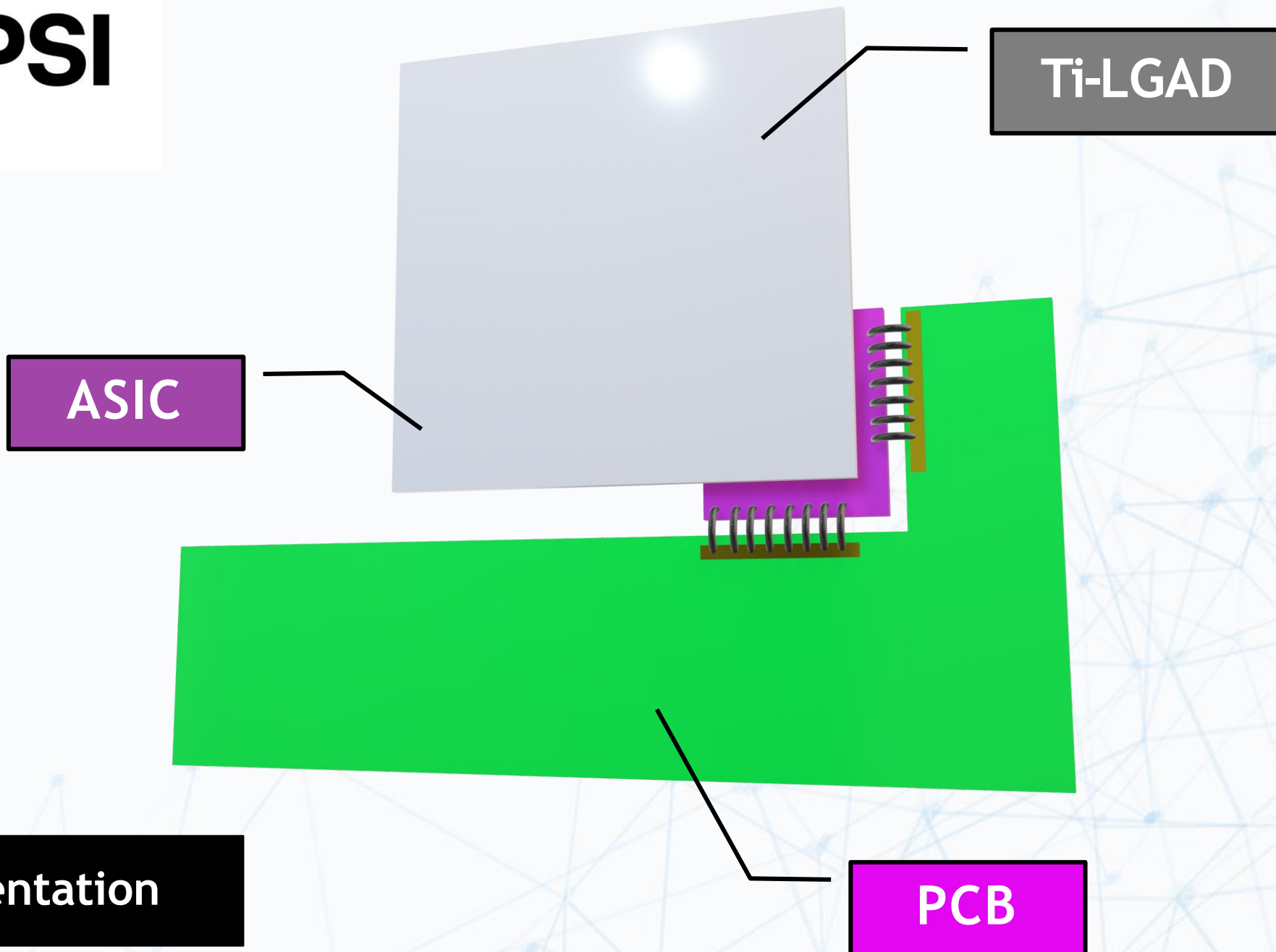
- ✓ Capacitance measurements of Ti-LGAD sensors showed **uniform values** with stable performance across **conditions** and mean capacitance for single pixels ($250 \times 375 \mu\text{m}^2$) is **$\sim 0.70 \text{ pF}$**
 → for the $100 \times 100 \mu\text{m}^2$ Ti-LGAD @ same $50 \mu\text{m}$ thickness : backplane-only estimation is **$\sim 0.075 \text{ pF}$** including inter-pixel: **$\sim 0.12\text{-}0.20 \text{ pF}$** (typical ballpark)
- ✓ The expected **features** of the generated signals were **confirmed**.

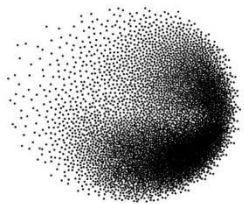


PSI



PSI

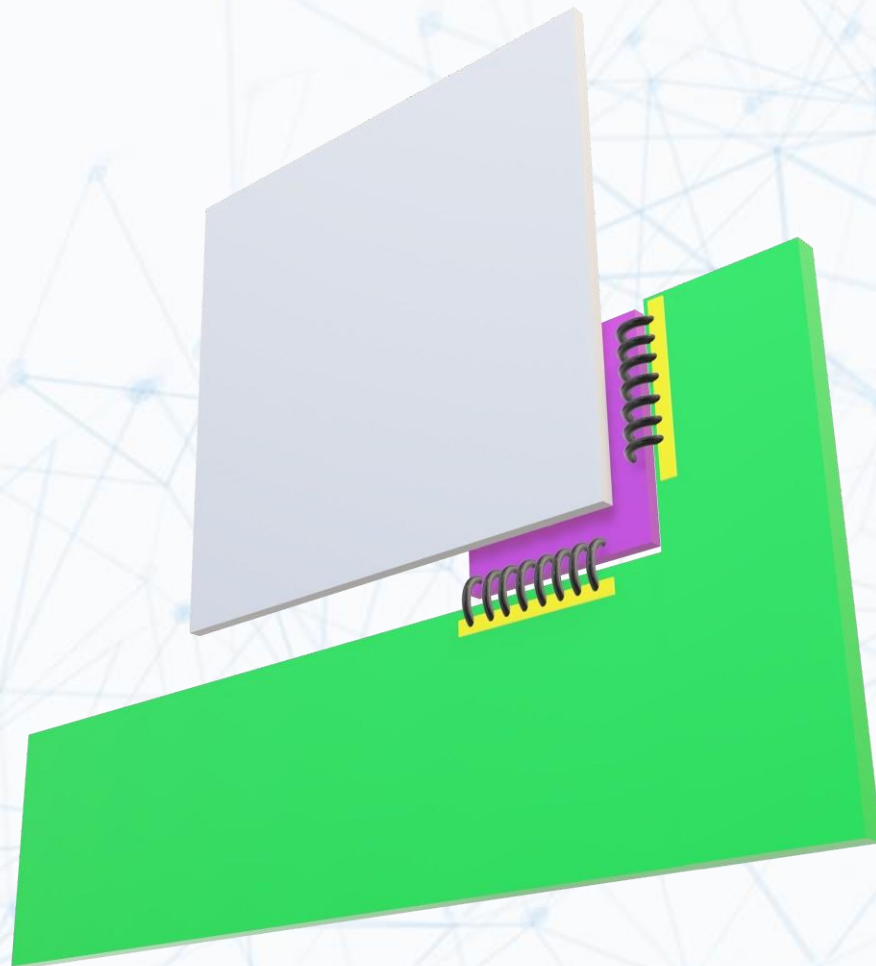
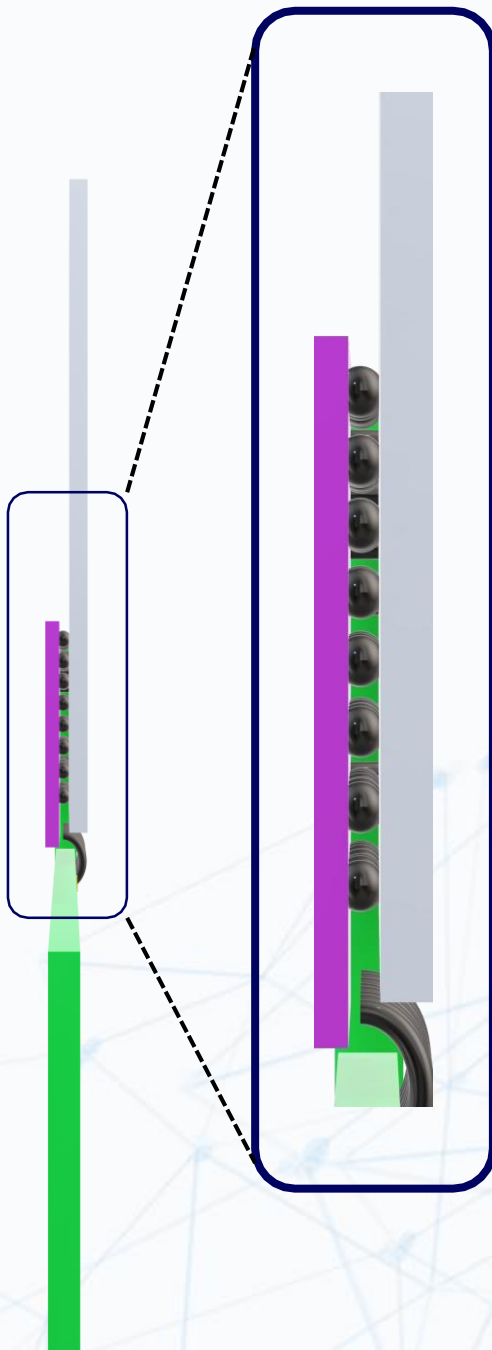
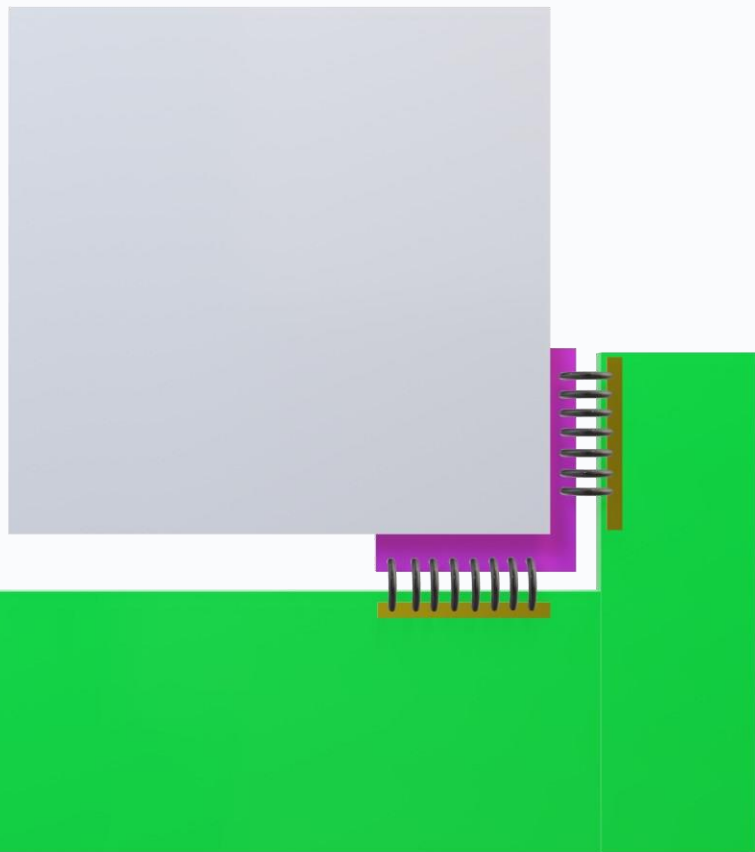




PSI



PSI



Implementation

Part 3 Preamplifier

First flavour CSA (Hans-Christian Kaestli)

Concept

Initial post-layout simulation results

