Development and Testing of an External and Self-Triggering System for HGCAL test systems

R. Shukla, Imperial College London

On behalf on the CMS Collaboration

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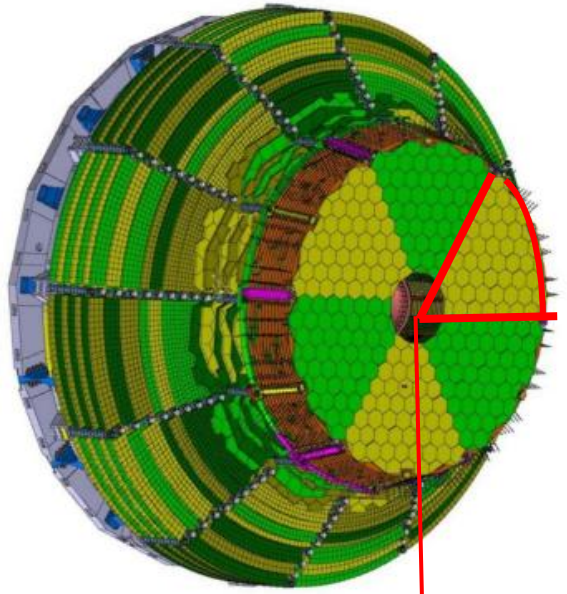
TIFR Mumbai

HGCAL

Overview

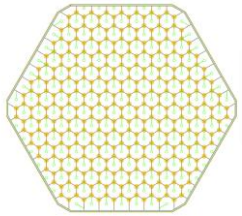
- **H**igh **G**ranularity **Cal**orimeter (HGCAL) is the endcap calorimeter for the CMS (Phase-2)
- HGCAL is a 5-D imaging calorimeter providing fine transverse and longitudinal shower position, energy and precision time measurement
- The HGCAL will be realized as a 47-layer sampling calorimeter
  - CE-E layers (26): Hexagonal Si sensors (cell size ~ 0.5 – 1.1 cm^2)
  - CE-H layers (21): Si sensors + scintillators in low radiation regions
- Each layer consist of self-supporting 'cassettes' which cover 30° or 60° in phi

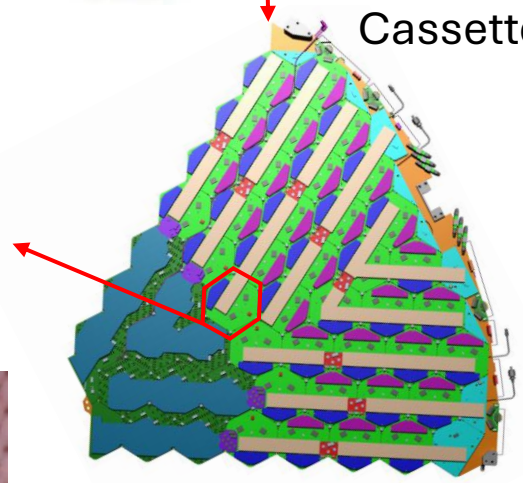
HGCAL End-cap

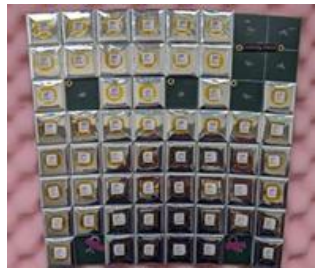


Cassette

Si-Module





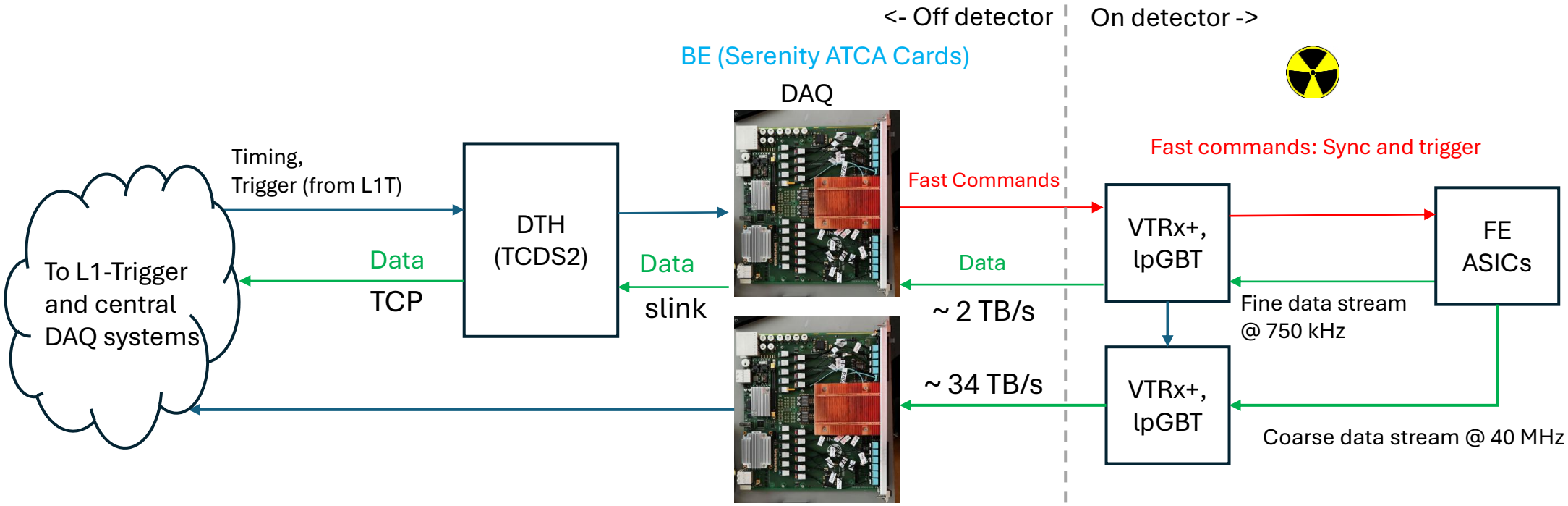


Scint. Tileboard

Ref. Daria's Talk

Look out for Rajdeep's talk tomorrow more information

HGCAL Readout and Triggering



TPG: Two stages (provides 3-D clusters and towers)

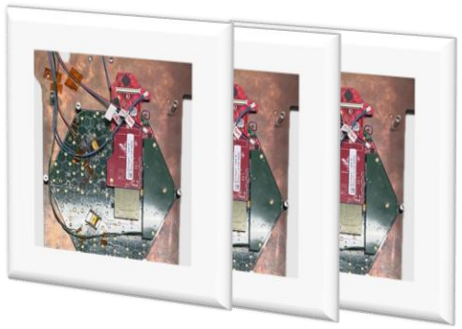
- The CMS experiment has a complex trigger system, which looks at streaming data for each collision from various subdetectors i.e. at 40 MHz (LHC clock)
  - On reception of the trigger (L1-accept) signal, fine grain data i.e. energy and time of arrival from each sensor cell is readout from the Front-End (FE)
- **The collisions and thus the trigger data are synchronous to LHC clock**

HGCAL Test Systems

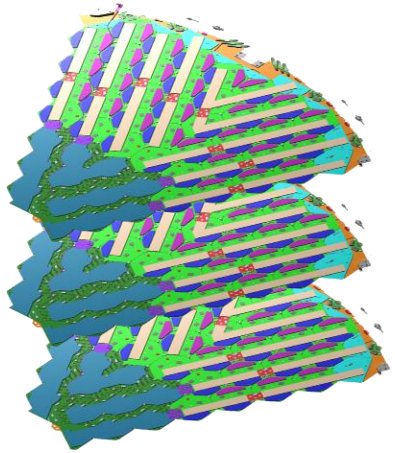
Modules to Sectors

- The HGCAL is now gearing towards production phase and this involves **testing systems of increasing size, leading up to the full detector**

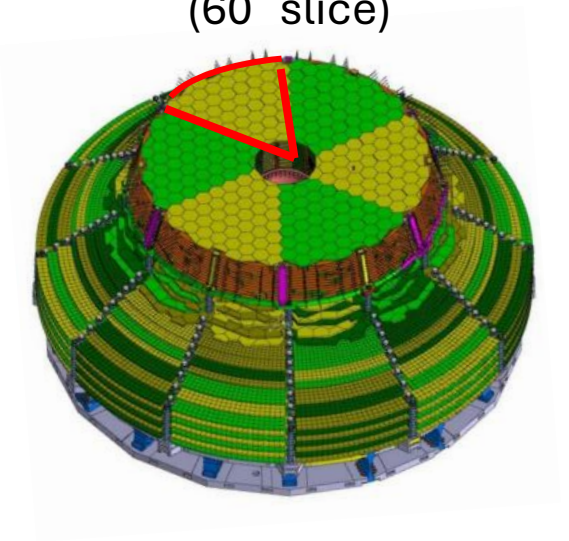
Multi-module tests:
Small stacks in test-beams



Cassette tests:
Single and Multi-cassette (cassette stacks)



Sector tests
(60˚slice)



- HGCAL TPG and overall L1-Trigger are still evolving, and thus final-like triggering is not possible for such tests
- Therefore, simpler and independent trigger system are required
  - Scintillators trigger / External trigger
  - Self-trigger

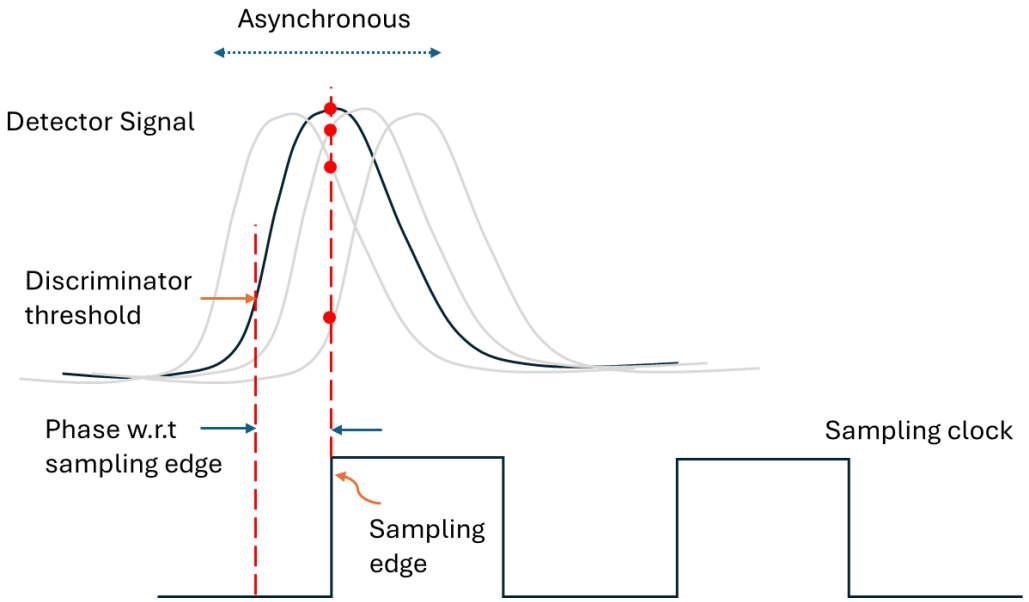
External Trigger

Beamline and Cosmic tests

External trigger

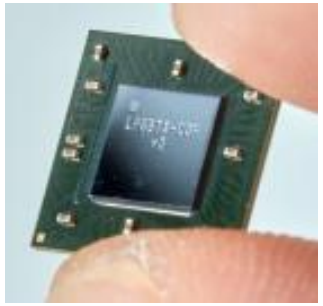
Requirements

- The scintillator trigger is typically used for beam triggers (beam-test) and cosmic test stands
  - In both cases triggers are asynchronous to the detector sampling clock
- Reasonably precise (< ns) time-of-arrival recording is required to select a trigger which is “in-time” for signal-peak at the FE ASIC



External trigger using lpGBT

Why?

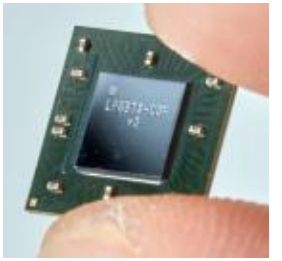


lpGBT web-page

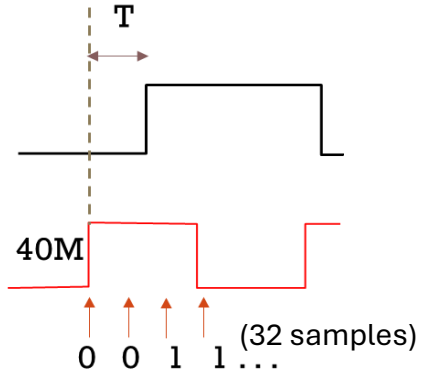
- Previous systems used FPGA based time of arrival measurement or a dedicated Time to Digital Converter (TDC)
  - Separate reference clock distribution to the detector area (80-100m away)
  - Extra communication layer to transfer trigger metadata and signal to BE electronics
  - **Such systems are expensive and not scalable**
- The lpGBT ASIC is at heart of almost all Phase-2 detector systems at CERN and particularly in HGCAL
  - Lot of expertise, hardware and firmware already exists and regularly being used
- Using lpGBT electrical link receiver to sample the discriminated trigger signal solves both issues
  - Very low jitter synchronous (< 5 ps) clock
  - Robust communication layer already implemented as part of the detector FE links receiver for BE
  - Natural extension of the existing FE infrastructure

External trigger using lpGBT

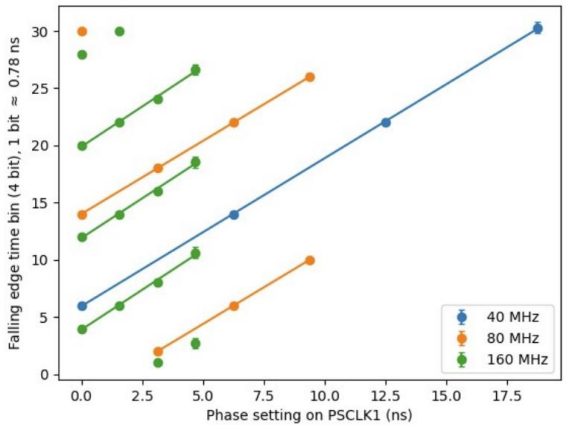
How?



- The lpGBT e-link receiver is used as a high-speed sampler of the discriminated trigger pulse
- At 1.28 Gsps (max for lpGBT), 32 samples are acquired within 25 ns
  - Time resolution: ~ 0.78 ns
  - A stable '0' -> '1' transition indicates presence of trigger
  - Position of the transition gives phase of the signal with respect to 40 MHz reference
  - Finer time resolution is possible by sampling copies of the same signal with phase shifted clocks (being tested)
- A simple firmware implemented to detect the transition and generate a trigger flag in BE
- Firmware also implements various tuning features
  - Programmable delay to tune the latency for the event capture
  - Programmable 32-bit sliding window for transition finding
  - Optional veto window to kill the triggers for N BX after a trigger



Private work

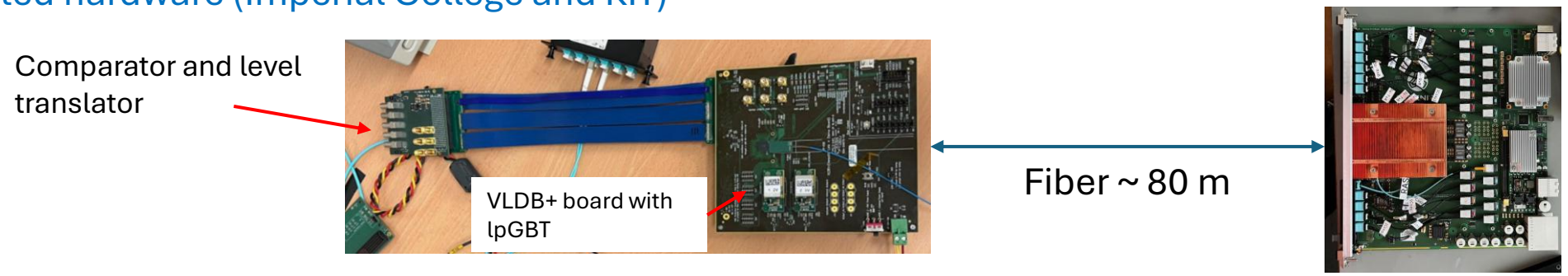


LpGBT sampling test with lpGBT generated clocks at different phases (F. Hummer)

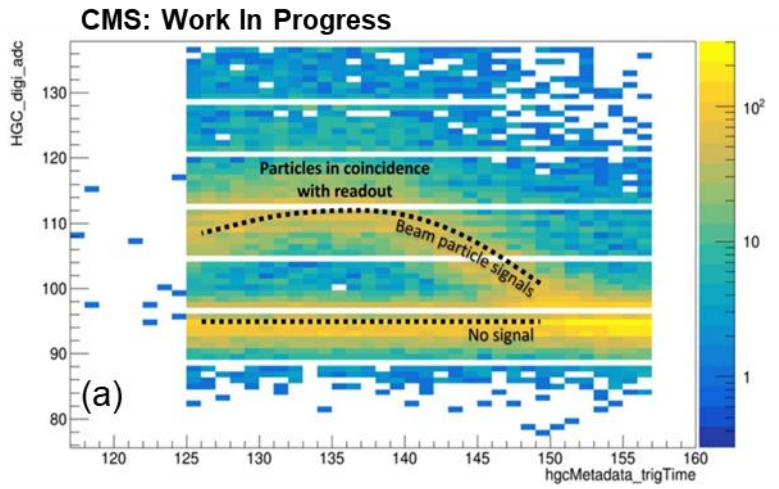
lpGBT based external trigger

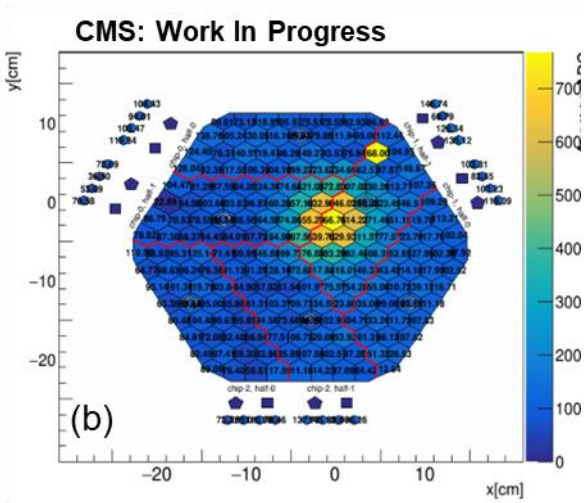
Implementation and Tests

- The system was first tested with off-the shelf prototype boards and has been evolving with design of dedicated hardware (Imperial College and KIT)



- It has been successfully used in HGCAL beam-tests from 2023 to 2025
  - Plot (a) effect of FE shaper sampling phase on recoded ADC value
  - Plot (b) shows the 2D histogram of ADC values showing beam spot clearly with 'in-phase' events selected
- The system will be extended to be used for upcoming cassette tests



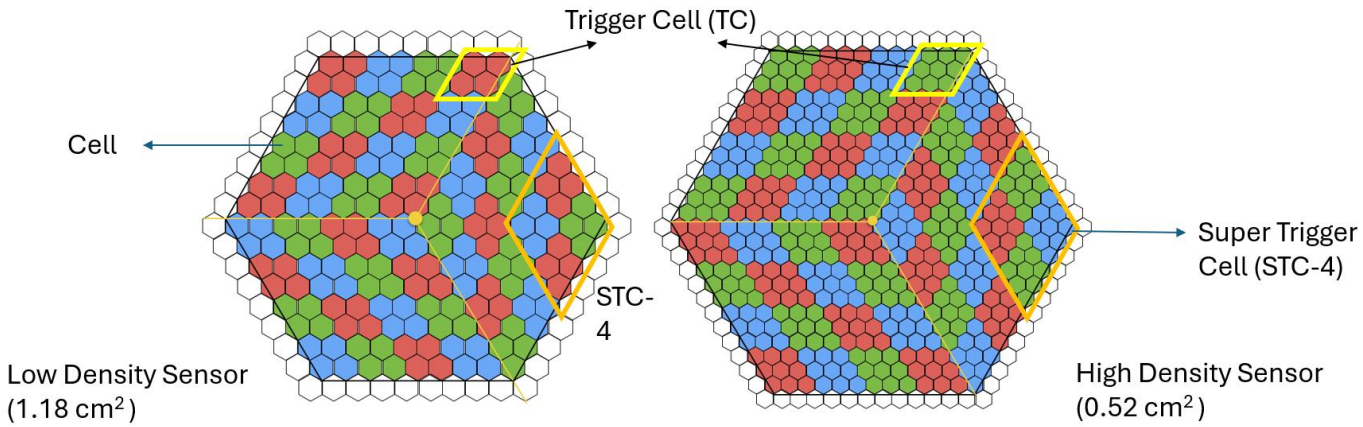


Ref. The CMS HGCAL trigger data receiver
DOI 10.1088/1748-0221/19/01/C01049

Self-Trigger

Self-Trigger

Using Coarse Sensor Data



- Self-trigger uses the coarse data from the FE i.e. **Trigger Cells to select an event**
  - Uses energy threshold (above noise floor) to select a genuine event
  - Bypasses the rest of the TPG path
- Aiming for two major applications of the self-trigger
  - Noise study in a single cassettes
  - Cosmic trigger for sector tests where scintillator trigger may not be possible

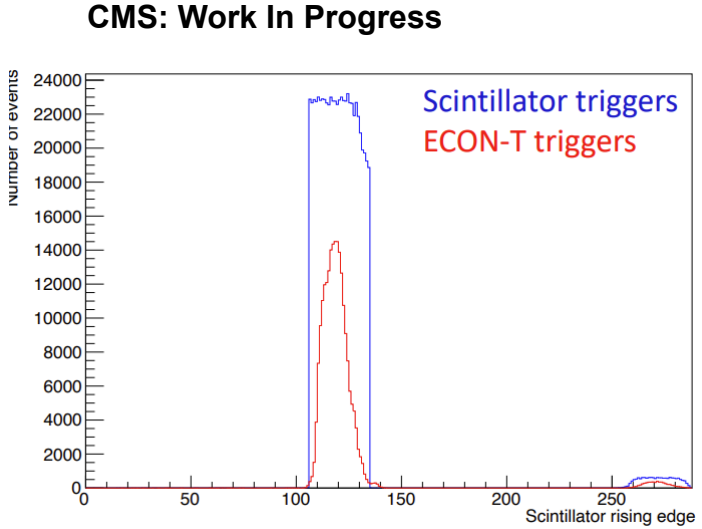
Self-trigger

Implementation and Tests

- Self-trigger firmware implemented in Stage-1 of the TPG BE board
  - One self-trigger block for each module (48 channels/TCs)
  - Threshold to apply energy cut on the TCs
  - TC mask to ignore noisy channels
  - Programmable delay line for trigger latency tuning

- Core firmware tested in beam-test along with scintillator trigger

- More elaborate multi-board self-trigger and scintillator trigger aggregator is being developed for HGCAL sector tests



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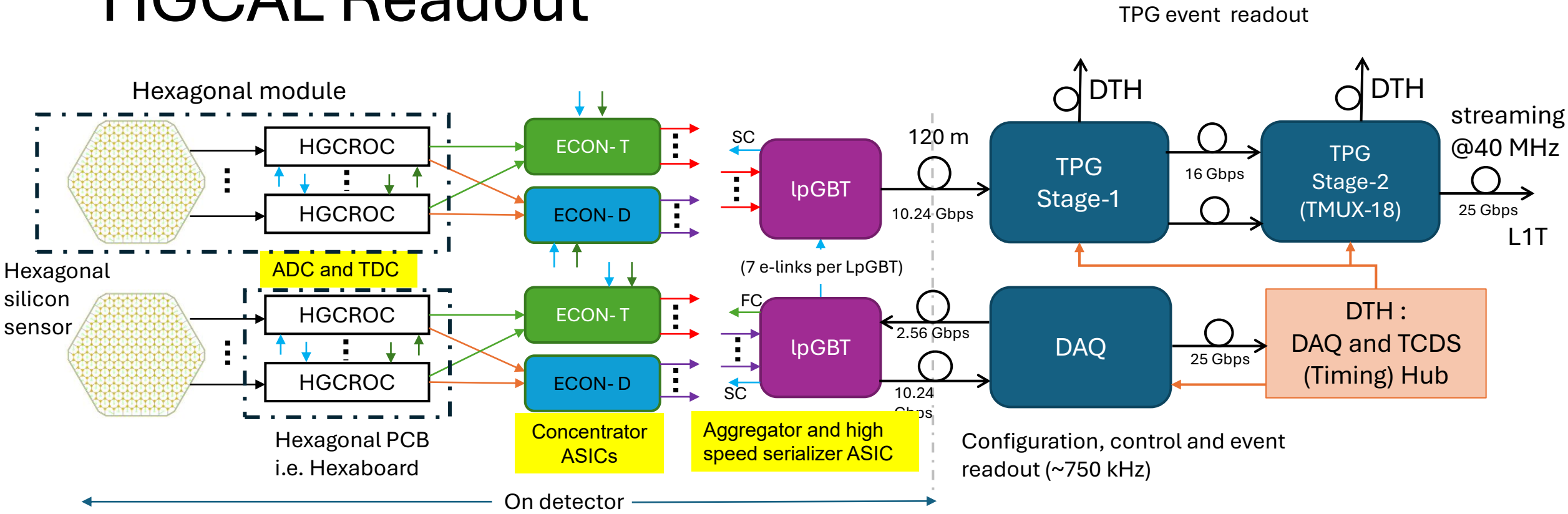
Summary and Outlook

- Novel lpGBT based external trigger system has been developed for HGCAL test systems
  - The system provides 0.78 ns time-of-arrival resolution for the trigger and has been used successfully in several beam-test campaign
  - Alternative to expensive FPGA and/or TDC based systems
  - Does not need dedicated time base synchronisation and optical interface allows long distance operation
  - We are also working on multi-phase sampling approach to achieve much smaller timing resolution
- The self-trigger system uses existing TC data from the sensor to generate a trigger
  - Very useful to study noise behaviour of the system
  - Being explored for cosmic triggering of the HGCAL sector
  - Bigger multi-board self-trigger aggregation system is under development

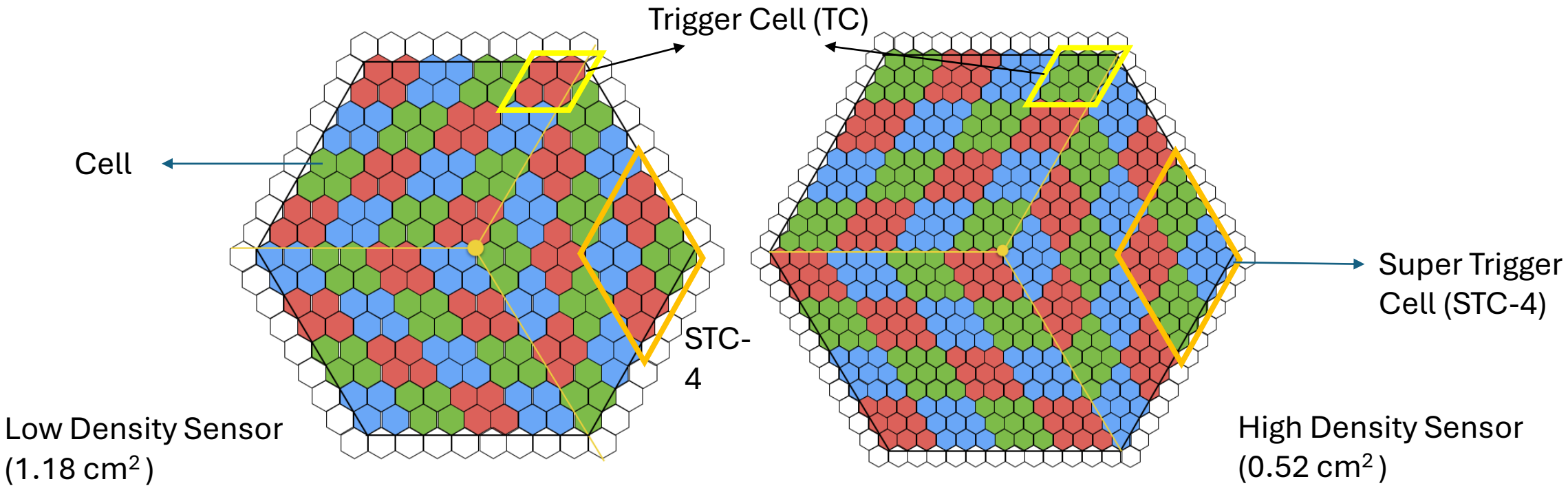
Backup

HGCAL Readout



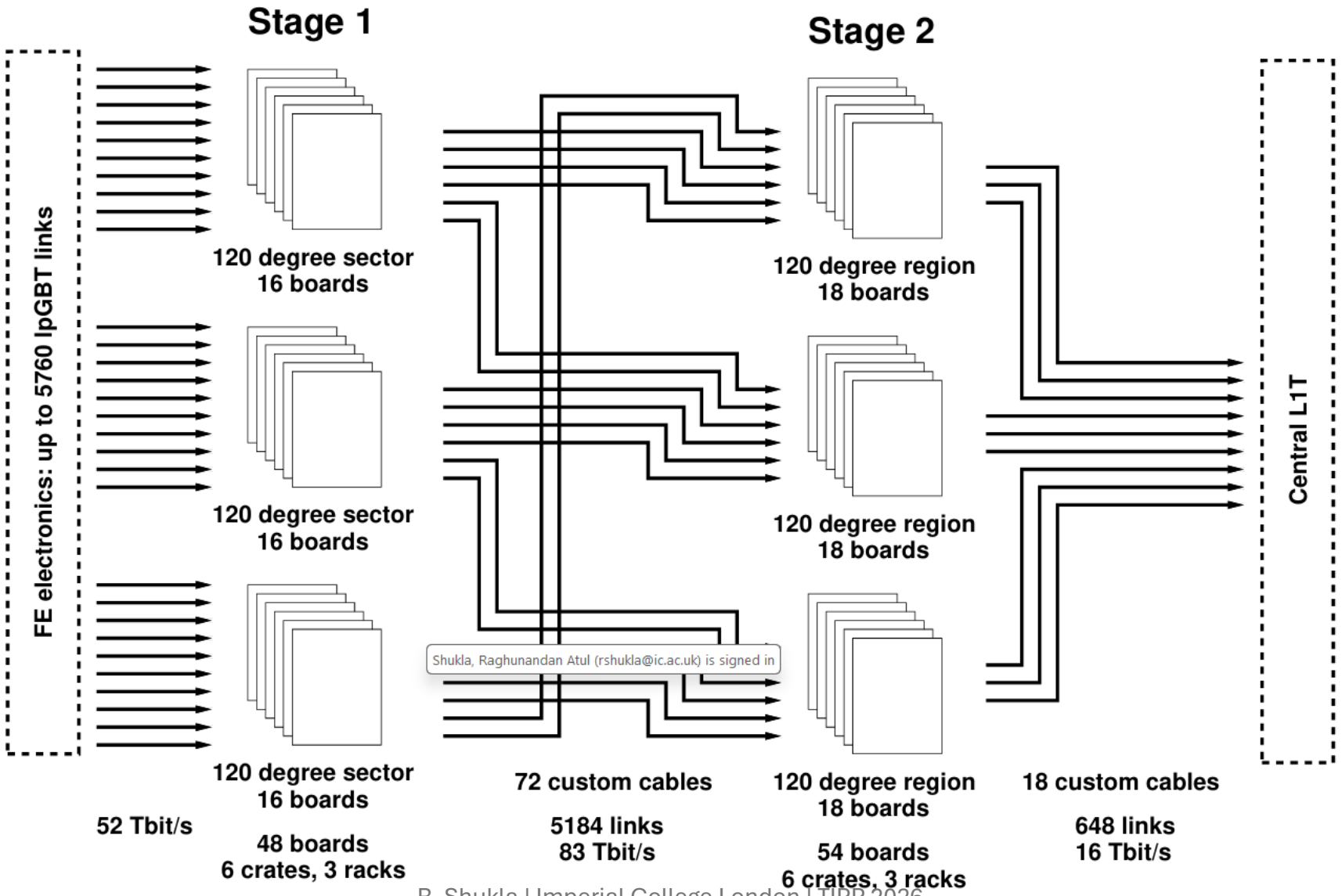
- HGCROC (readout chip) reads each cell from the sensor (charge and timing) and computes Trigger Cells
  - Information further compressed on-detector by concentrator ASICs (ECONs)
  - Sent to off the detector using CERN lpGBT and VTRX+ system
- Large number of links: ~10k DAQ and Trigger lpGBTs (Low-power Gigabit Transceiver)
- All BE subsystems are envisaged to be implemented on common Serenity ATCA platform and associated firmware/software infrastructure (EMP/HERD)

Trigger Cells

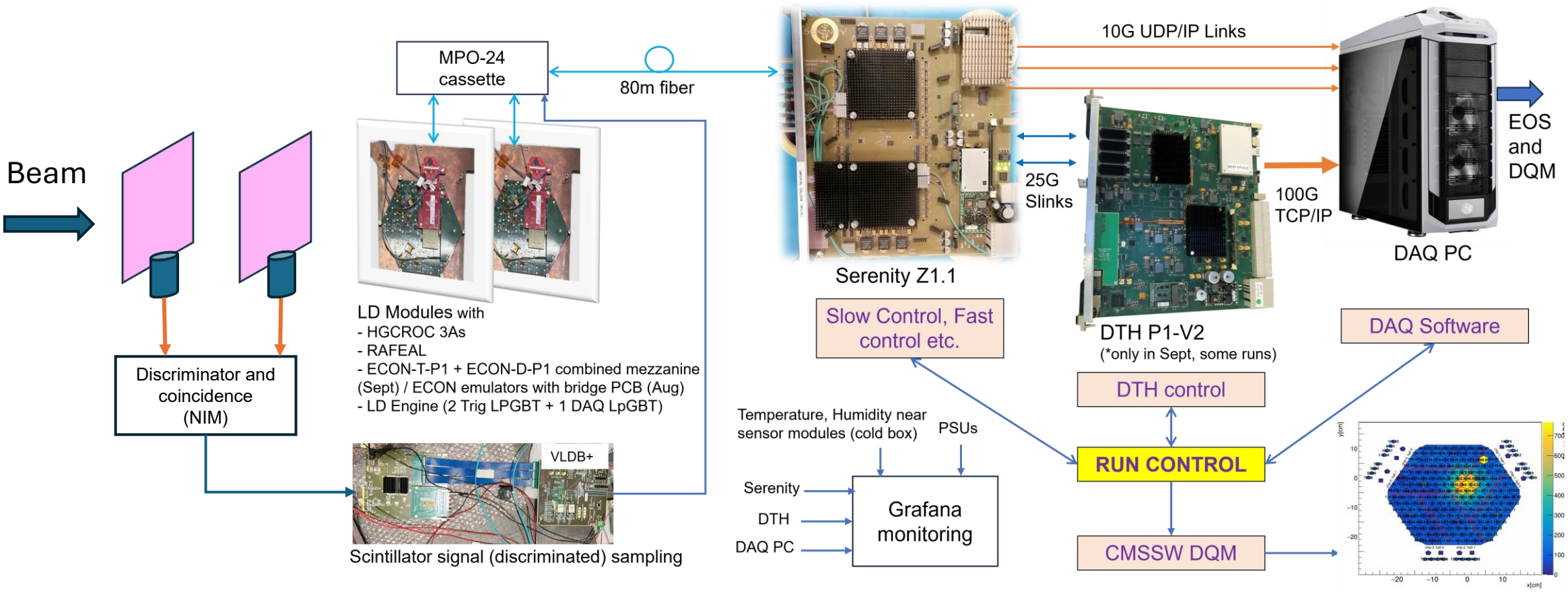


- HGCROC also adds sensor cells (change) to a coarser unit i.e. collection of 2x2 or 3x3 cells to form a Trigger Cell (TC) – these propagate through trigger path
- The concentrator ASIC (ECON-T) can further add-up trigger cells to form Super Trigger Cells (STC) and also calculates sum of energies for whole module (Module Sum) for some algorithms
    - Baseline is to use ECON-T with Best Choice configuration in CE-E and STC configuration in CE-H

TPG architecture



Typical Beam-test Setup



lpGBT ASIC

Specifications

- lpGBT (Low-Power GigaBit Transceiver) is an ASIC developed at CERN ECE group which provides
  - Very low jitter (< 5 ps) BE synchronous clock and control bus distribution
    - Control using IC, I2C and HDLC protocols
  - Seven 1.28 Gbps electrical links (e-links)
  - 10.24 Gbps uplink to the Backend
  - Data integrity with scrambling and error correcting encoding (FEC5/FEC12)
  - System monitoring using ADCs and temperature sensor