

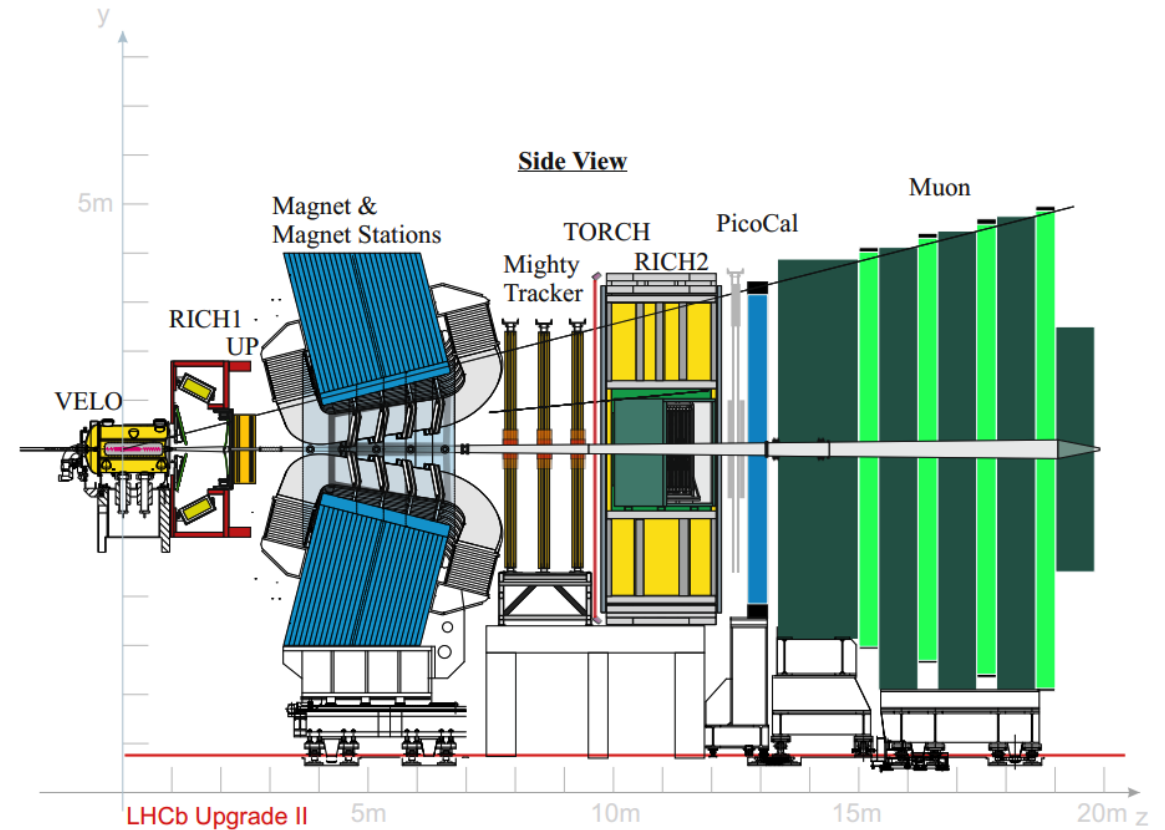
# Recent progress and R&D toward LHCb VELO Upgrade II

**Morag Williams on behalf of LHCb VELO group and LHCb collaboration**

# LHCb Upgrade II

Required to fully exploit flavour physics under high pile-up HL-LHC conditions

- Installation during LHC long shutdown 4
- Aim: similar or better signal-to-background discrimination as current detector



*Schematic side-view of the Upgrade II baseline detector, from LHCb UII scoping document [1].*

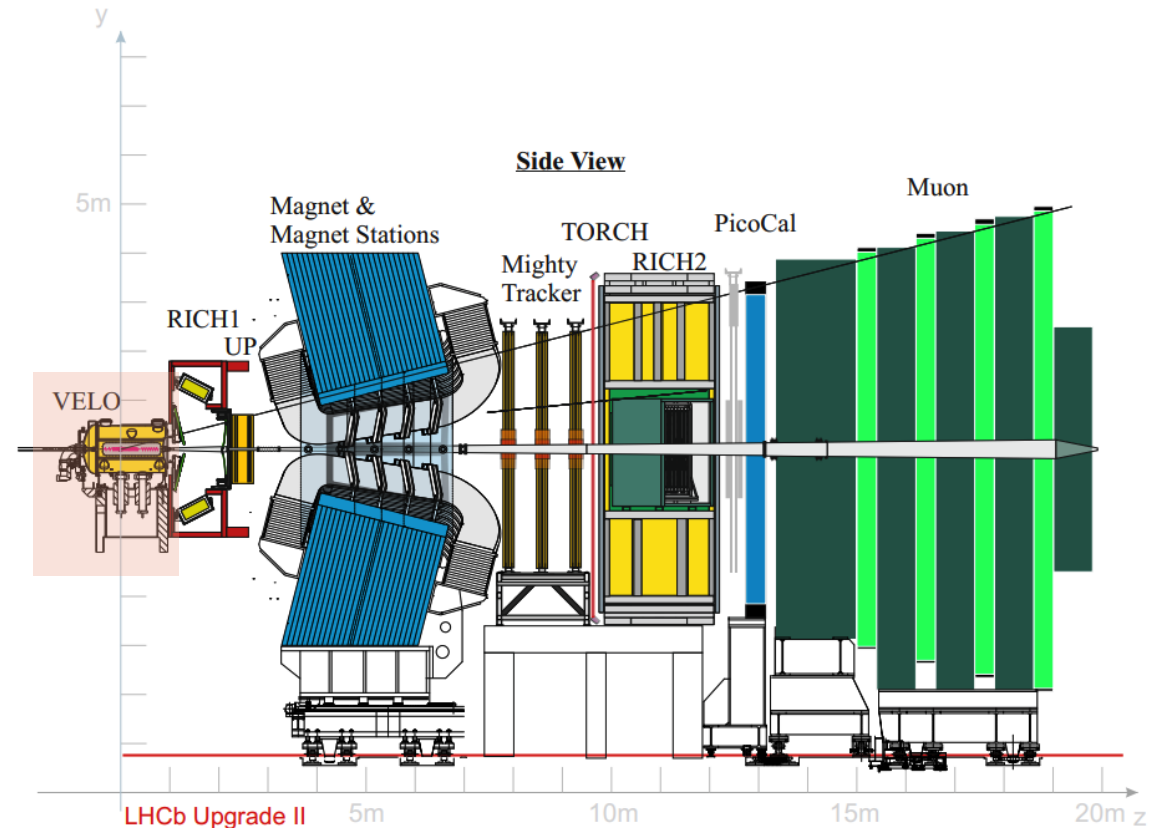
# LHCb Upgrade II

Required to fully exploit flavour physics under high pile-up HL-LHC conditions

- Installation during LHC long shutdown 4
- Aim: similar or better signal-to-background discrimination as current detector

Challenging HL-LHC environment, especially for the vertex detector, the VELO:

- ~40 interactions per bunch crossing → challenging primary and secondary vertexing
- Increased particle multiplicity and extreme rates
- Non-uniform radiation damage  $\leq 6 \times 10^{16}$  MeV  $n_{eq}$   $cm^{-2}$  → radiation hardness challenge for sensors and electronics



*Schematic side-view of the Upgrade II baseline detector, from LHCb UII scoping document [1].*

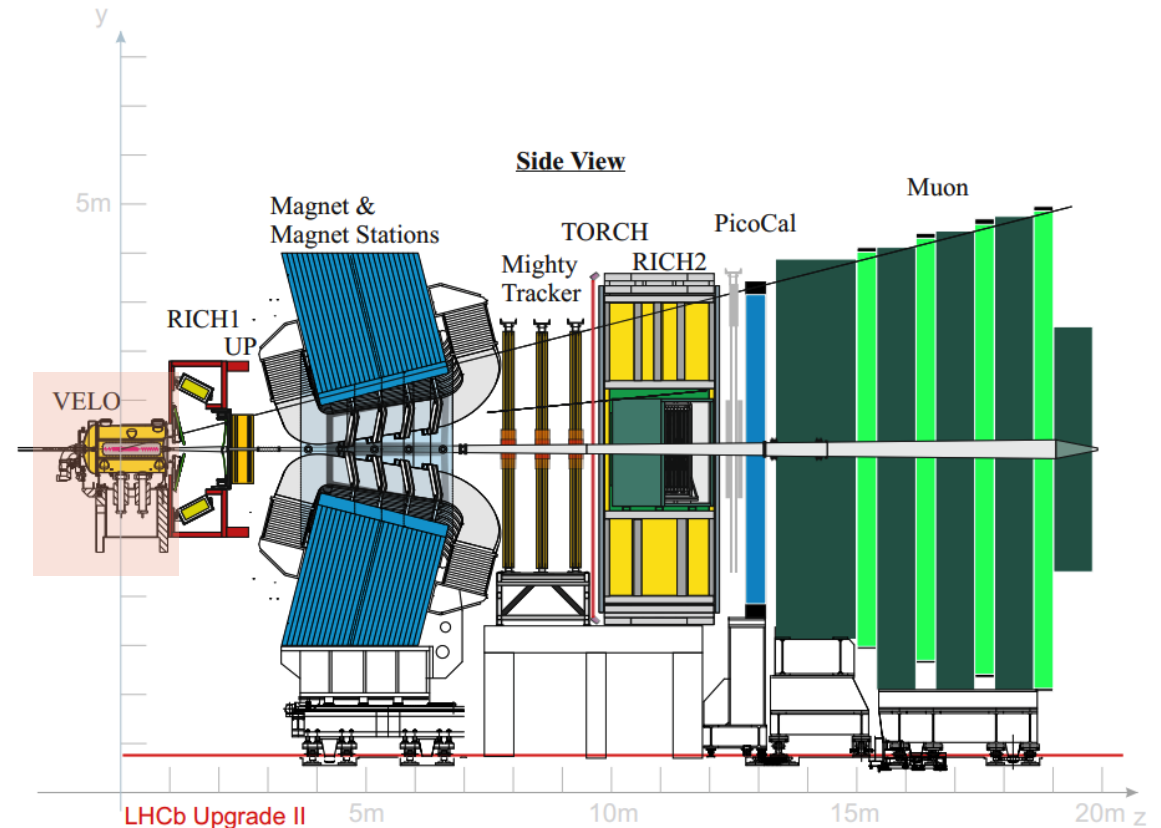
# LHCb Upgrade II

Required to fully exploit flavour physics under high pile-up HL-LHC conditions

- Installation during LHC long shutdown 4
- Aim: similar or better signal-to-background discrimination as current detector

Challenging HL-LHC environment, especially for the vertex detector, the VELO:

- ~40 interactions per bunch crossing → challenging primary and secondary vertexing
- Increased particle multiplicity and extreme rates
- Non-uniform radiation damage  $\leq 6 \times 10^{16}$  MeV  $n_{eq}$   $cm^{-2}$  → radiation hardness challenge for sensors and electronics



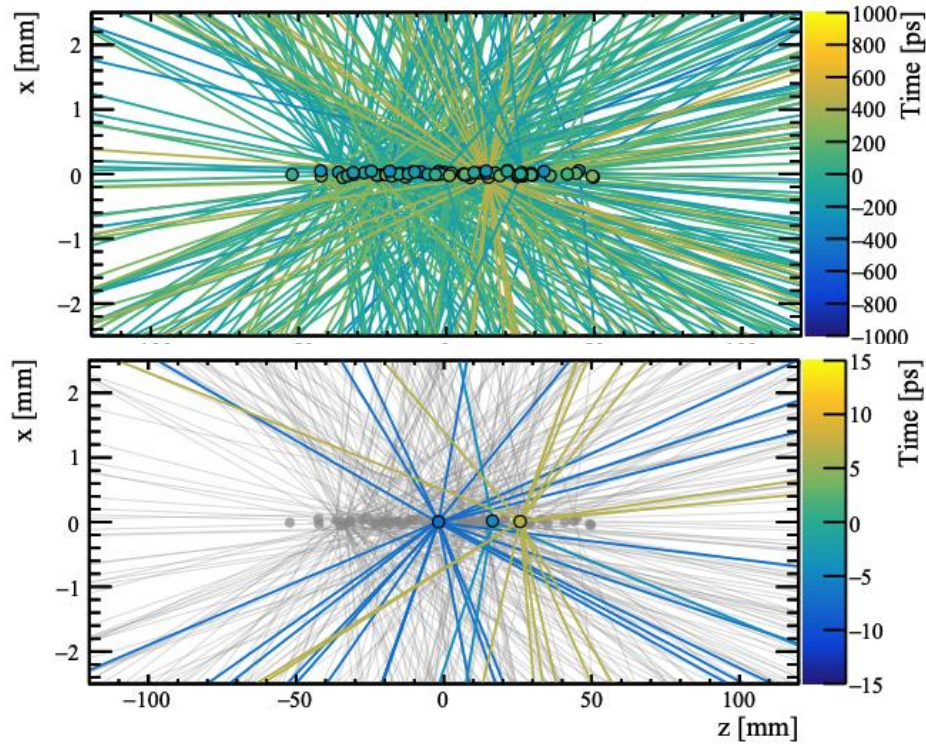
Schematic side-view of the Upgrade II baseline detector, from LHCb UII scoping document [1].

→ For more details on current VELO detector, see talk on Radiation Damage and Operation of the LHCb Upgrade I Vertex Locator by Valeriia (2<sup>nd</sup> Feb, parallel session-II).

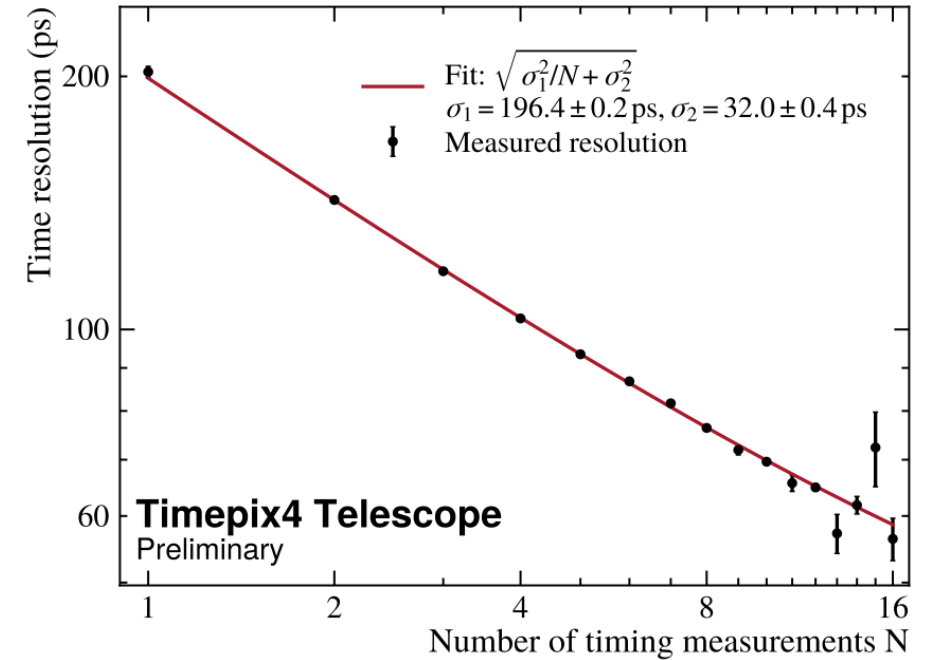
# VELO UI: strategy

## 1) Pixel detector with timing information (4D)

- time resolution of  $\leq 50$ ps per hit to suppress background from pile-up



Tracks produced in a bunch crossing with  $\sim 40$ pp collisions, as seen from a detector with no timing capability (top) and with 30ps selection (bottom) [1].



Preliminary testbeam measurements using the LHCb Timepix4 telescope, showing the improvement in track time resolution with increasing number of measurements [2][3].

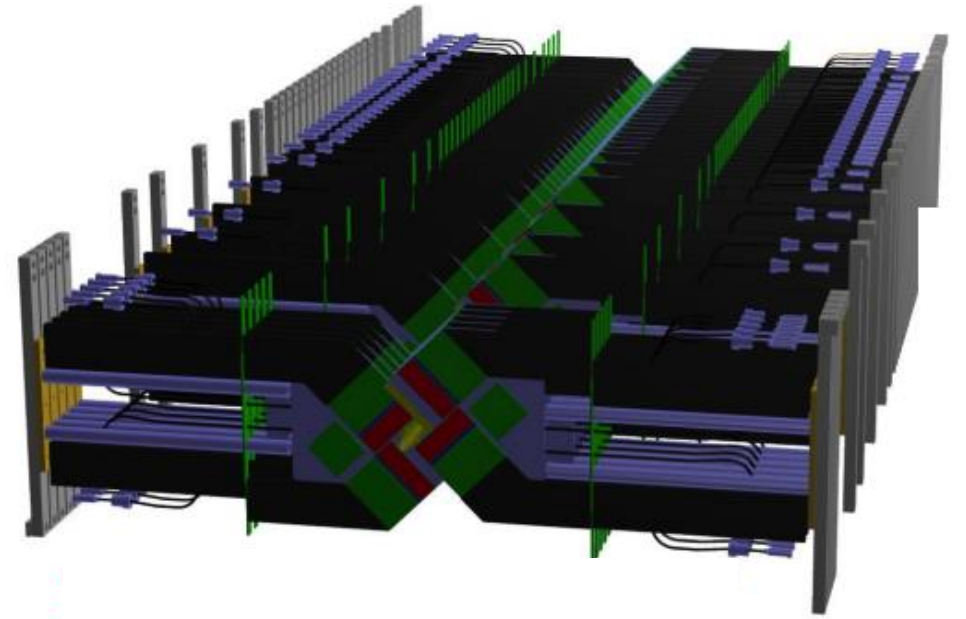
# VELO UII: strategy

## 1) Pixel detector with timing information (4D)

- time resolution of  $\leq 50$ ps per hit to suppress background from pile-up

## 2) Radiation-hard technologies

- ASIC developed in 28nm CMOS technology
- Move to radiation hard sensor technologies, like 3D sensors
- Module inner radius increased  $\rightarrow$  halves highest radiation damage, relying on precision timing to maintain resolution



*Simulated design of the baseline UII VELO detector, with an inner radius of 7.2mm and reduced material budget. Current simulated mechanics are placeholders and are under study [4].*

# VELO UI: strategy

## 1) Pixel detector with timing information (4D)

- time resolution of  $\leq 50$ ps per hit to suppress background from pile-up

## 2) Radiation-hard technologies

- ASIC developed in 28nm CMOS technology
- Move to radiation hard sensor technologies, like 3D sensors
- Module inner radius increased  $\rightarrow$  halves highest radiation damage, relying on precision timing to maintain resolution



**Detector simulation feedback  
plays a critical role in plans  
and studies**

# 3D sensor design

## 3D sensors:

- Intrinsically fast and radiation hard from lateral charge transport in high E fields
- Signals induced closer in time than in planar sensors due to short inter-electrode distance

→ interesting technology for VELO UII

## Technology also introduces challenges:

- High sensor capacitance worsens front-end timing jitter
- Reduced detection efficiency from electrode 'dead'-areas
- Highly non-uniform E field

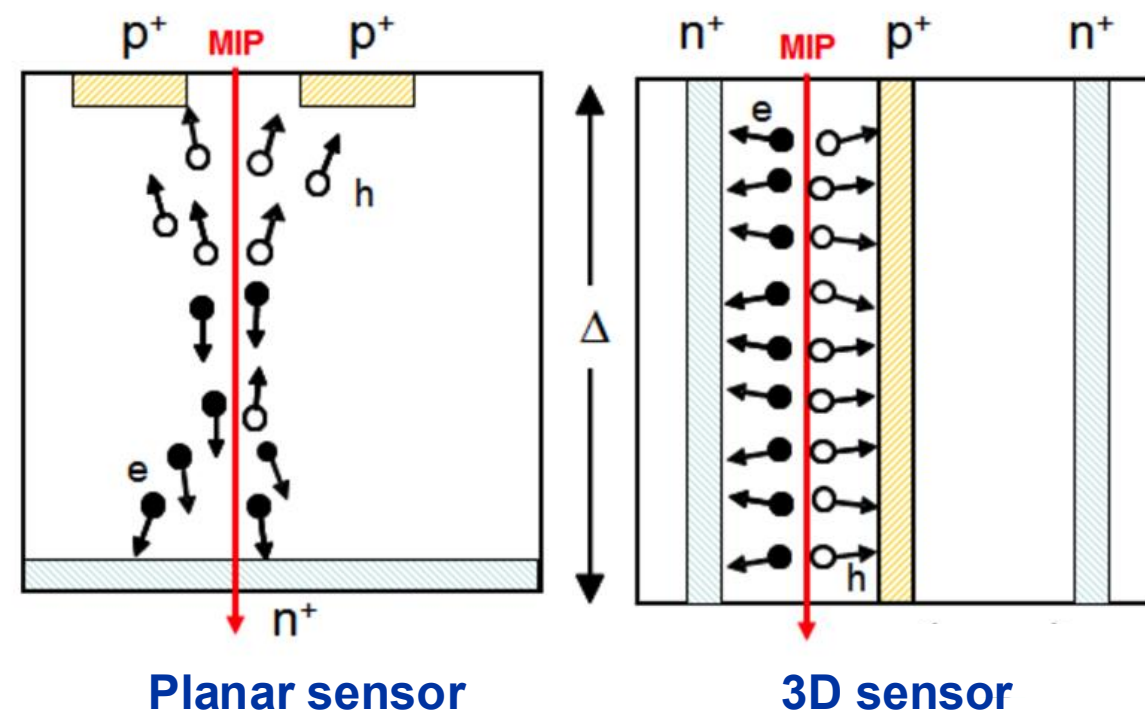
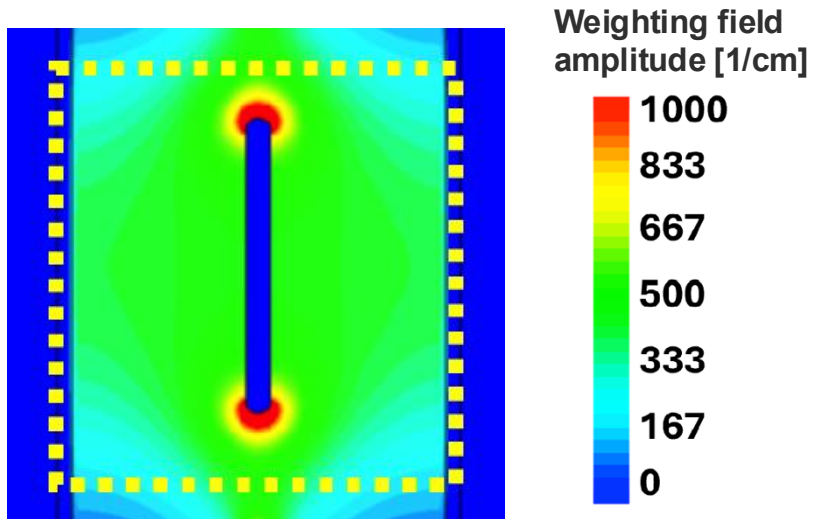


Diagram of planar and 3D sensor charge transportation [5]

# 3D sensor design

Large parameter space of design configurables for 3D sensors:

Trench-shaped central electrode:



For a 55 $\mu\text{m}$  pitch and 150 $\mu\text{m}$  thick sensor:

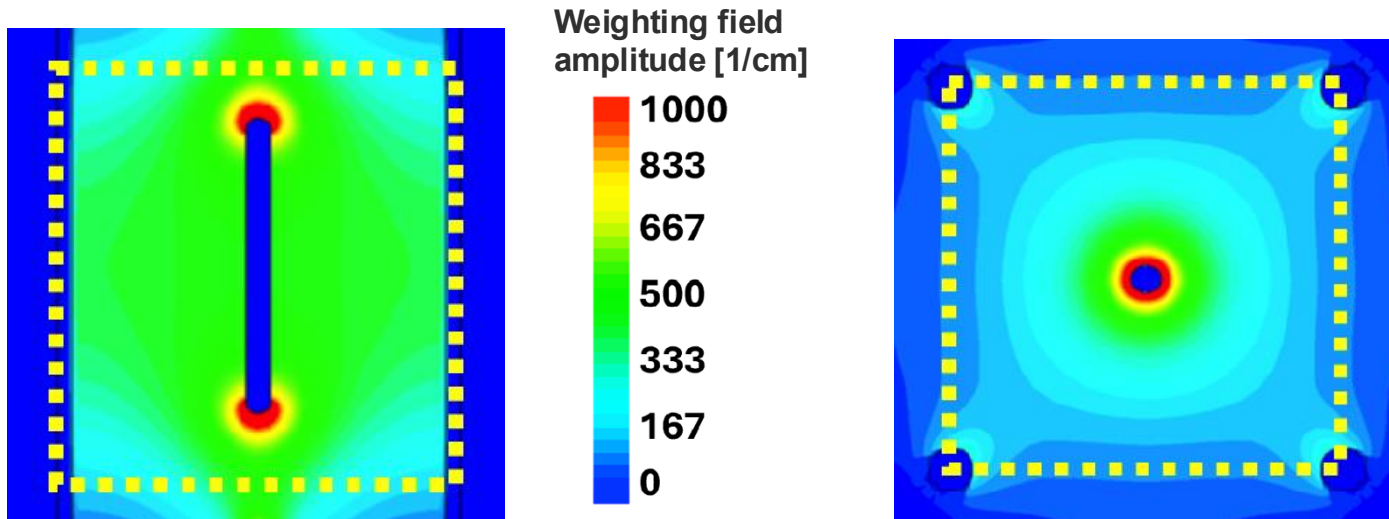
Electrode geometry	Simulated $\sigma_t$ [ps]	Capacitance [fF]
Trench	30	~100

# 3D sensor design

Large parameter space of design configurables for 3D sensors:

Trench-shaped central electrode:

Columnar single electrode ('1E'):



For a 55 $\mu\text{m}$  pitch and 150 $\mu\text{m}$  thick sensor:

Electrode geometry	Simulated $\sigma_t$ [ps]	Capacitance [fF]
Trench	30	~100
1E	73	35

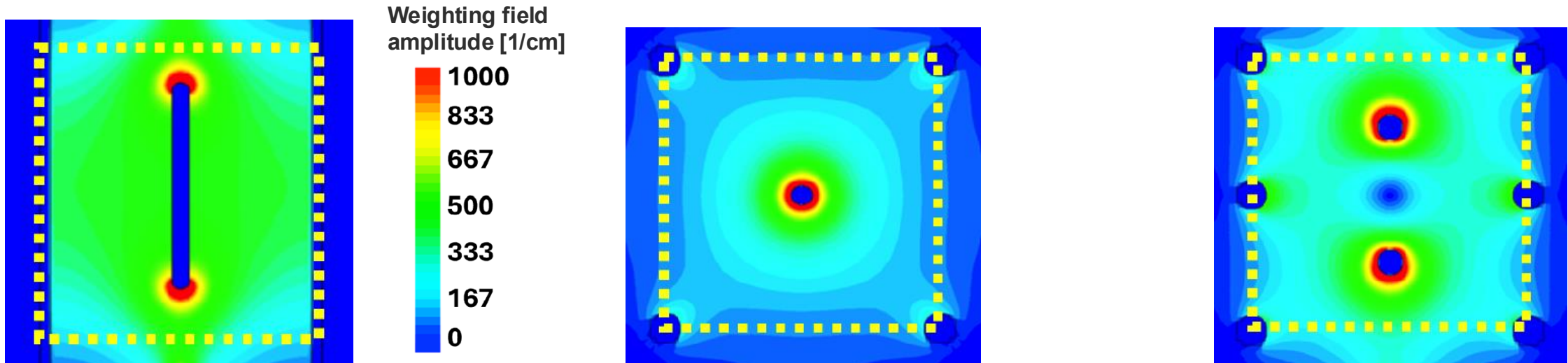
# 3D sensor design

Large parameter space of design configurables for 3D sensors:

Trench-shaped central electrode:

Columnar single electrode ('1E'):

Columnar multi-electrode (e.g. 323):



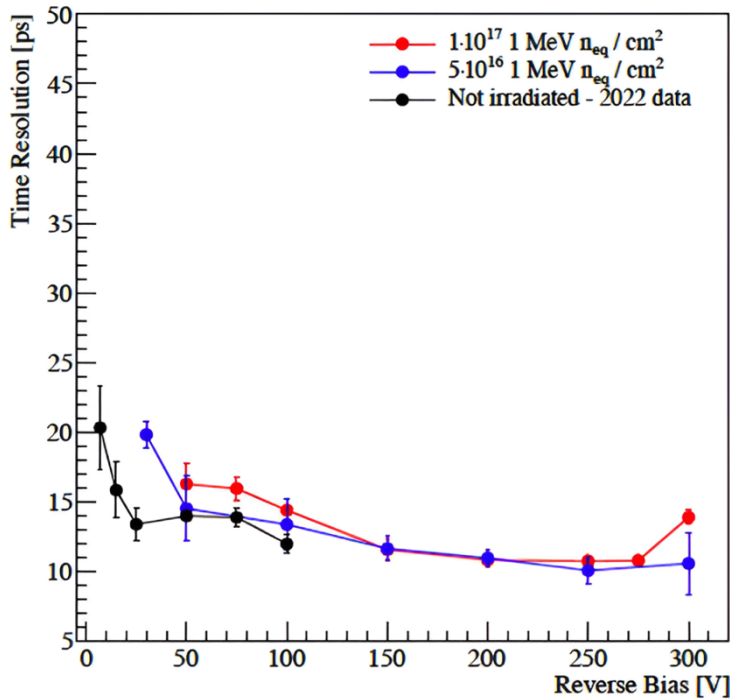
For a 55 $\mu\text{m}$  pitch and 150 $\mu\text{m}$  thick sensor:

Electrode geometry	Simulated $\sigma_t$ [ps]	Capacitance [fF]
Trench	30	~100
1E	73	35
323	38	60

# 3D sensor performance

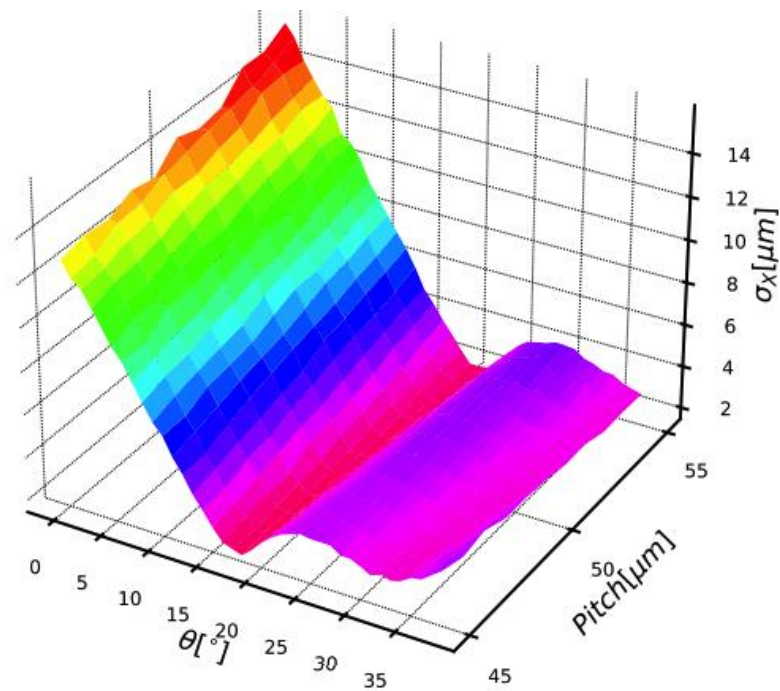
## Key figures-of-merit for VELO UII

Radiation hardness, timing...



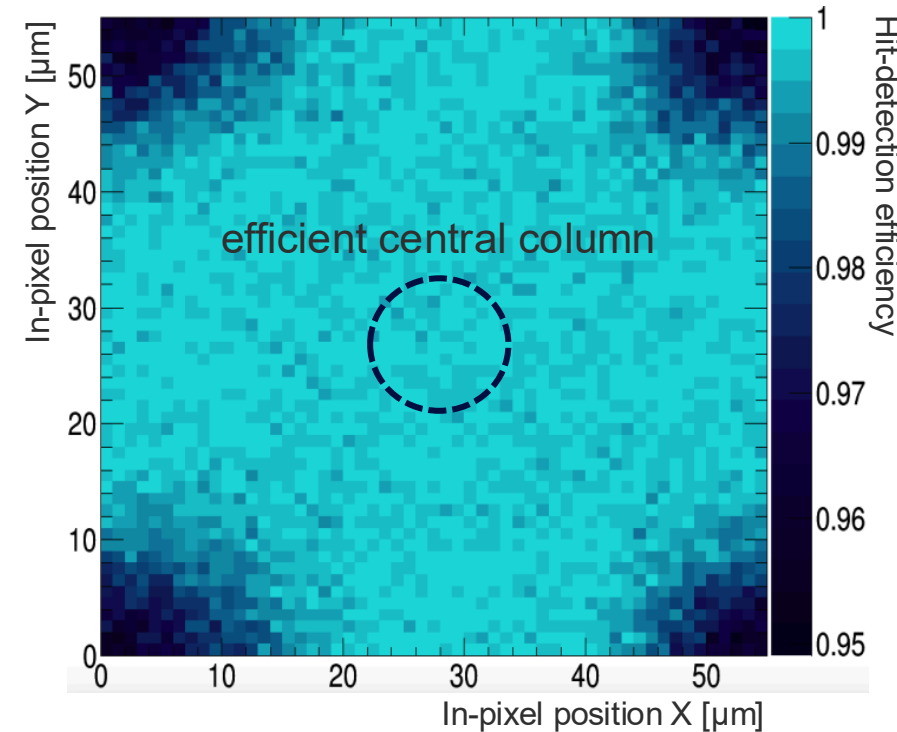
Testbeam measurement of FBK 3D trench assemblies with pitch  $55\mu\text{m}$  and thickness  $150\mu\text{m}$ , irradiated and non-irradiated [7].

...spatial resolution...



Simulated 3D sensor spatial resolution for  $150\mu\text{m}$  thick 1E sensor for different pitches and track incidence angle [8].

...and detection efficiency

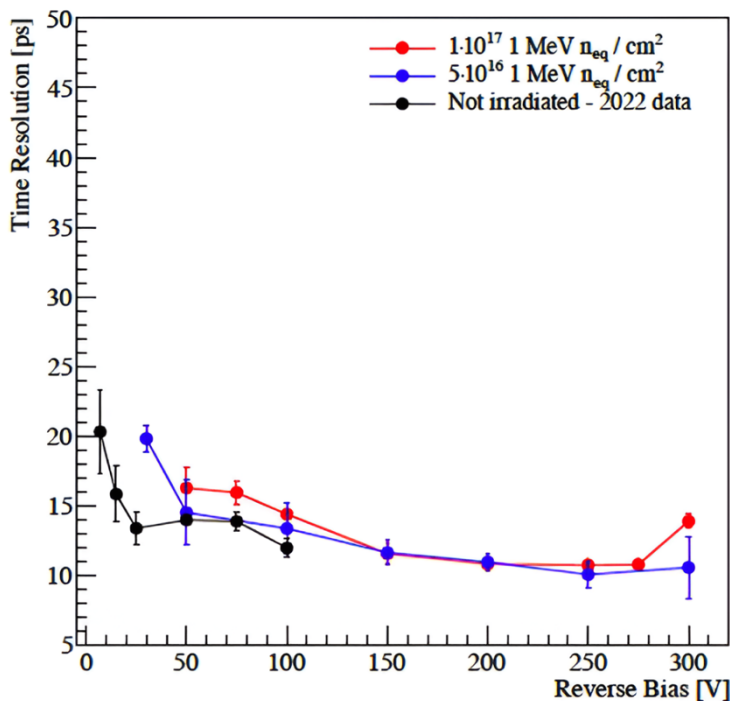


Testbeam hit-efficiency measurement of CNM 3D 1E assemblies on Timepix4 ASICs with pitch  $55\mu\text{m}$ , 60V bias, threshold of  $2ke^-$  [9].

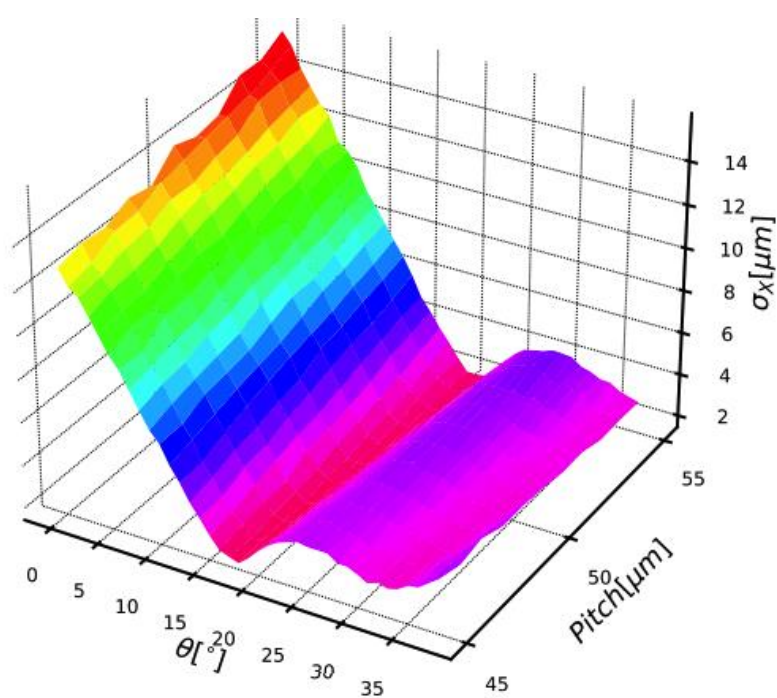
# 3D sensor performance

## Key figures-of-merit for VELO UII

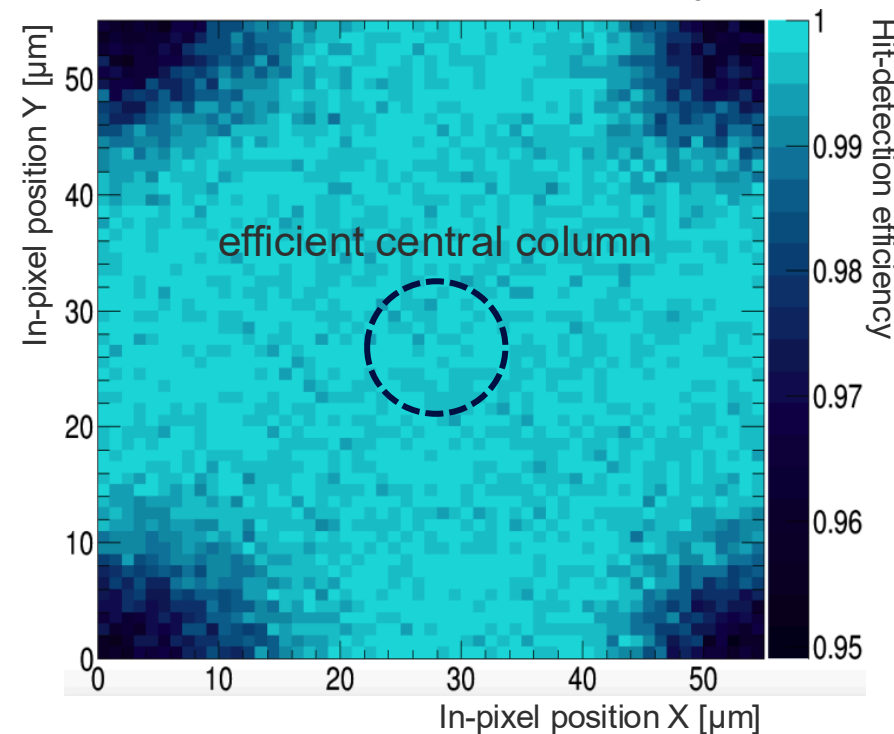
Radiation hardness, timing...



...spatial resolution...



...and detection efficiency



**3D sensors: Proven performance both through simulation and experimental results**

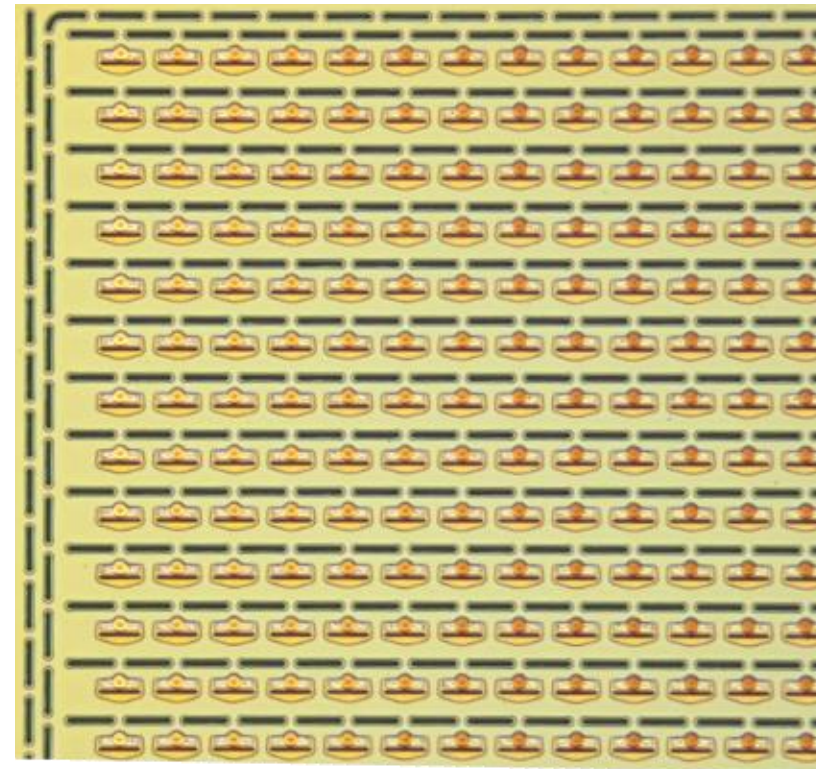
**Design investigation: converging on VELO UII optimised 3D sensor designs**

# 3D sensor production

Production of VELO U11-specific 3D sensor designs with multiple foundries:

## 3D trench (FBK, AIDAInnova)

- Best timing performance, challenging production yields and capacitance
- Hybridisation ongoing, both flip-chip and using anisotropic conductive films (ACF)



*AIDAInnova 3D trench sensors after UBM deposition [2].*

# 3D sensor production

Production of VELO UII-specific 3D sensor designs with multiple foundries:

3D Column (FBK)	3D column (SINTEF)
1E and 323 geometries	
150 $\mu$ m thickness	150 and 230 $\mu$ m thicknesses
Column radius $\sim$ 5 $\mu$ m	Column radii: $\sim$ 4 $\mu$ m and 7-9 $\mu$ m
Foreseen Feb 2026	Foreseen Q4 2026

# 3D sensor production

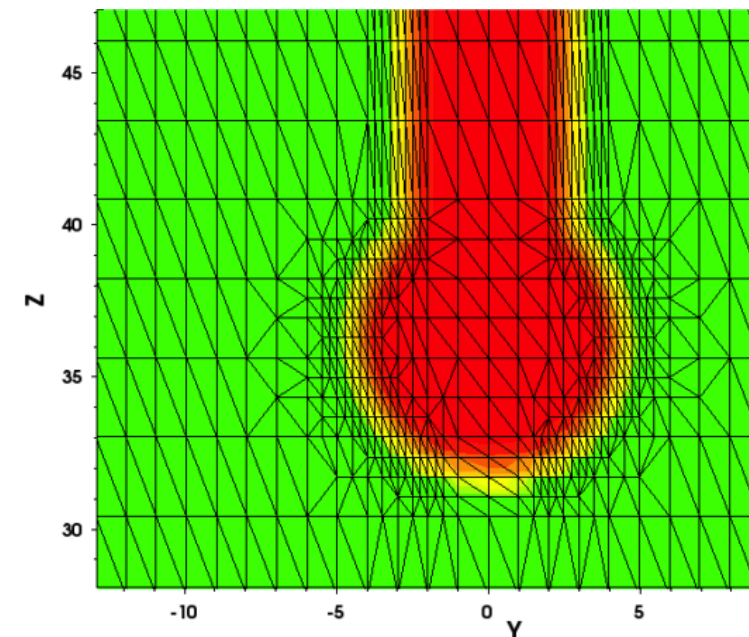
Production of VELO UII-specific 3D sensor designs with multiple foundries:

3D Column (FBK)	3D column (SINTEF)
1E and 323 geometries	
150 $\mu$ m thickness	150 and 230 $\mu$ m thicknesses
Column radius $\sim$ 5 $\mu$ m	Column radii: $\sim$ 4 $\mu$ m and 7-9 $\mu$ m
Foreseen Feb 2026	Foreseen Q4 2026

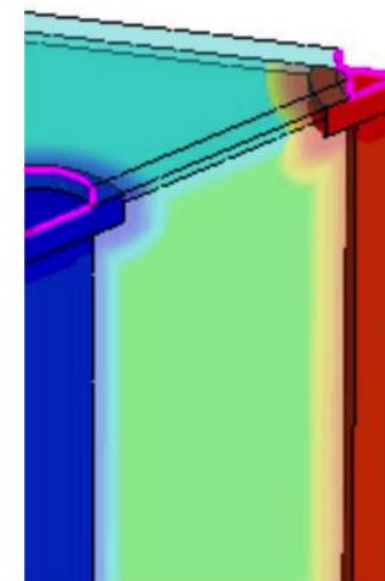


Also includes:

- variants with thinner columns (aspect ratio up to 1:27), for capacitance reduction
- production variants to improve high-voltage tolerance



TCAD simulation of rounded end-of-column geometry for a 3D column sensor [11].



TCAD simulated design of a 3D sensor with varying p-spray layer [10].

# ASIC development

## R&D challenges:

- **Timing** <30ps, with clock distribution jitter <10ps
- **Rate** for the hottest ASIC  $\sim 100\text{Gbs}^{-1}$
- Sufficient and stable **power** per pixel
- **Radiation hard** technology (28nm CMOS)

For timing, clock and power distribution are key difficulties to overcome.

# ASIC development

## R&D challenges:

- **Timing** <30ps, with clock distribution jitter <10ps
- **Rate** for the hottest ASIC ~100Gbs<sup>-1</sup>
- Sufficient and stable **power** per pixel
- **Radiation hard** technology (28nm CMOS)

For timing, clock and power distribution are key difficulties to overcome.

Two ASICs under development; two approaches to meet the same R&D challenges:

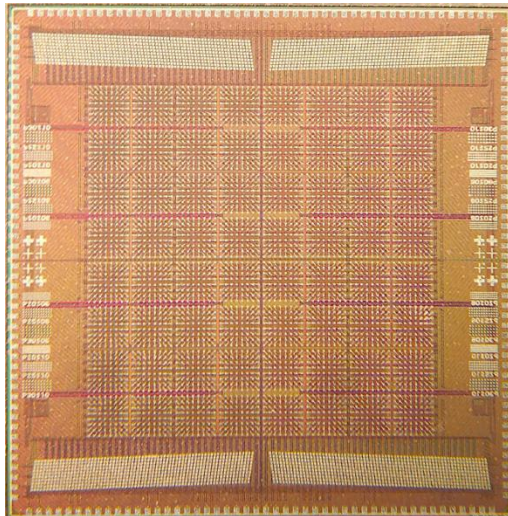
Picopix	IGNITE
50µm pitch	45µm pitch
On-pixel analog power drop compensation Full chip DLL for clock distribution	3D integration: one ASIC for analog, one for digital Eases power and clock distribution design
ASIC in advanced stages of design, with an extensive verification plan being implemented	Analog 64x64 pixel ASIC prototype undergoing characterisation testing; digital design ongoing

# ASIC development

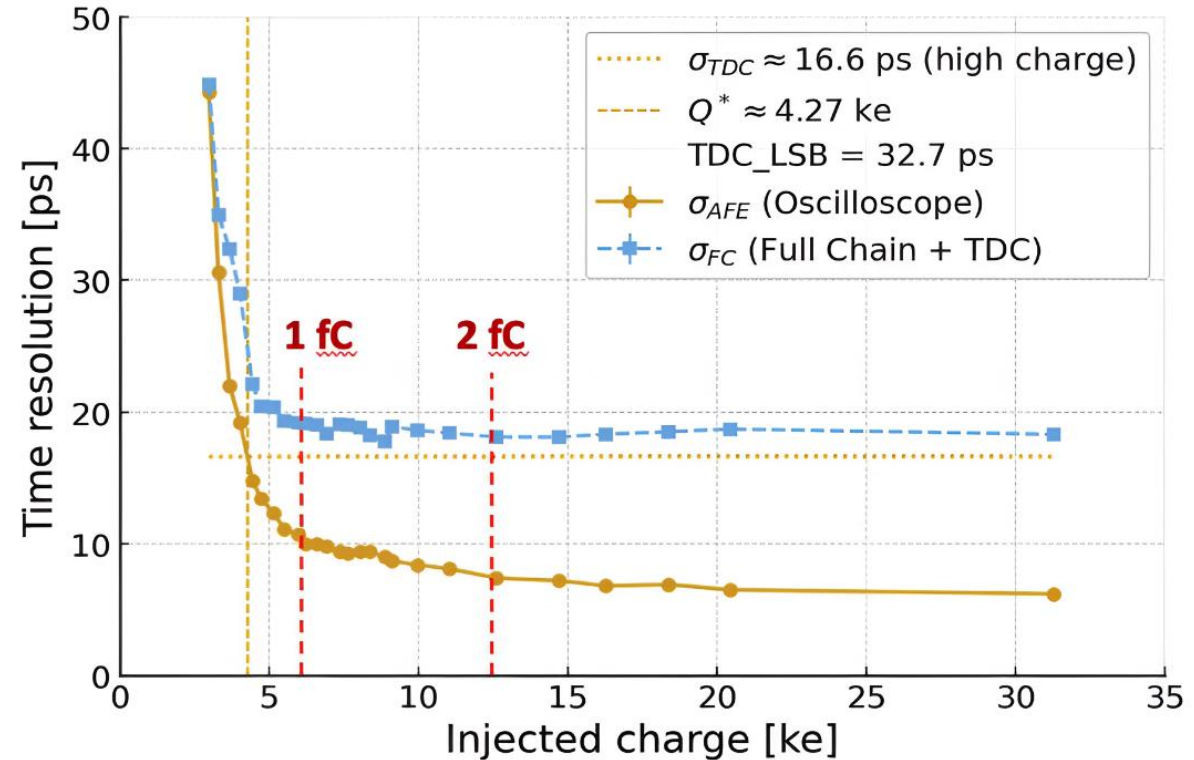
## IGNITE prototype analog ASIC testing

First laboratory tests with internal test pulses:

	$\sigma_t$	$Q_{\text{input}}$	$C_{\text{sensor}}$
Target	<30ps	>6ke <sup>-</sup>	100fF
Achieved	<20ps	≥6ke <sup>-</sup>	0fF



- Uniform response across ASIC
- Tests of assemblies ongoing: prototype ASIC bonded to 3D-trench sensors



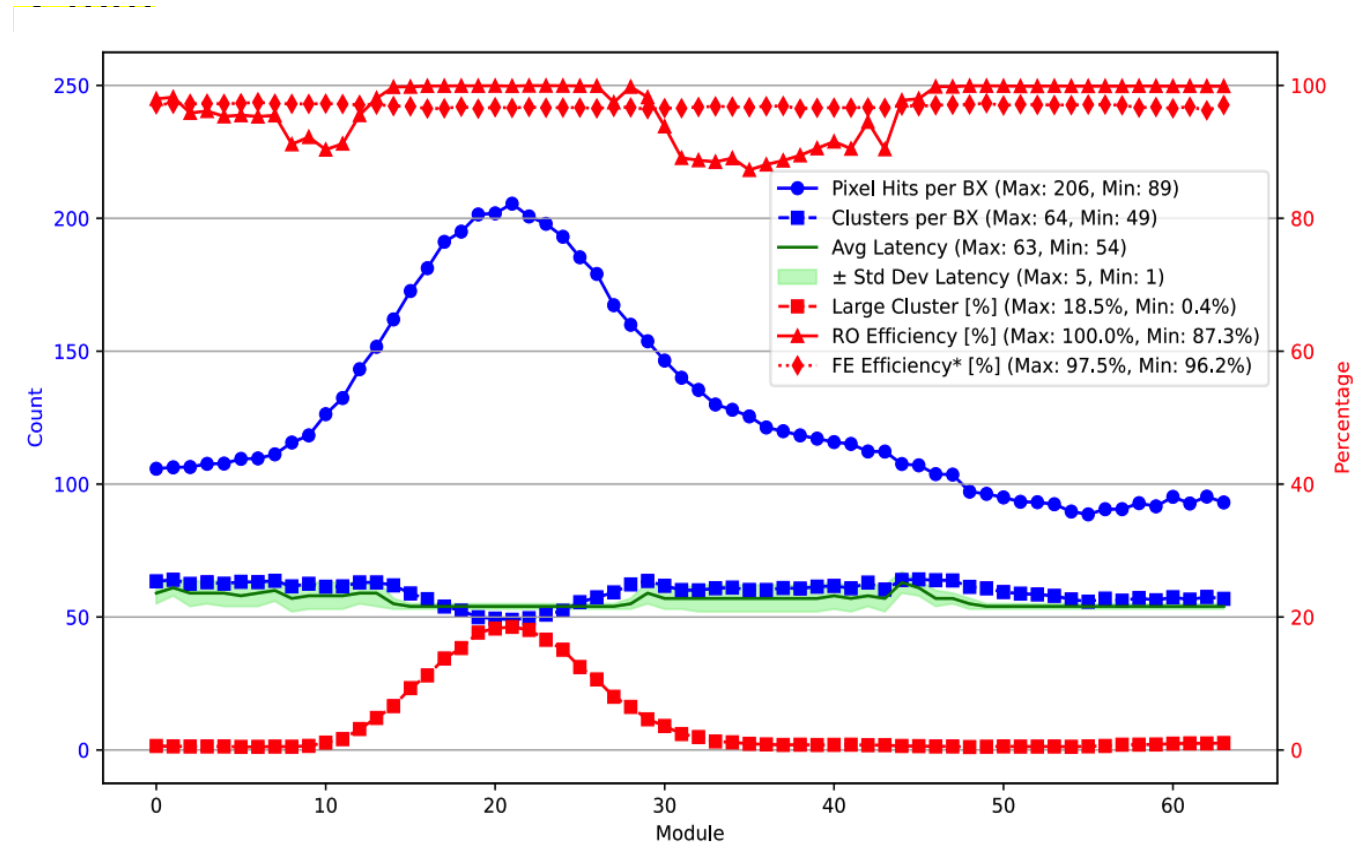
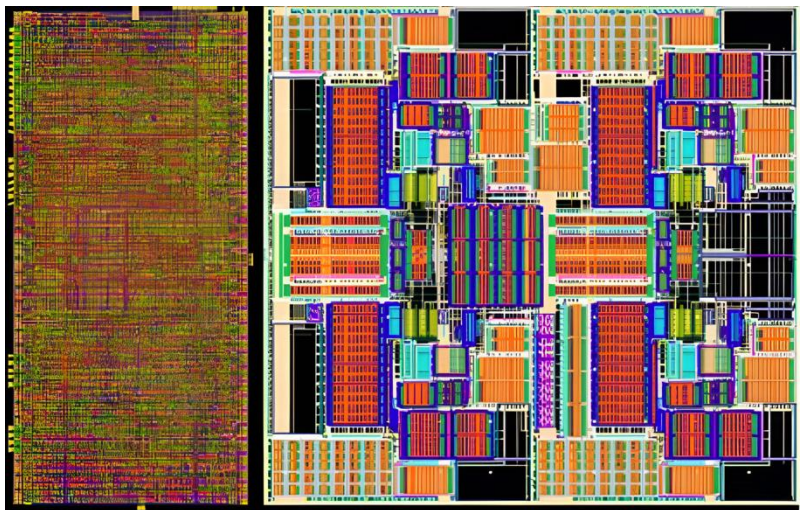
Plot of the time resolution measured by IGNITE prototype analog ASIC when test pulses are injected into the ASIC internally [2] [12].

# ASIC development

## Picopix data rate simulations:

PixESL simulated ASIC bandwidth limitations:

- Simulated VELO UII data at three different module radii
- indicates achievable data rate at 6.2mm radius
- radiation tests will confirm this



\*after VETO

Average Latency: 56

PixESL simulation for a VELO UII detector with a 6.2mm radius [13][14].

# Conclusions

- **VELO UII mechanics, cooling and electronics → see talk by Bhagyashree (5<sup>th</sup> Feb, parallel session-II)**
- **Sensor development: 3D sensors designs investigating for enhanced timing and radiation hardness, while minimising capacitance and maximising high voltage tolerance**
- **Sensor production: Trench and columnar sensors with multiple foundries with UII optimised designs**
- **ASIC development: Picopix and IGNITE**

## Timeline:

- **VELO UII ASIC + sensor assembly testing in 2026**
- **Prototype module in 2027**

# Bibliography

- [1] LHCb UII scoping document: [link](#)
- [2] Progress towards the LHCb Upgrade II Timing VELO, 118<sup>th</sup> LHCb week: [link](#)
- [3] Paper in preparation for 2026 publication
- [4] U2 simulation overview, VELO and VELO UII parallel session, 118<sup>th</sup> LHCb week: [link](#)
- [5] Status and Perspectives of Silicon Detectors: [link](#)
- [6] Timing-Optimised 3D Silicon Sensor with Columnar Electrode Geometry: [link](#)
- [7] Characterisation of 3D trench silicon pixel sensors irradiated at  $1 \cdot 10^{17}$  1 MeV neq cm<sup>-2</sup>: [link](#)
- [8] Development of fast-timing sensors and multichannel characterisation board, VCI2025: [link](#)
- [9] Testbeam results on 3D silicon sensor with the Timepix4 telescope: [link](#)

- [10] 3d simulations at CERN, VELO Upgrade 2 sensors and ASICs meeting: [link](#)
- [11] 3d simulations at Nikhef, VELO Upgrade 2 sensors and ASICs meeting: [link](#)
- [12] ASICs and Sensors, VELO and VELO UII parallel session, 118<sup>th</sup> LHCb week: [link](#)
- [13] Picopix status, VELO Upgrade 2 workshop: [link](#)
- [14] PixESL: a Virtual Prototyping Framework for Pixel Detector Electronics in High Energy Physics, 6th Allpix squared user workshop: [link](#)

Additional info:

- Considerations for the VELO detector at the LHCb upgrade II: [link](#)
- Letter of Intent for the LHCb Upgrade: [link](#)



[home.cern](https://home.cern)