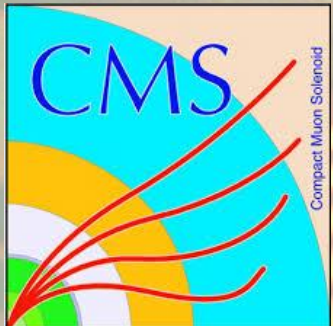


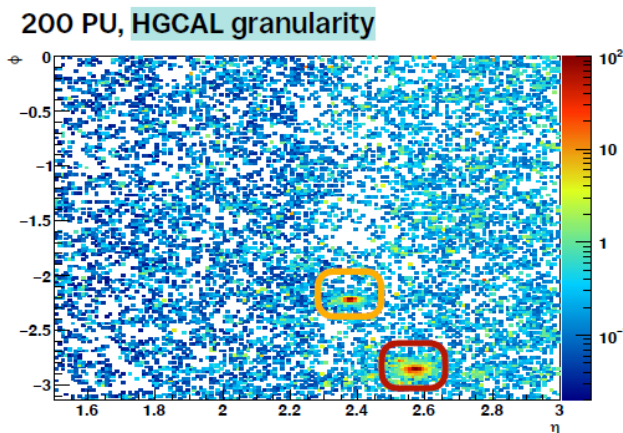
HGCROC3: Radiation-Hard Front-End ASIC for the CMS HGICAL

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T. Fiutowski, J. Gonzalez, F. Guilloux, M. Idzik, C. de La Taille, A. Marchioro, J. Moron, L. Raux,
K. Swientek, D. Thienpont, T. Vergine

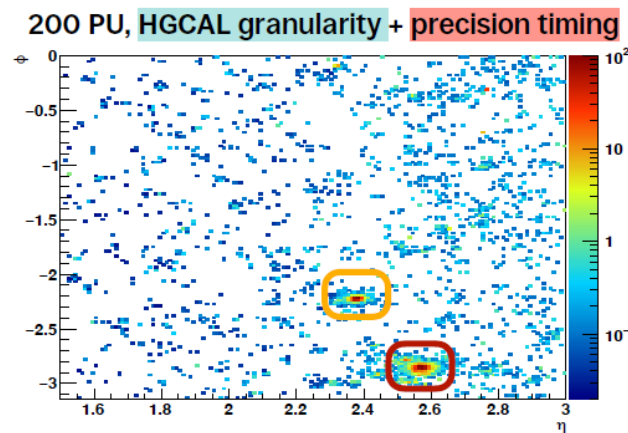
February 5, 2026



- The High-Granularity Calorimeter will replace the existing endcap calorimeters of CMS detector for the High-Luminosity phase of LHC
 - Silicon-based modules for electromagnetic (CE-E) and part of the hadronic (CE-H-Si) section
 - Plastic scintillators tiles for the low-radiation hadronic section (CE-H-SiPM)
- Timing measurement for **pile-up mitigation** and **vertex location**



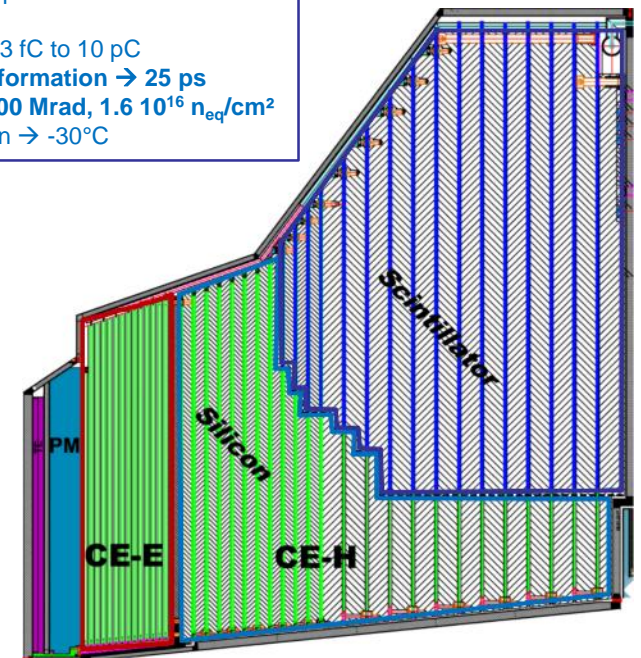
HGCAL TDR



Target for timing performance: resolution of 30ps

Electronics requirement

- 6M channels and 100k chips
- Low noise $\rightarrow \sim 0.3$ fC
- Wide dynamic range $\rightarrow 0.3$ fC to 10 pC
- High precision timing information $\rightarrow 25$ ps
- High radiation level $\rightarrow 200$ Mrad, $1.6 \cdot 10^{16}$ n_{eq}/cm²
- Low temperature operation $\rightarrow -30^\circ\text{C}$



Overall chip divided in two symmetrical parts

- 1 half is made of:
 - 39 channels: 18 ch, CM0, Calib, CM1, 18 ch (78 channels in total)
 - Bandgap, voltage reference close to the edge
 - Bias, ADC reference, Master TDC in the middle
 - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

Measurements

- Charge
 - ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
 - TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
 - ADC: 0.2 fC resolution. TOT: 2.5 fC resolution
- Time
 - TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

Two data flows

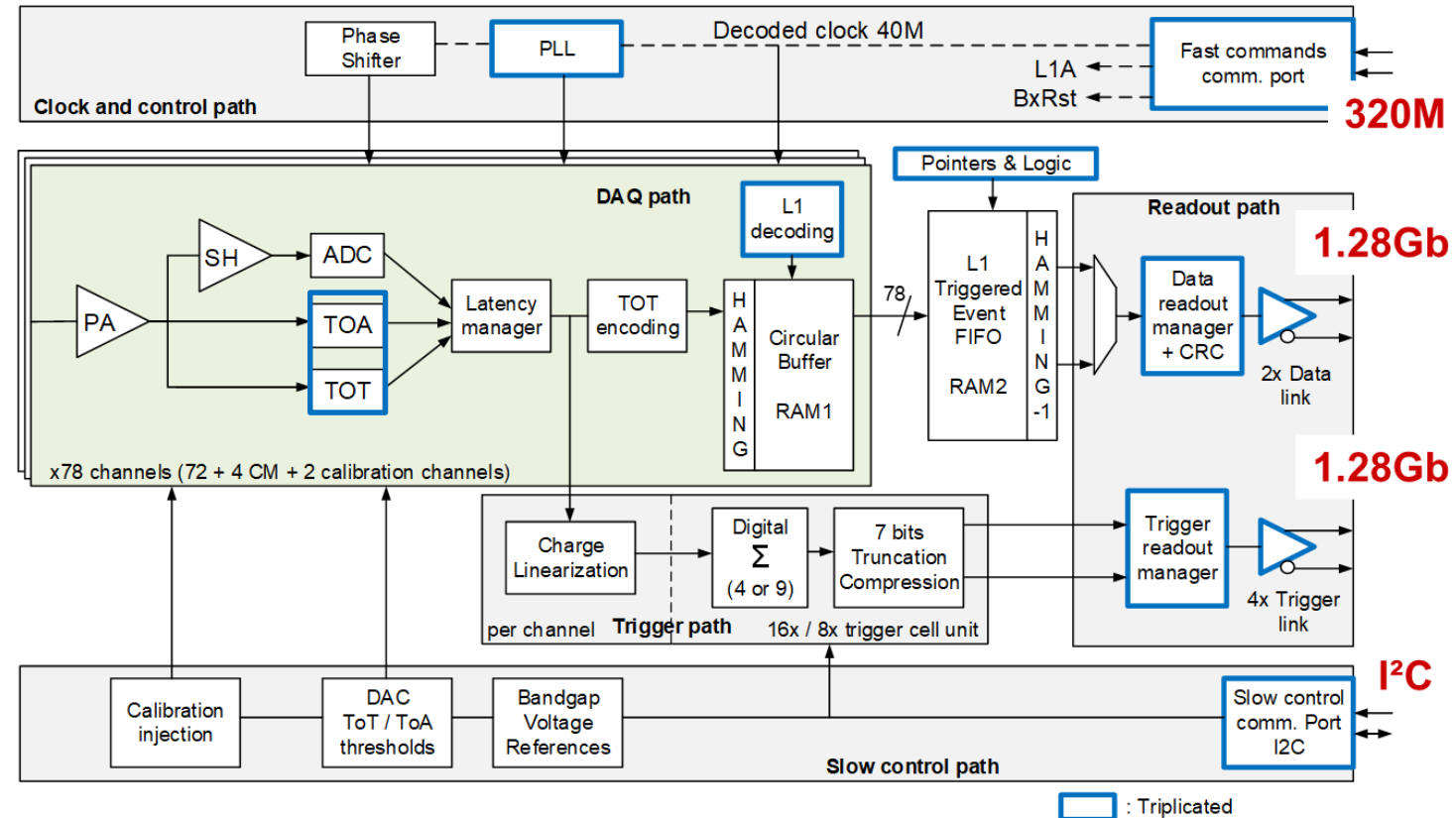
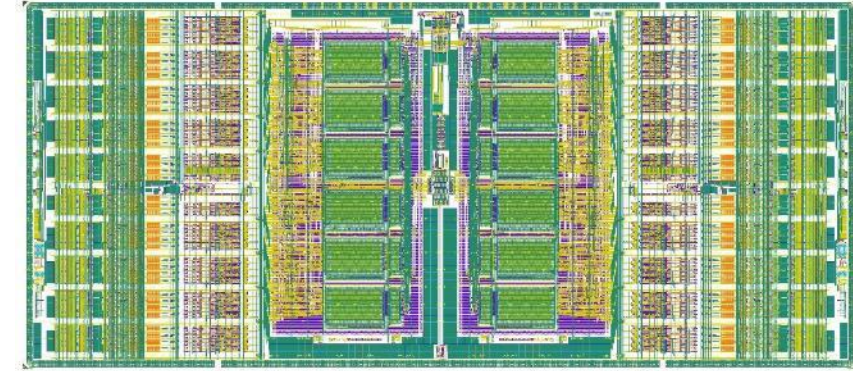
- DAQ path
 - 512 depth DRAM (CERN), circular buffer
 - Store the ADC, TOT and TOA data
 - 2 DAQ 1.28 Gbps links
- Trigger path
 - Sum of 4 (9) channels, linearization, compression over 7 bits
 - 4 Trigger 1.28 Gbps links

Control

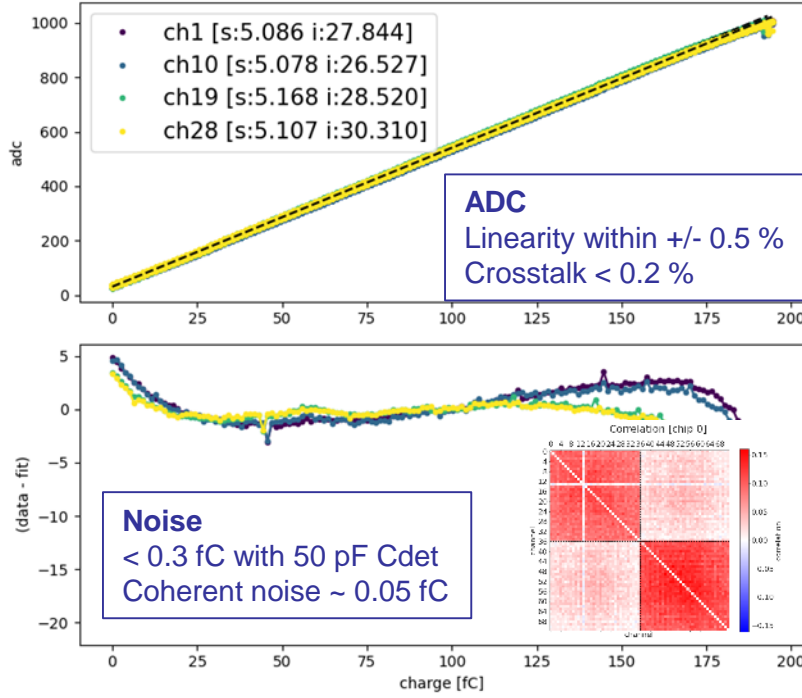
- Fast commands
 - 320 MHz clock and 320 MHz commands
 - A 40 MHz extracted, 5 implemented fast commands
- I2C protocol for slow control

Ancillary blocks

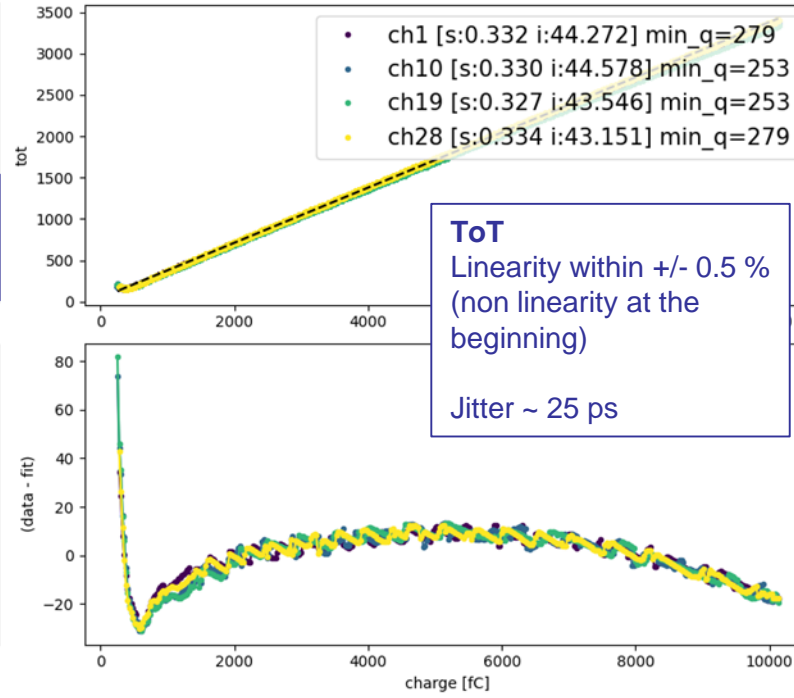
- Bandgap (CERN)
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL (IRFU)
- Adjustable phase for mixed domain



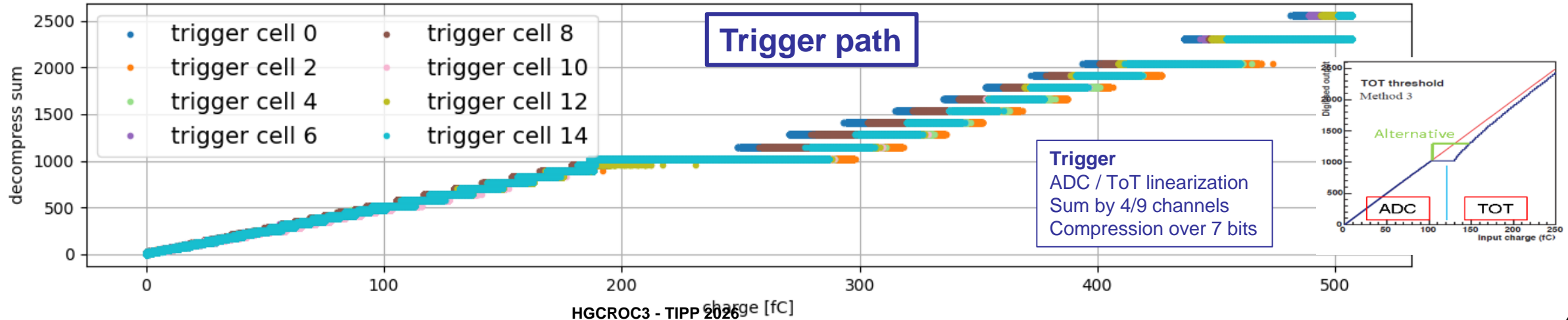
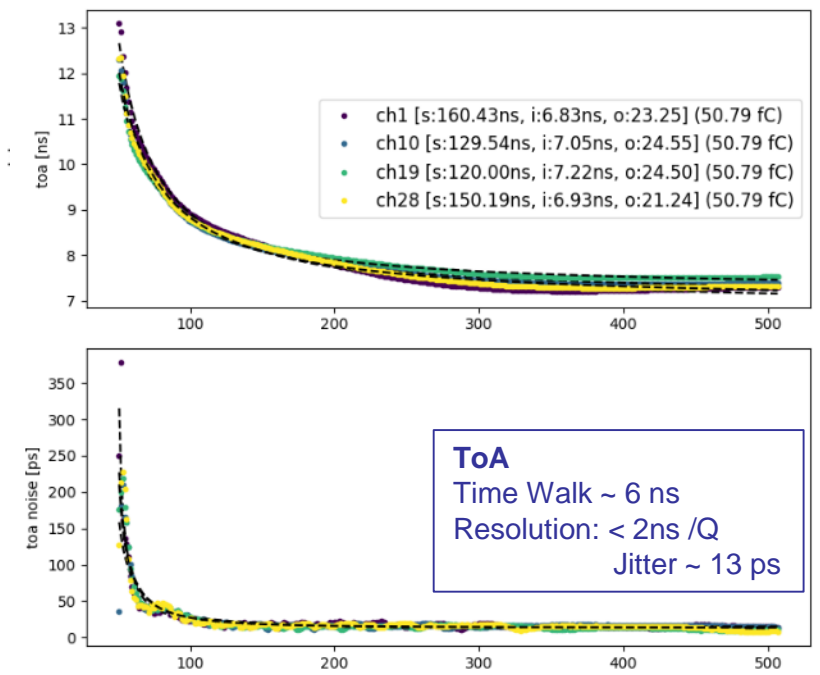
ADC



ToT



ToA



The time resolution is limited by several factors:

- **Jitter: electronic noise and signal slope:** the noise is superimposed on the signal, leading to amplitude fluctuations and thus time uncertainty

$$- \sigma_t^{elec} = \frac{\sigma_v^{elec}}{dV/dt} = \sim \frac{e_n C_d}{2Q} \sqrt{\tau_p}$$

- Time measurement performed after the preamplifier rather than after the shaper

- Noise decreases as $\sqrt{\tau}$, signal slope increases with $1/\tau$

- Low-noise, large gain-bandwidth product ($G_0 \omega_0$)

- $\tau_p = \sim \frac{C_d}{G_0 \omega_0 C_f}$

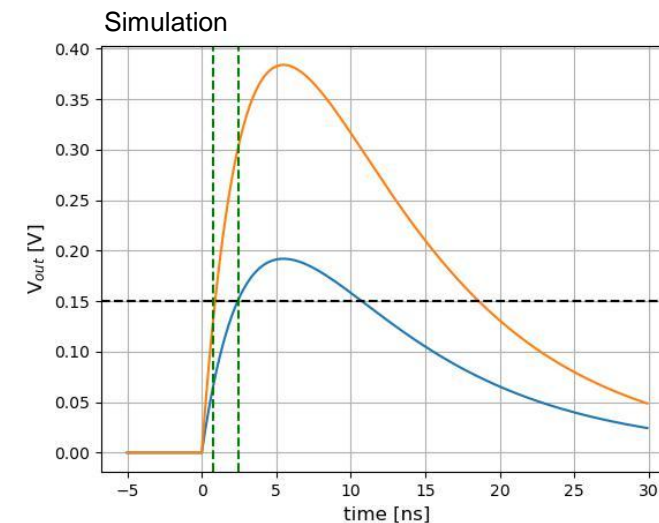
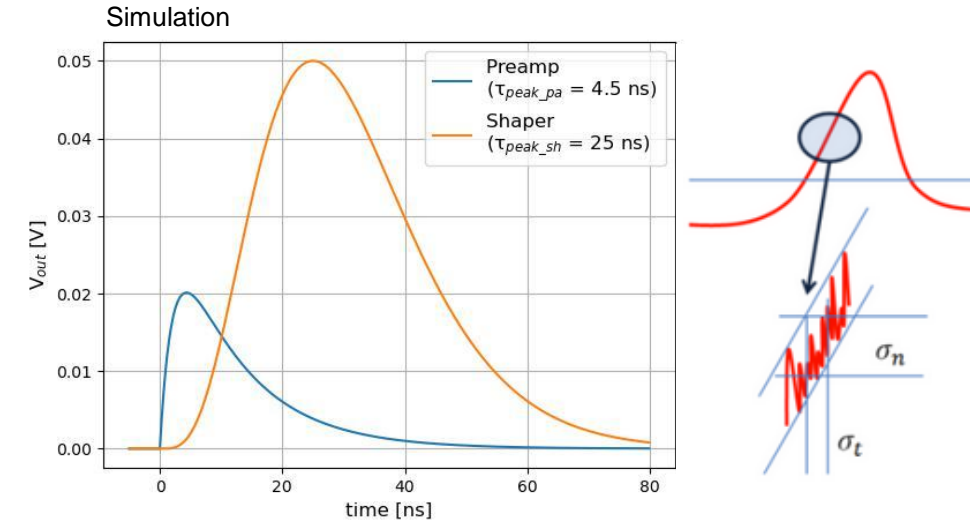
- $G_0 = 100 \text{ dB}_{20}$, $f_0 = 50 \text{ kHz}$, $C_d/C_f = 100$ and $e_n = 0.7 \text{ nV}/\sqrt{\text{Hz}}$
 $\rightarrow \sigma_{elec}(10fC) = \sim 100 \text{ ps}$, $\sigma_{elec}(100fC) = \sim 10 \text{ ps}$

- **Time Walk correction:** the threshold voltage V_{th} is reached at different times for signals with different amplitudes

$$- TW = -\tau_p \ln\left(1 - \frac{C_f * V_{th}}{Q}\right)$$

- **TDC resolution and PLL clock jitter**

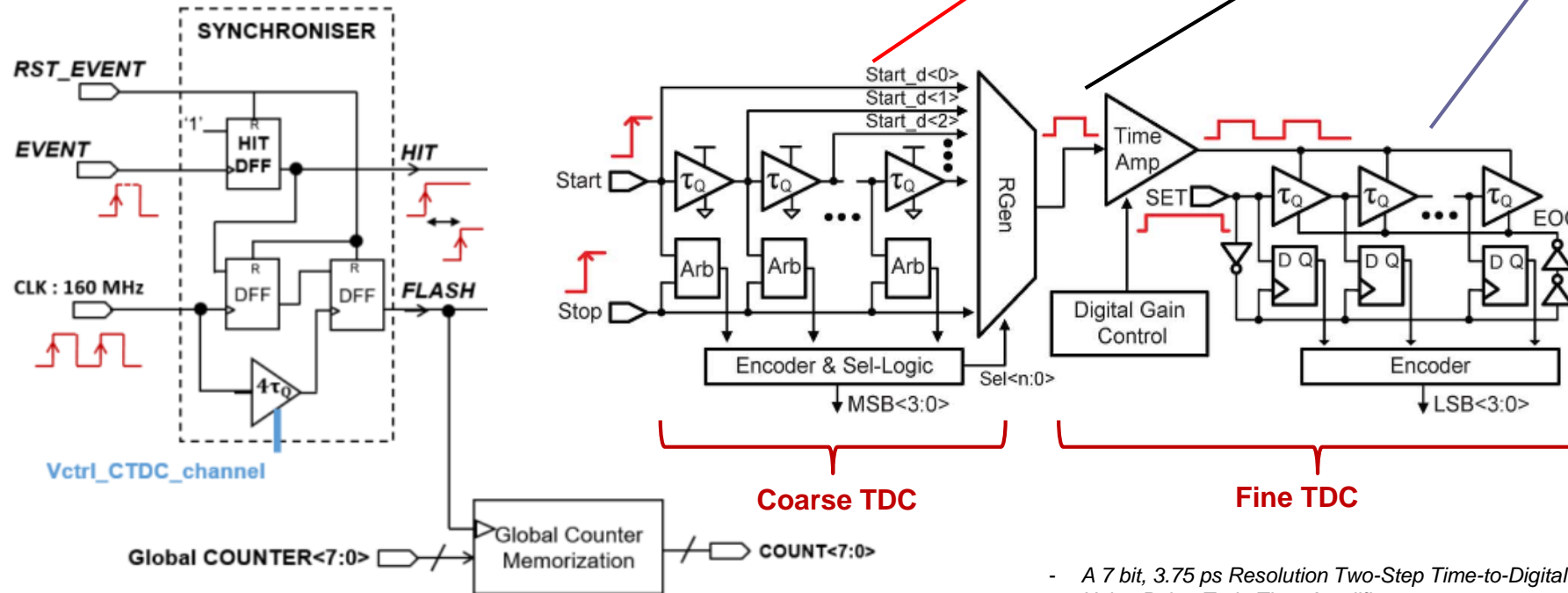
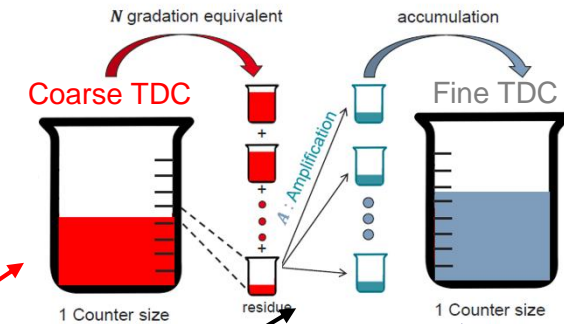
$$\sigma_t^2 = \sigma_{elec}^2 + \sigma_{TW}^2 + \sigma_{TDC}^2 + \sigma_{clk}^2$$



The TDC is based on 3 sub-blocks providing each a time resolution

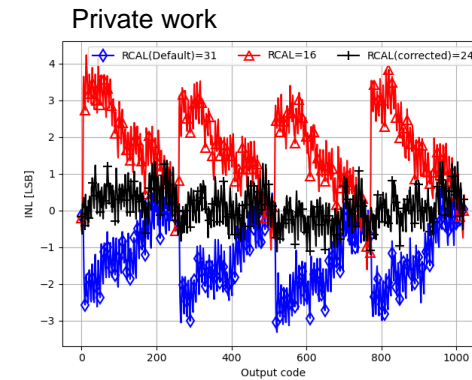
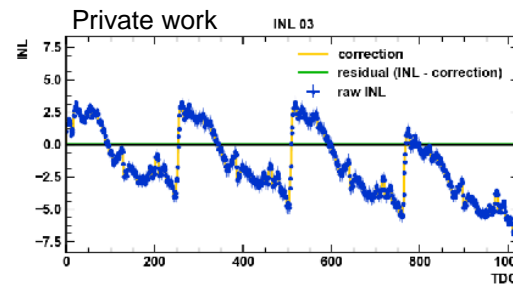
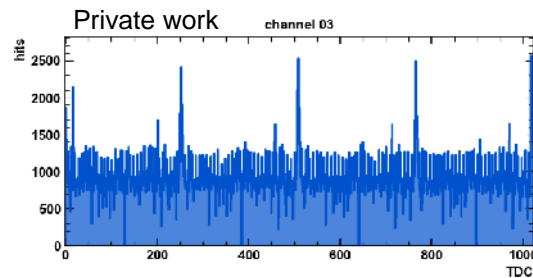
- Asynchronous counter running at 160 MHz: **LSB = 6,25 ns**
 - Synchroniser: remove metastability between event input and clk_160M
- 5 bits Coarse TDC: classic delay line, **LSB = 195 ps**
 - Low power, Vctrl made in a common Master TDC block
 - Residual time amplifier
- 3 bits Fine TDC: delay line, **LSB = 24.4 ps**
 - Measurement of the amplified residual time

ToA 10b-TDC: BX time-stamping + 25 ns dynamic range, 25 ps resolution

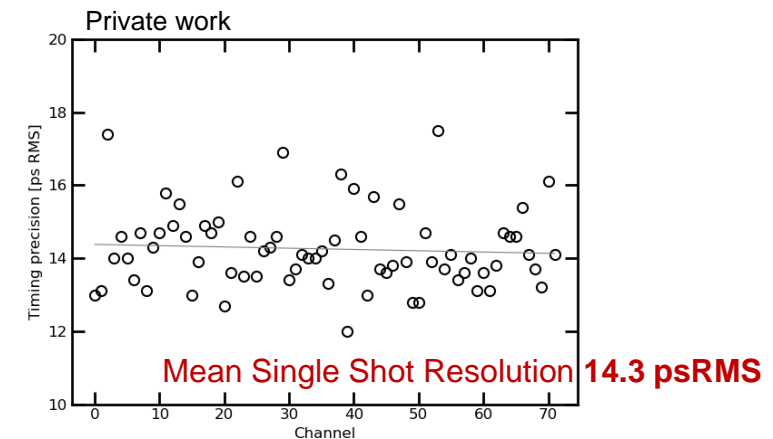
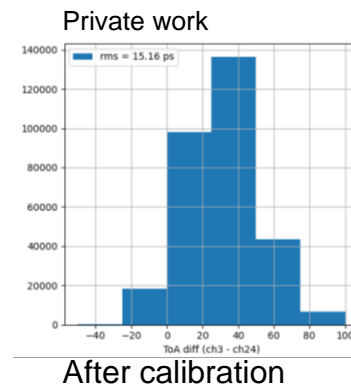
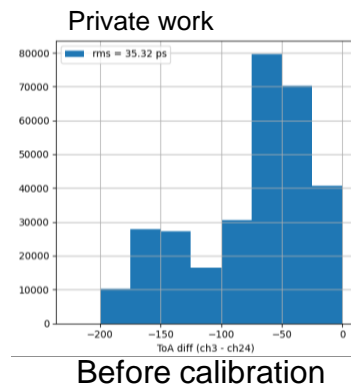


- A 7 bit, 3.75 ps Resolution Two-Step Time-to-Digital Converter in 65 nm CMOS Using Pulse-Train Time Amplifier
- A 3-step Low-latency Low-Power Multichannel Time-to-Digital Converter based on Time Residual Amplifier

- Inter-calibration of the three TDC sub-blocks is required to achieve good linearity and therefore optimal performance
- An on-chip asynchronous clock generator is integrated to perform this calibration
 - Code distribution → INL and DNL extraction
 - Coarse and Fine TDC calibrations are performed by adjusting a control voltage at both chip and channel levels

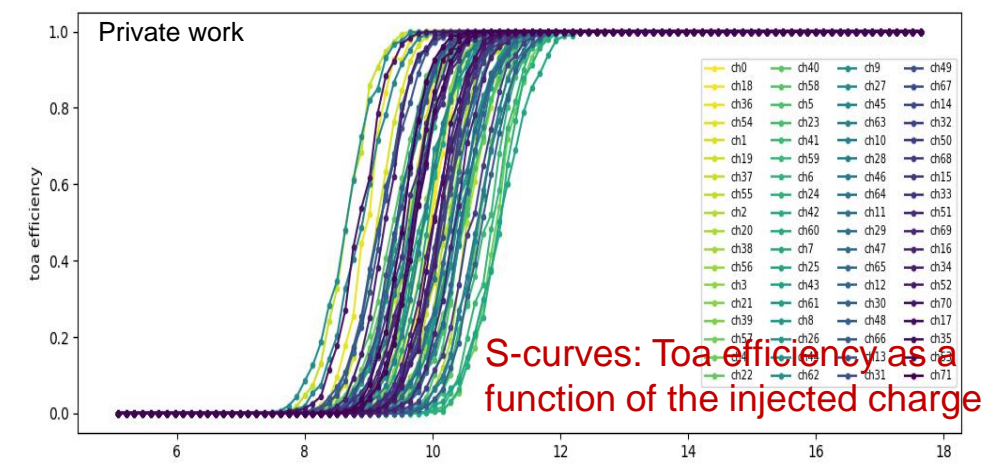
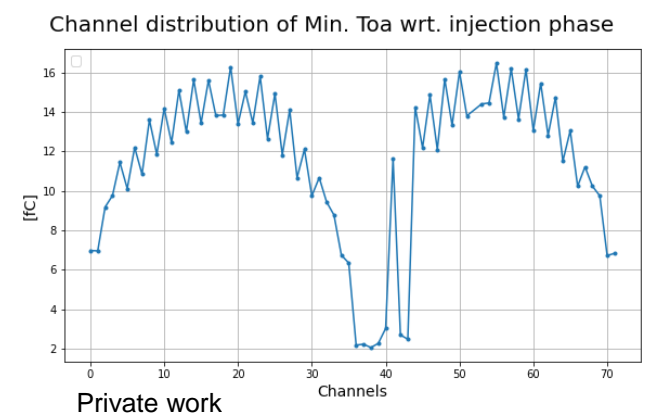


- The TDC performance was evaluated by injecting an asynchronous signal into two channels (Δt from 0 to several ms)



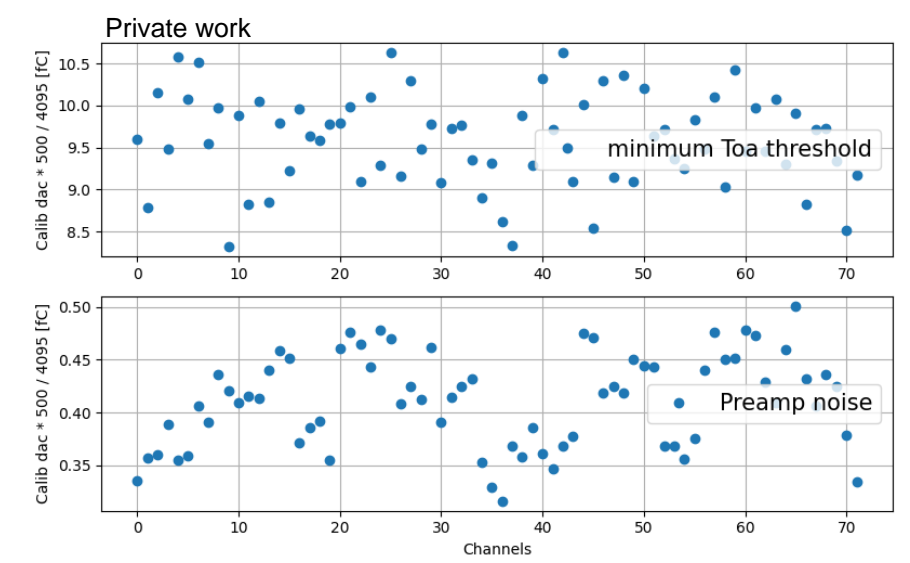
Minimum ToA threshold

- Minimum ToA threshold after alignment around 10 fC
 - Low dispersion, below 2 fC
- 0.5 fC electronics noise at the preamp output → minimum Toa threshold should be just higher than 2,5 fC
 - 8 fC is the best we achieved
 - Minimum toa threshold > 5 * noise → digital noise
- A 40 MHz coupling component is added to the preamplifier signal, altering its waveform
 - As a result, both the minimum ToA threshold and the time walk become phase-dependent with respect to the digital clock



From gaussian fit

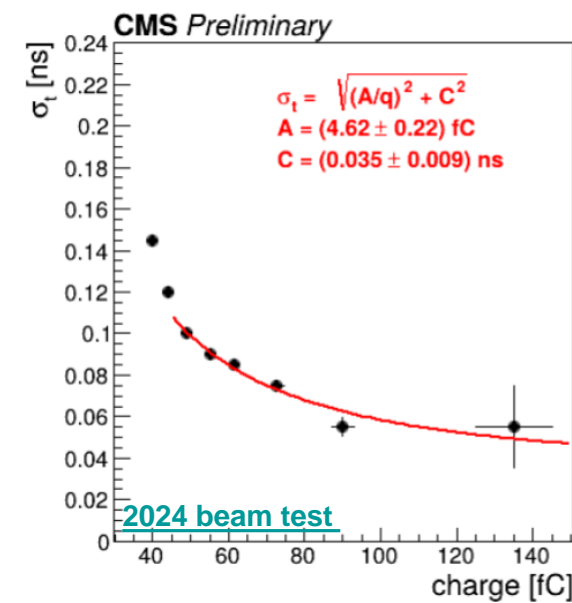
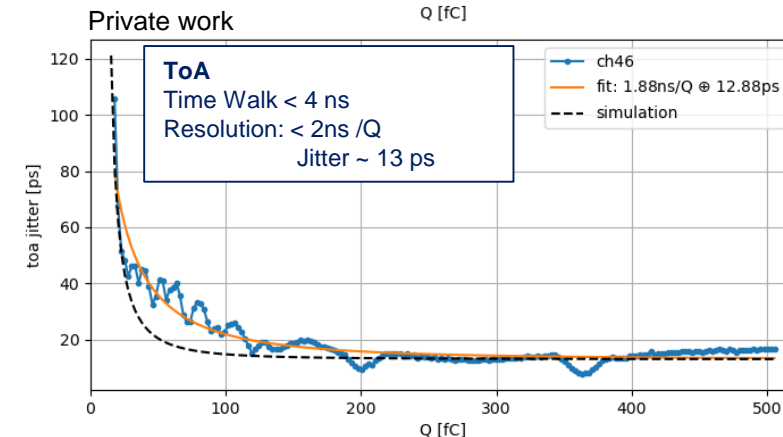
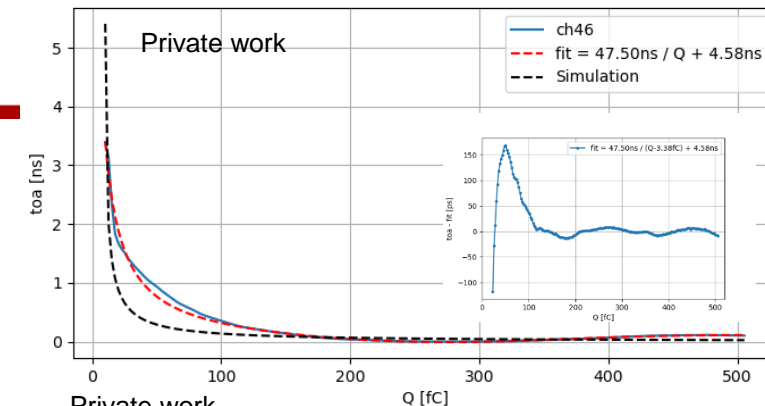
- Mean → minimum toa threshold
- Sigma → electronics noise at the preamp output



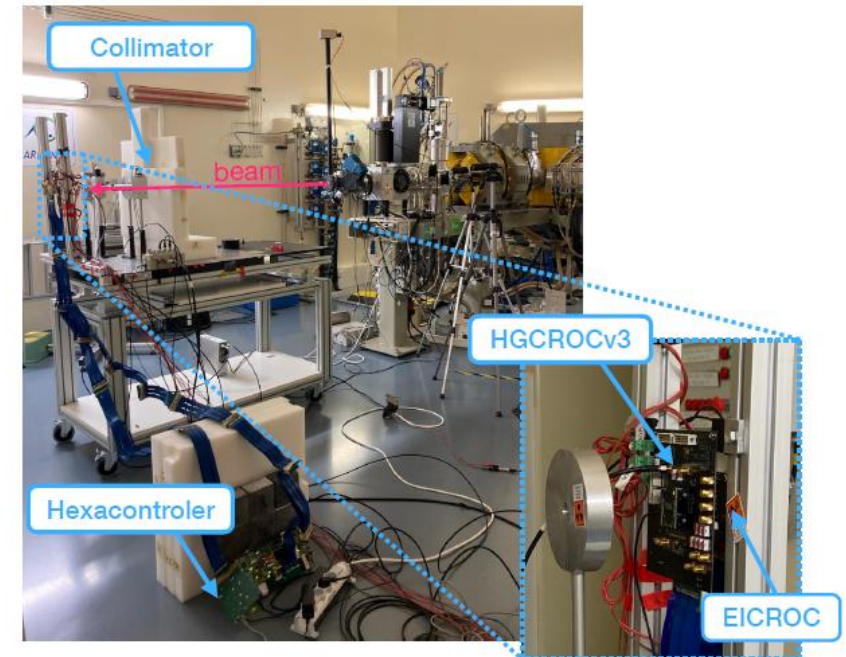
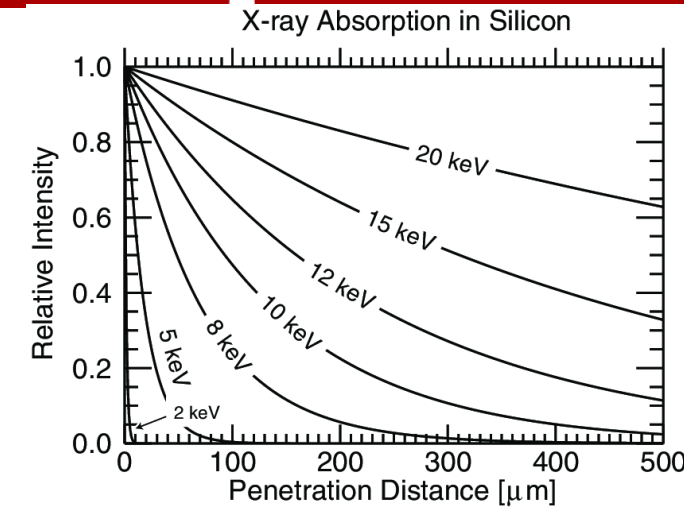
HGCROC: timing performance

The time measurement resolution depends on several factors:

- Jitter: 13 ps constant term
 - Distribution of internal clocks (PLL and TDC clocks) and intrinsic resolution of the TDC itself
- Time-Walk correction
 - A good first-order agreement is observed between measurements and simulations
 - The time walk is below 4 ns, with some deviations from an ideal simulation
 - Deviations can be attributed to
 - Digital coupling, which distorts the preamplifier signal
 - The effect of full preamplifier saturation in ToT mode
 - The impact of the interconnection between the preamplifier and the sensor cell
 - Time-walk correction must also be derived from real data (laser measurements and beam tests)
 - 35 ps constant term in beam test



- The chip have been tested against **TID** up to 345 Mrad
 - CMS forward region will be exposed to a total integrated dose of up to ~ **200 Mrad**
 - Must be thinned down to ~ 70 μm , at room temperature and -10 $^{\circ}\text{C}$
 - **No big impact** observed on any part of the chip
- **Heavy ions** in Louvain, Belgium
 - 1 campaign in 2022
 - No I2C failures, no SEL
- **Proton** irradiation campaigns at *Arronax* in Nantes, France
 - *More than 7 campaigns*
 - *Beam*: 70 MeV protons, flux from 10^8 to 10^{11} p/cm²/s
 - **HGCAL** radiation environment dominated by light hadrons
 - more **realistic** description of the HGCROC3 behaviour with proton
 - higher flux and more error **statistics**



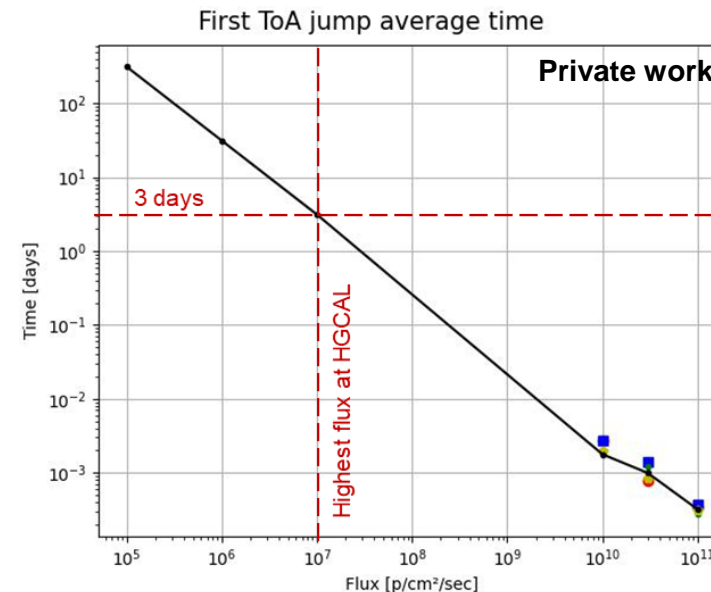
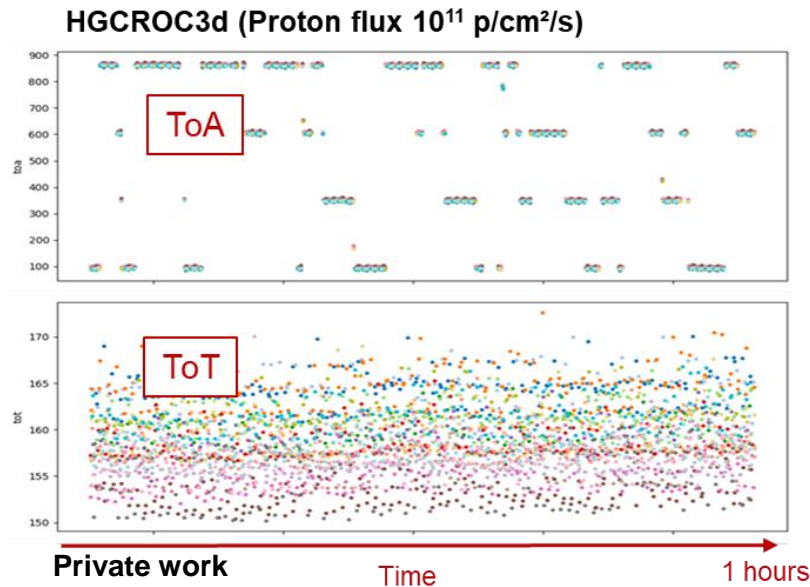
- **Heavy ions results**

- No Single-Event Latchup
- No I2C configuration error

- **Protons results**

- Robust triplicated logic and acceptable SEU rate in non-triplicated logic and data
- ToA jumps observed at higher rate, can be restored by an I2C transaction (100 μ s)
 - Jump magnitude pointed to the asynchronous counter responsible for the 2 most significant bits
 - ToA jumps cross-section $4.10^{-13} \text{ cm}^{-2}$
- average first ToA jump time about 3 days in the worst section of HGICAL (for 1 chip but without I2C reset)

Category	Time [s]	# Errors	Cross Section [cm^{-2}]	HGCAL Rate [s^{-1}]
I2C configuration	108 000	< 1	$< 4.2 \times 10^{-16}$	$< 1.01 \times 10^{-4}$
Triplicated Logic	62 639	< 1	$< 7.26 \times 10^{-16}$	$< 1.74 \times 10^{-4}$
Non-triplicated logic	340	30	4×10^{-12}	0.8
Trigger data	34	38	5×10^{-11}	10.16
DAQ memory	4 352	127	1.33×10^{-12}	0.318



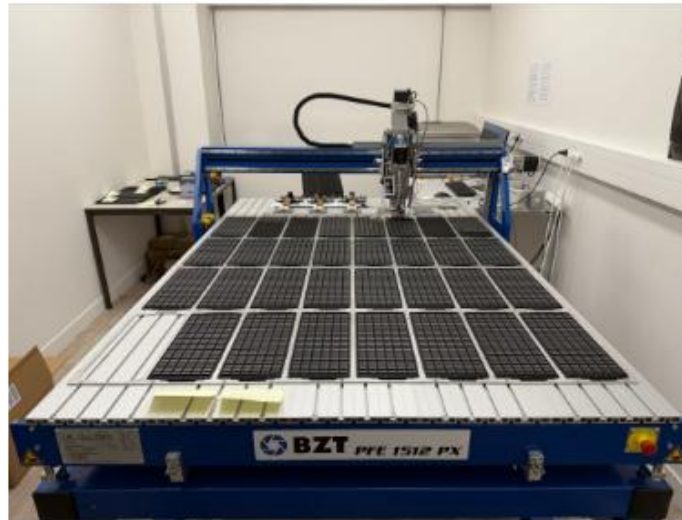
- Time measurement is a key feature for HGICAL, as it is essential to mitigate the impact of pile-up and to enable accurate event reconstruction
 - This requires a high-performance front-end and TDC, as well as a low-jitter clock distribution
 - A time resolution of 13 ps is achieved using internal charge injection
 - Time-walk effect remains the most challenging to correct while maintaining time resolutions at the level of a few tens of picoseconds
 - highly sensitive to the system environment, including digital noise, saturation effects and calibration
- The HGCROC3 chip is now in the production phase
 - Two robots are now running every days to test the 100k chips required for HGICAL

- 2 robots: LLR and OMEGA
 - **High Density** (HD) and **Low Density** (LD) packages, QR code printed on package for tracking
 - 120k chips in total: 36k HD Si / 84k LD Si / 4.3 k LD SiPM
- Production quantity is based on ~ 80 % yield
- The effective yield varies between 85% and 92% depending on the runs
 - It was far below at the beginning because of a lot of crashes, poor socket connection, etc
- The two robots are now running every days

LLR robot (LD)



OMEGA robot (HD)



Chip LD



Chip HD

- Production quantity is based on ~ 80 % yield
- The effective yield varies between 85% and 92% depending on the runs
 - It was far below at the beginning because of a lot of crashes, poor socket connection, etc
- The two robots are now running every days
- Main cause of failures
 - 1 bad channels: ADC and/or TDC
 - Consecutives noisy channels: packaging issue
 - 1 bad half-chip because of something wrong in the bias
 - Surprisingly, bad I2C parameter default values

