

External VMM3a Readout for the Straw Trackers

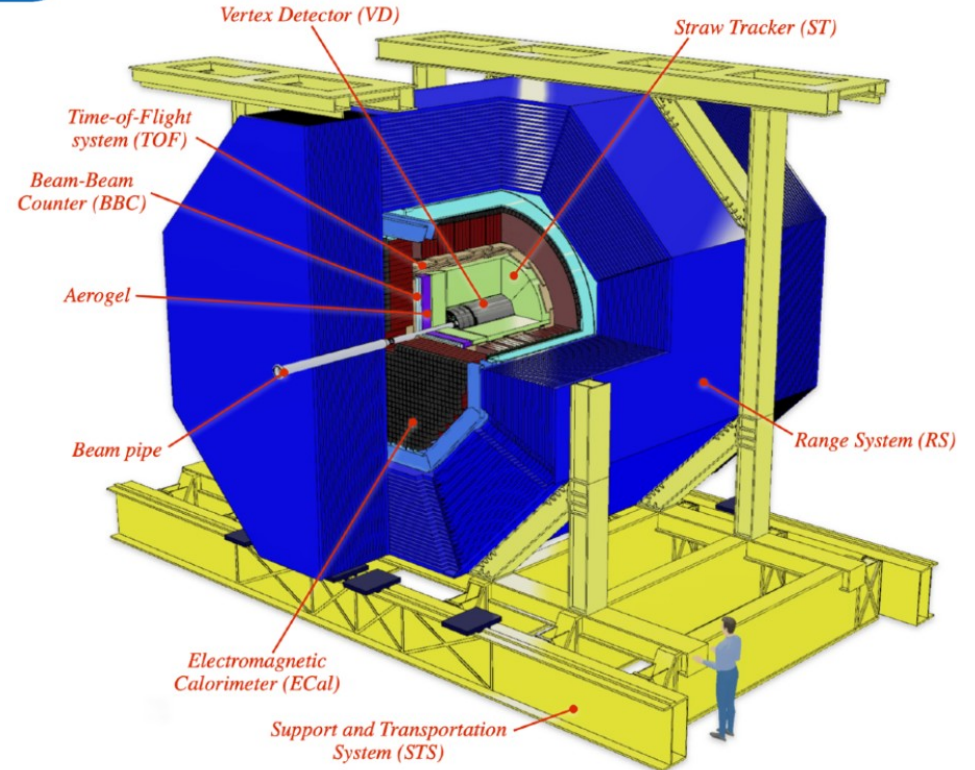


Motivation:



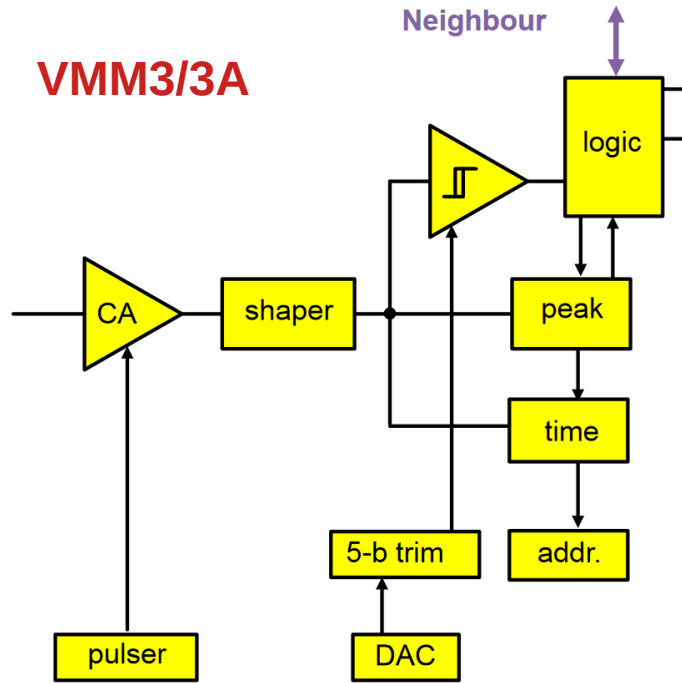
- 30k+ channels
- 150um spatial resolution
- dE/dX charge resolution
- Simultaneous Charge & Time measure

A dedicated R&D is ongoing to study the possibilities for STT Front-End Electronics (FEB) solution.



VMM3a FEE Prototype

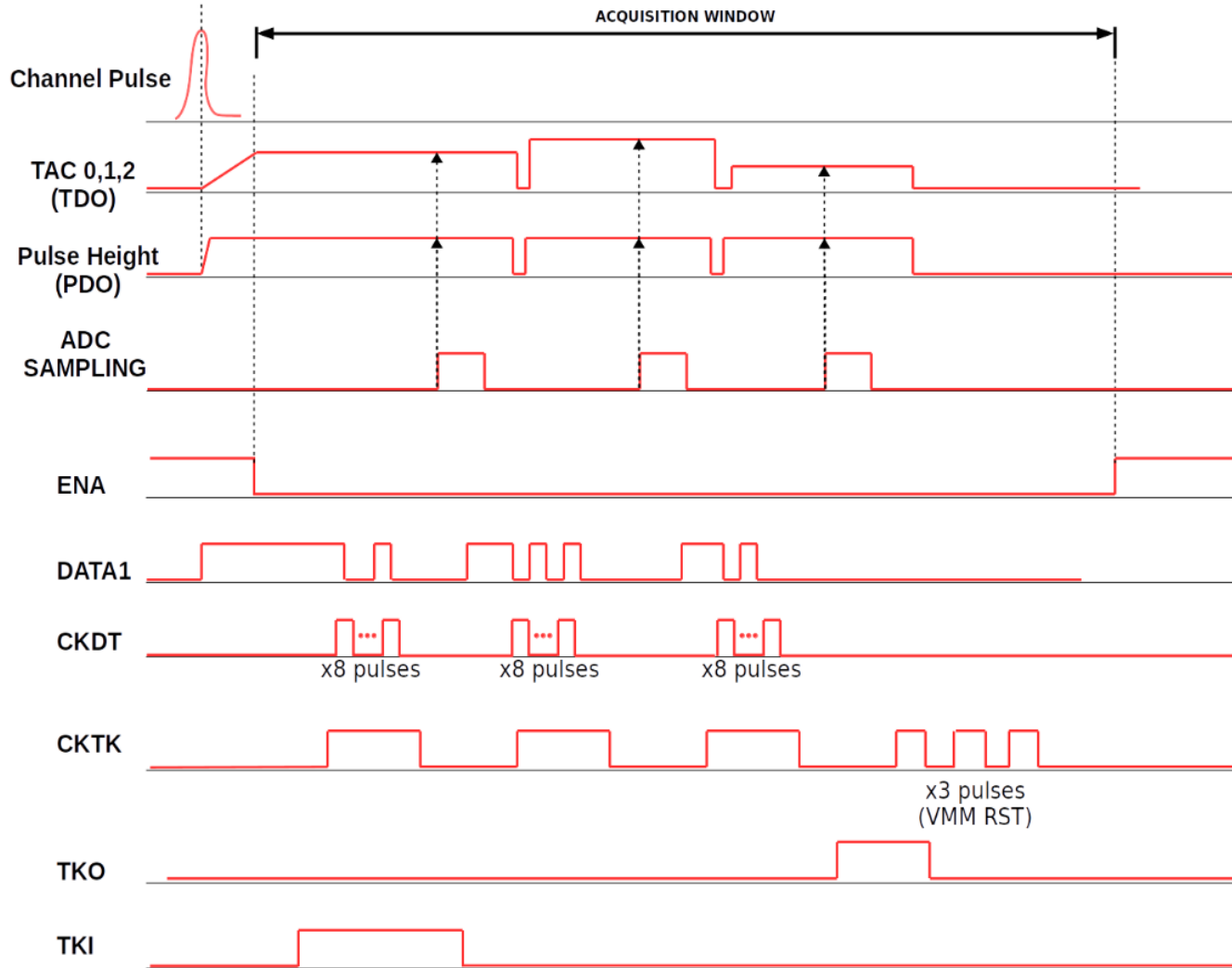
Investigating existing readout solutions



Number of channels	64
Clock frequency	10...80 MHz
Input capacitance	<300 pF
Dynamic range	up to 2 pC
Gain	0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC
Peaking time	25 / 50 / 100 / 200 ns
ENC (energy branch)	<3000 e ⁻
TDC binning	~1 ns
Maximum event rate	140 kHz/ch
Consumption	15 mW/ch

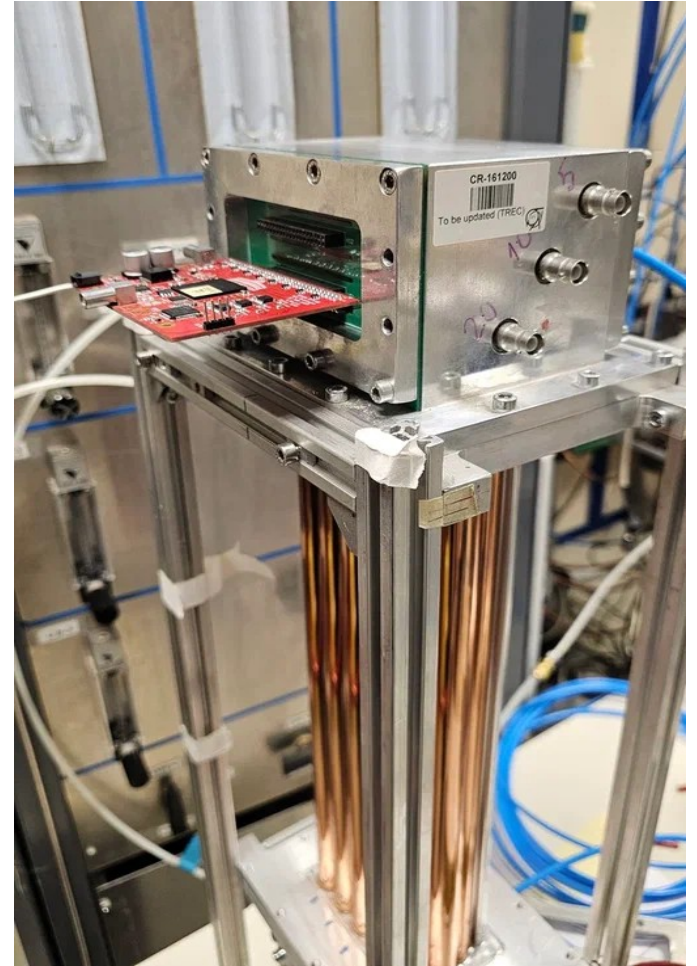
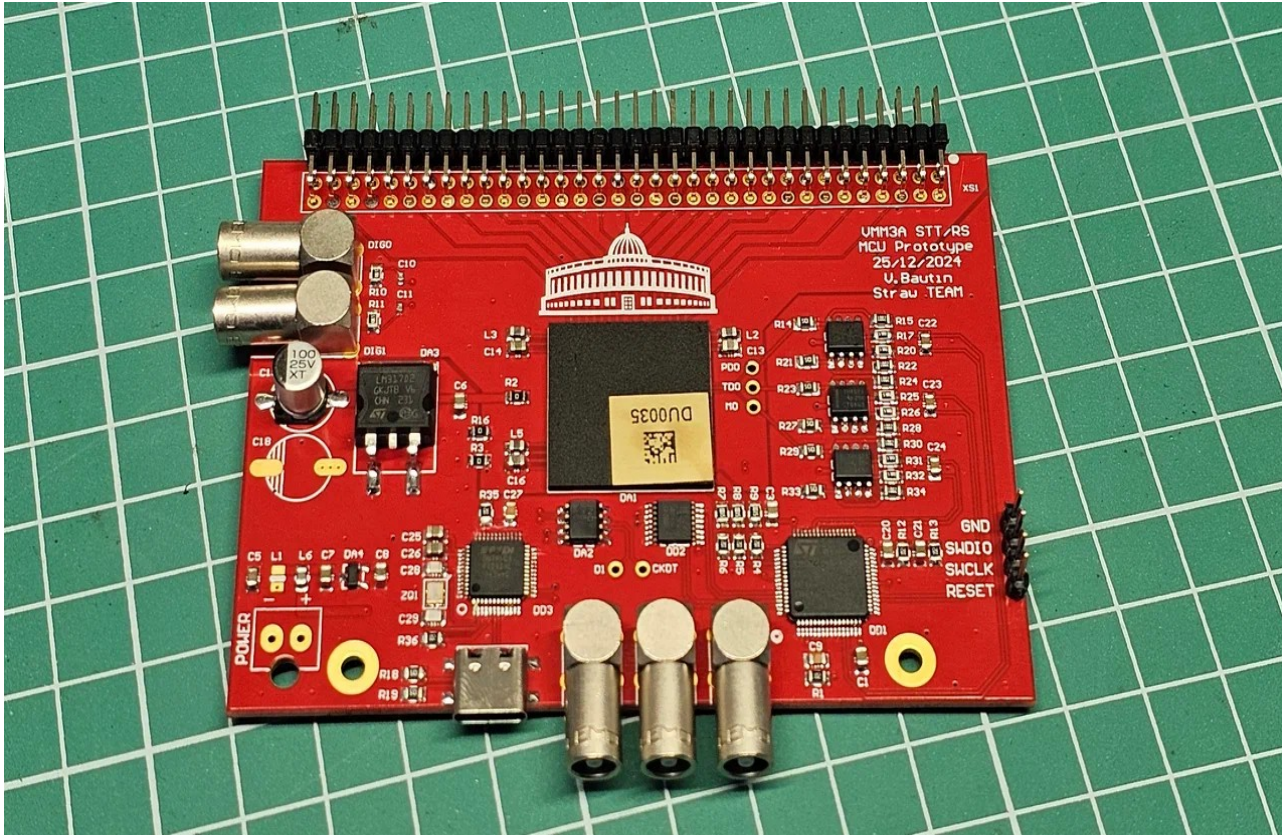
VMM3/3A ASIC is well known chip for gaseous detectors. It has amplifier and shaper adjustable in a wide range. But it was not really done for the timing measurements so fastest shaping is 25ns and ToA mode has some issues.

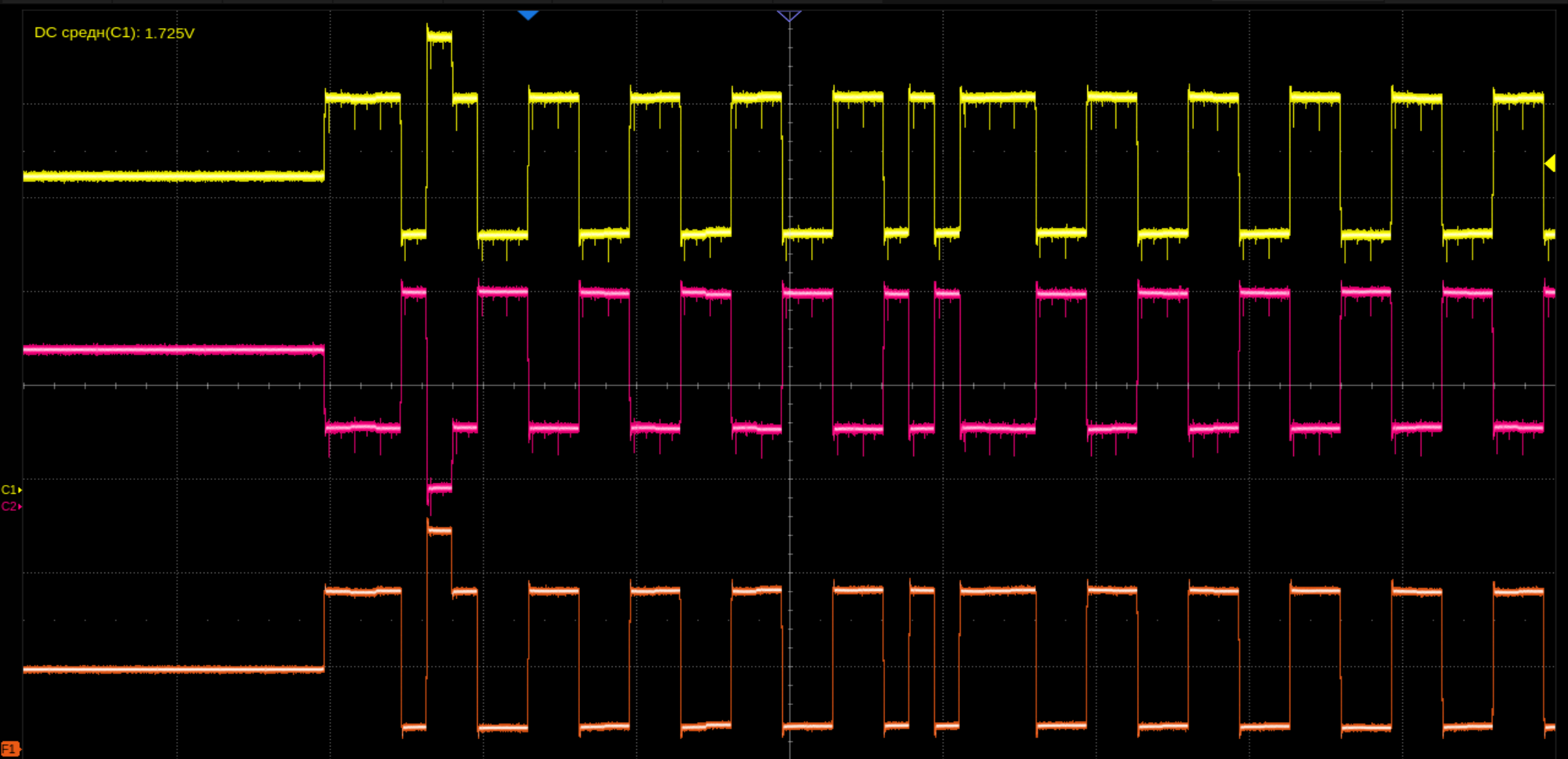
VMM3 with External ADC



- Once the process is complete the **ASIC can be switched readout phase**. The first set of amplitude and time voltages is made available at the **analog outputs**. The **address of the channel is serialised** and made available at the digital output using **six data clocks**.

VMM3A FEB designed

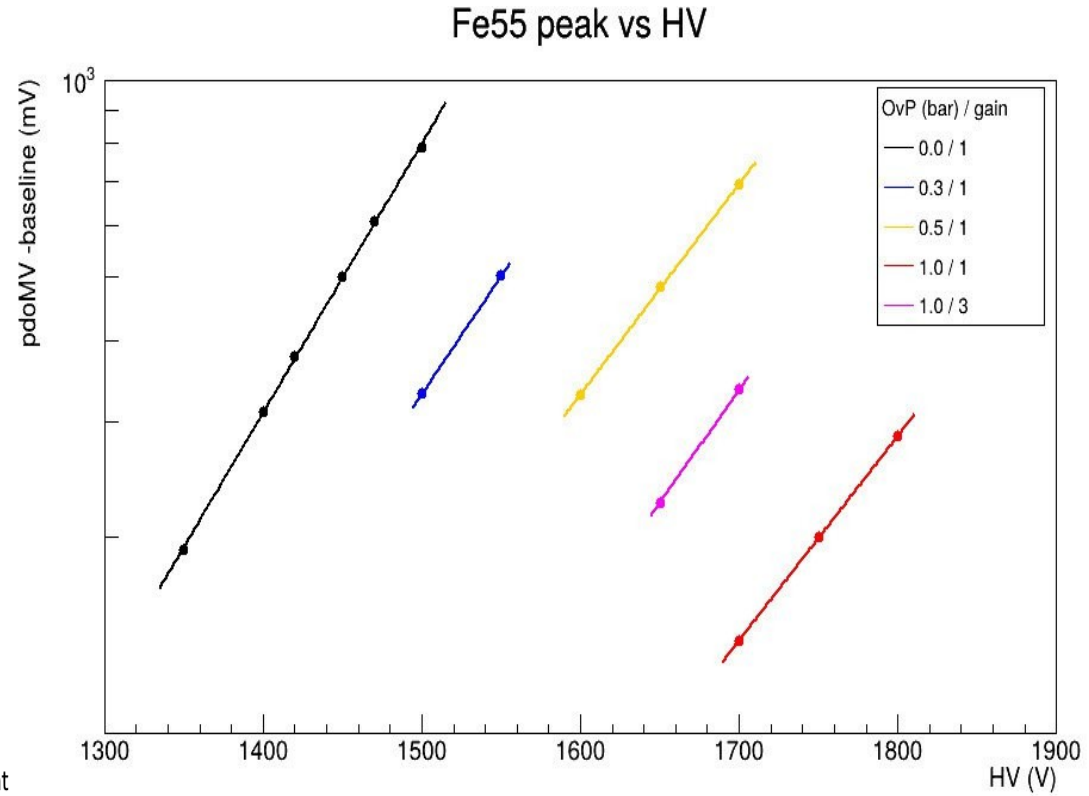
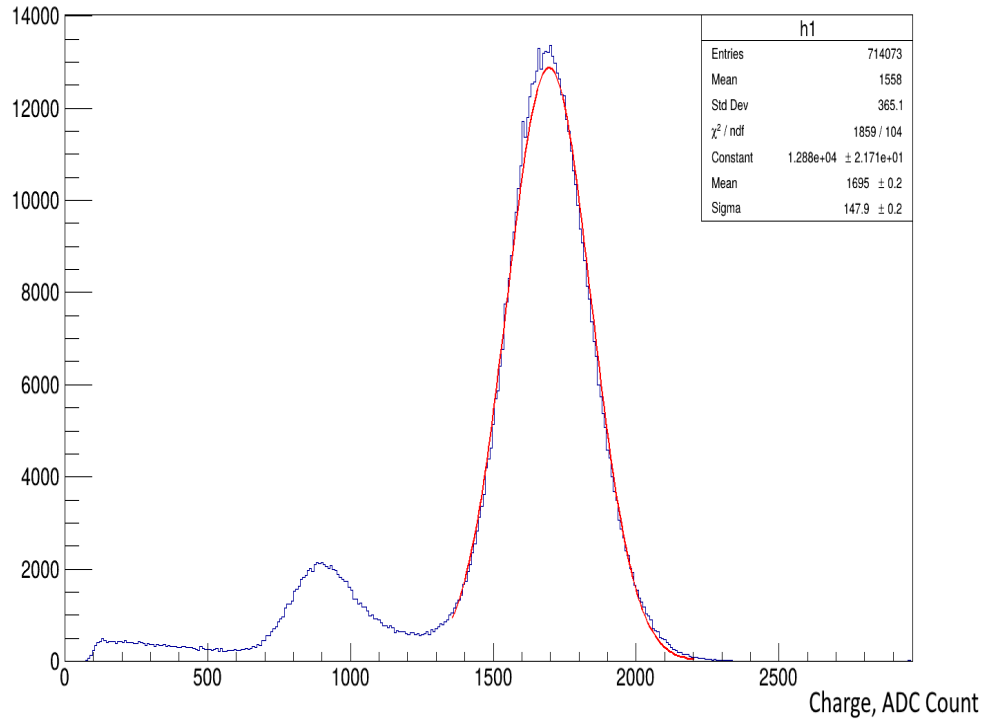




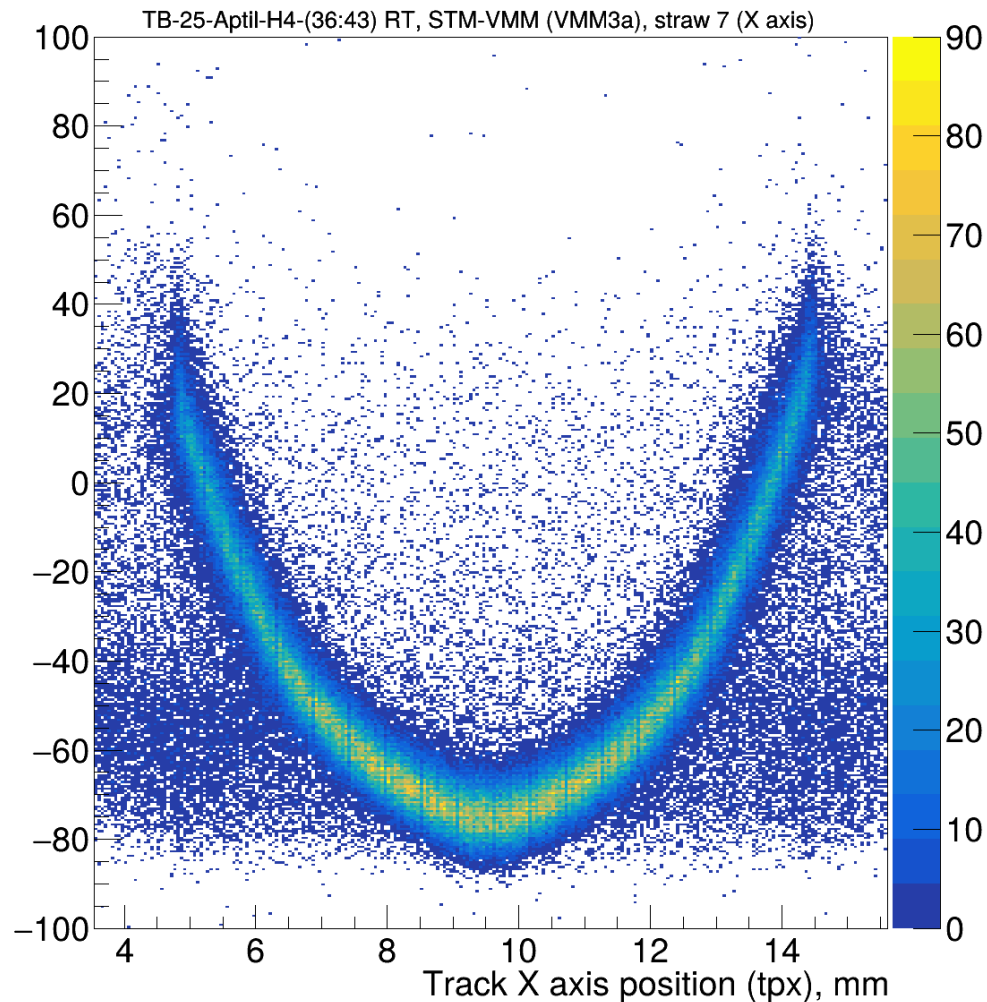
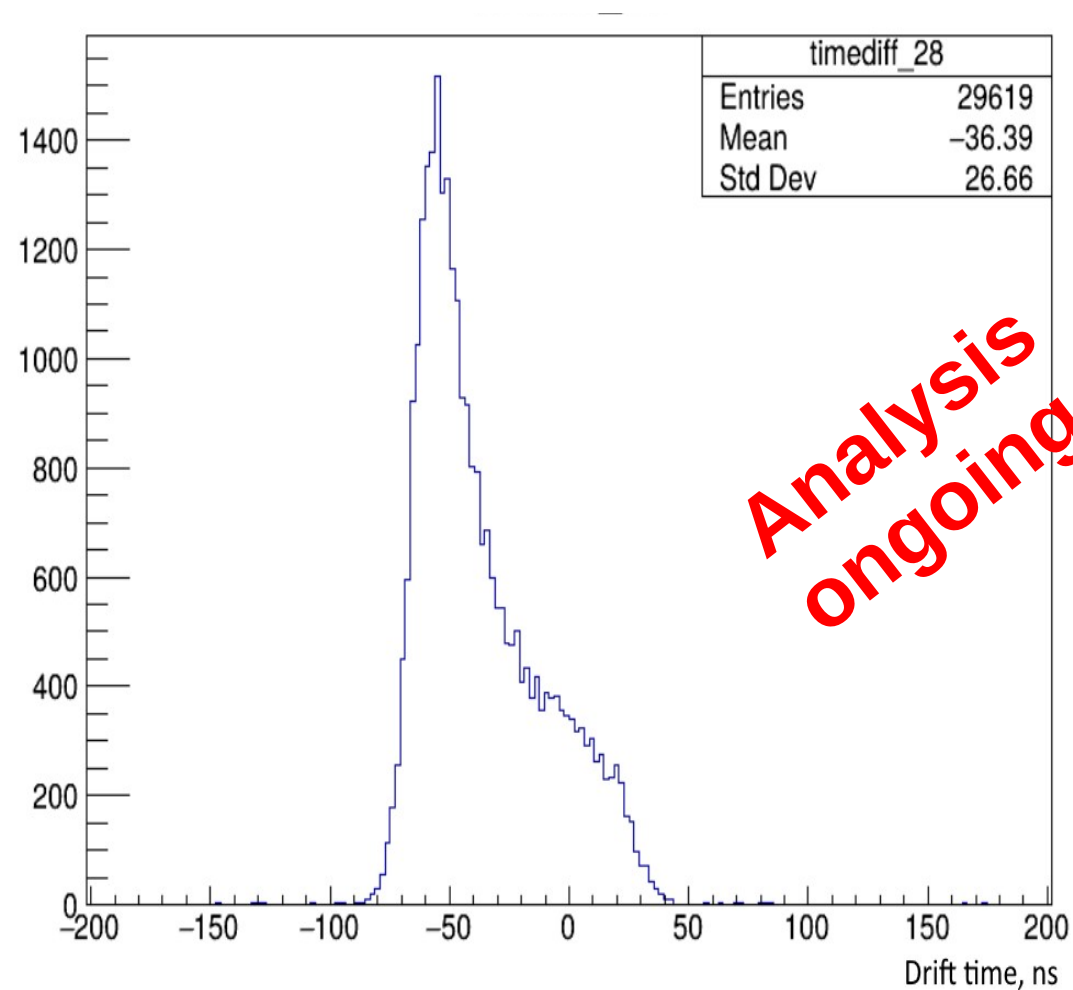
C1	DC1M	C2	DC1M	F1	C1-C2
10X	500mV/	10X	500mV/		1.00V/
FULL	-555mV	FULL	-640mV		-3.87V

Развертка	Синхр	C1 DC	Time
34.1us	Ждущий	1.74V	16:00:23
20.0us/div	Фронт	Нараст	2025/2/17
1.00Mpts			
5.00GSa/s			

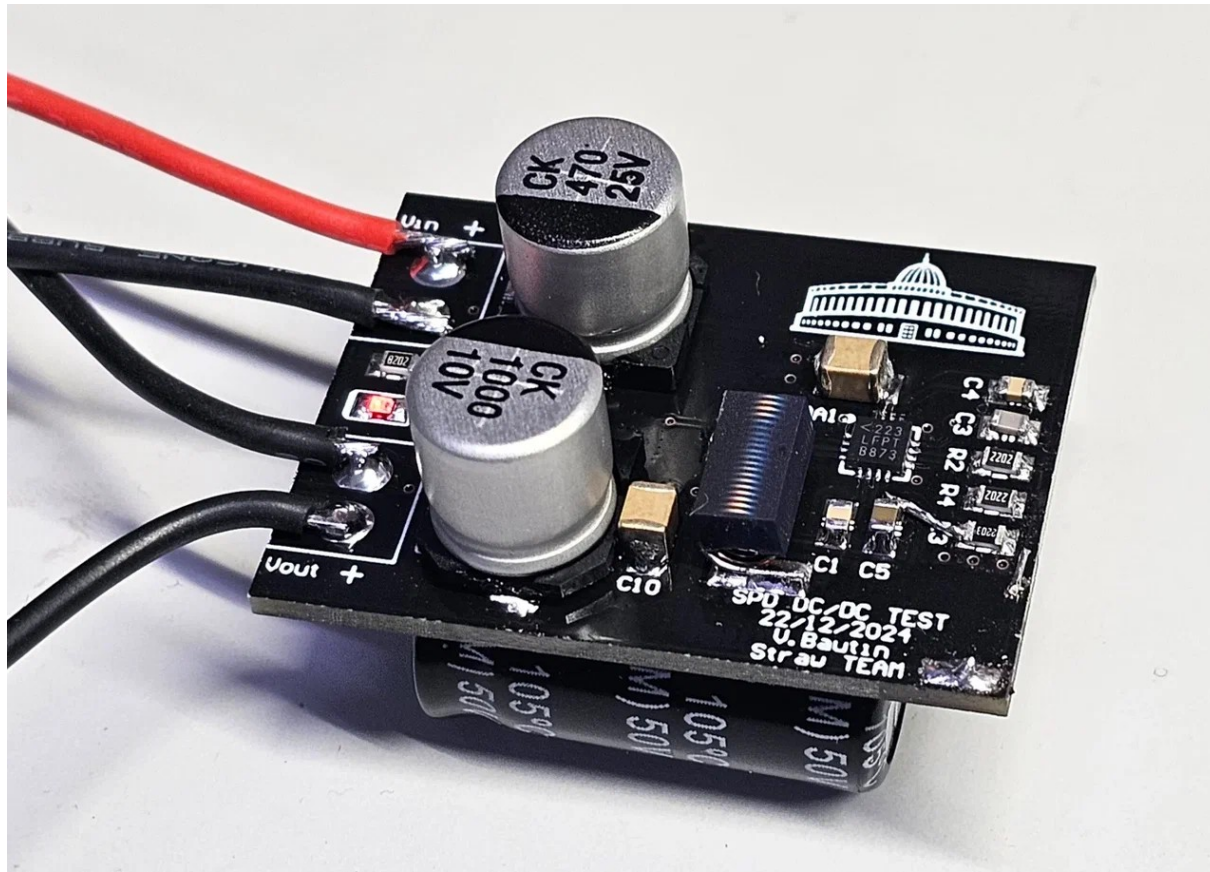
Fe55 Source, Ar/CO2 70:30 Mixture



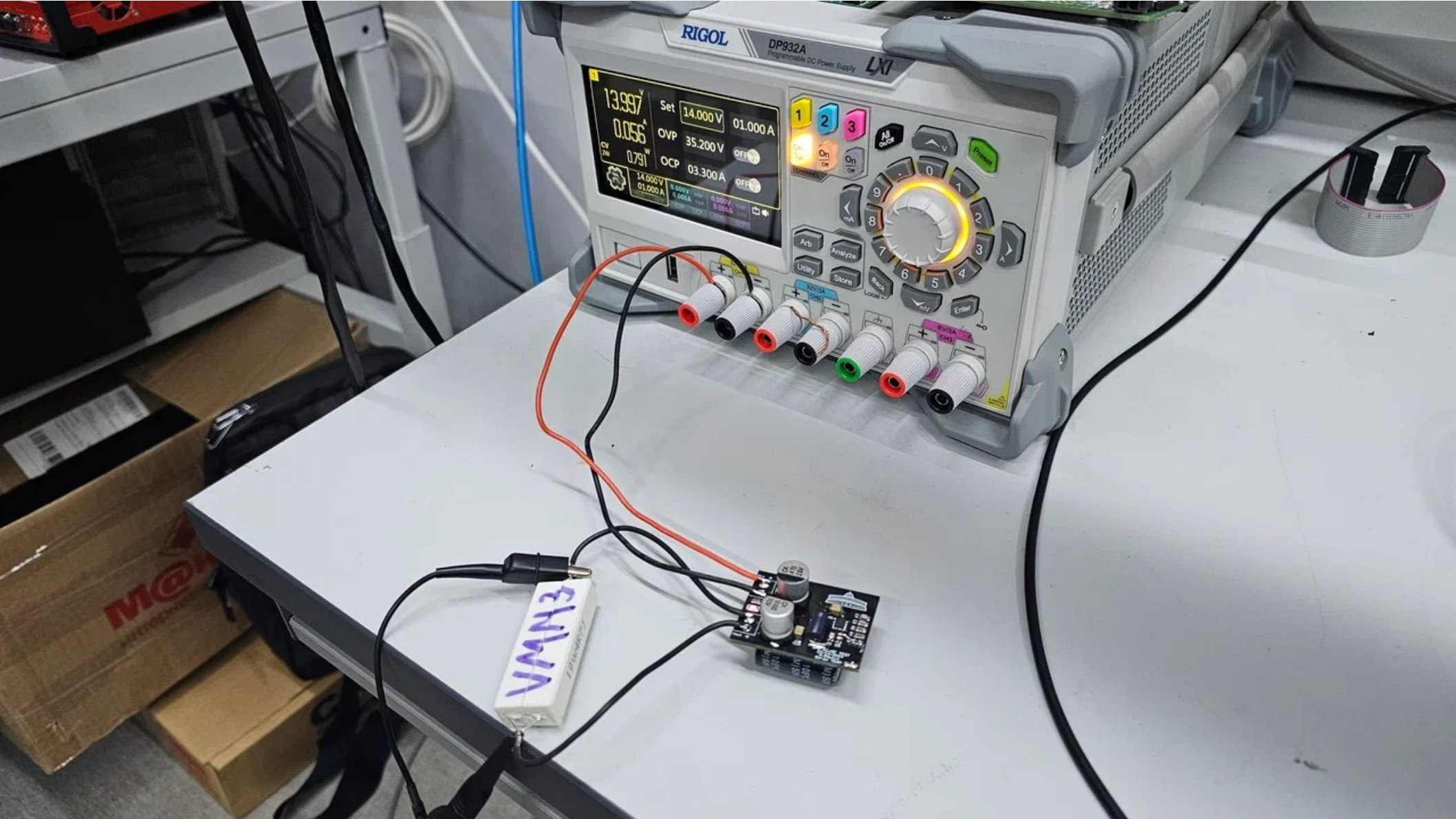
Time Measurements (Muon Testbeam April 2025)



DC/DC with Magnetic Field



In our recent design we have implemented several solutions prior to the **SPD-NICA** specifics. We have tested special DC/DC circuitry. By using the core-less coils new schematic is capable of operating in the magnetic fields of 1.5T. We have set up the tests with the load mockup, checking the efficiency, testing cooling options and the noise level.



RIGOL

DP932A

Programmable DC Power Supply

LXI

13.997V
0.056A
CV 0.791
14.000V 01.000A
Set 14.000V 01.000A
OVP 35.200V OFF
OCP 03.300A OFF
9.900V 0.900A
4.900V 0.400A
0.900V 0.090A

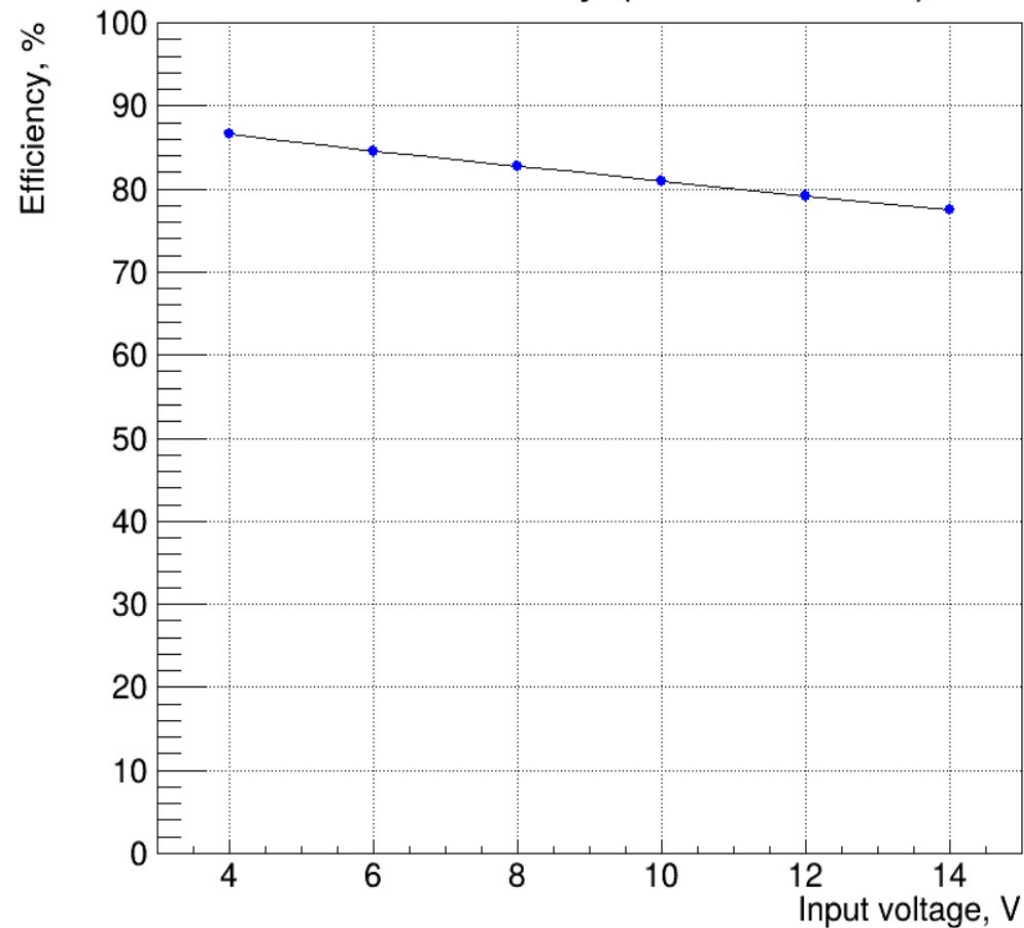
1 2 3
On On On
mA
0 1 2 3 4 5 6 7 8 9
Arb Analyze Utility Store Back Load Enter
+ -
+ -
+ -

VM2N3
E-TECHNOLOGY

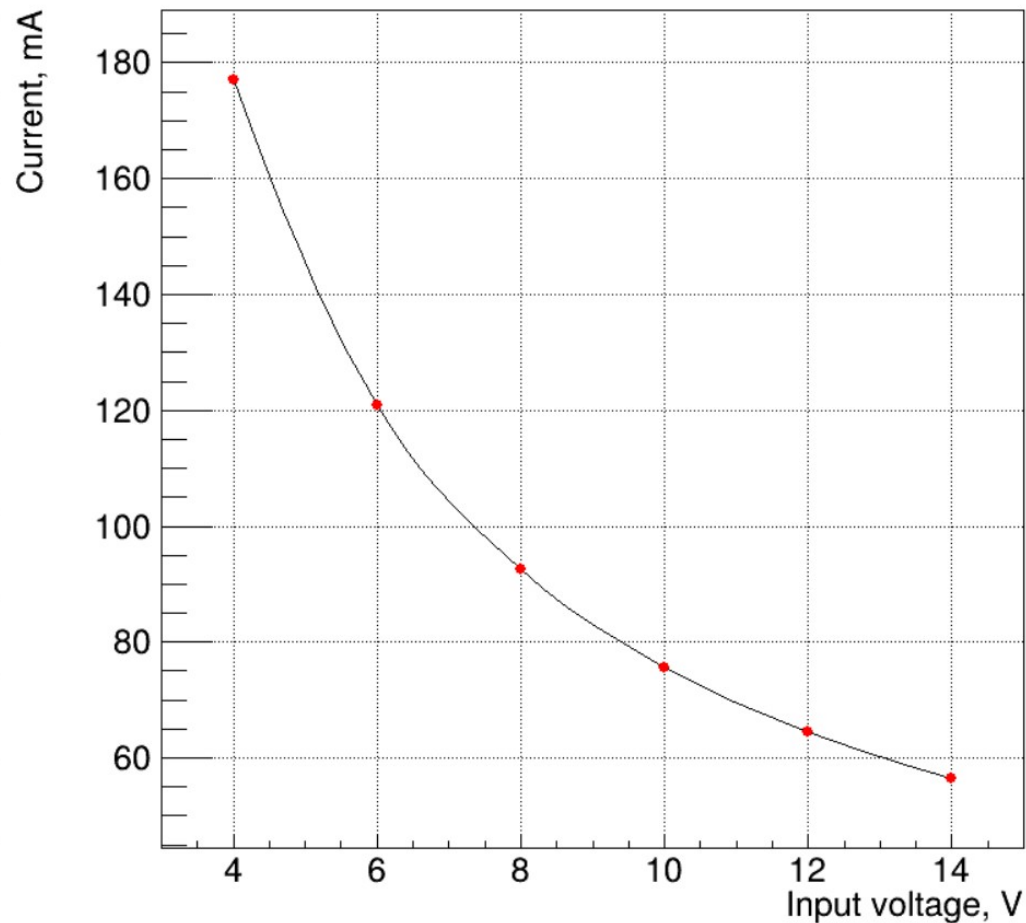
1000µF 16V
1000µF 16V

1-48712531

Power Efficiency (600mW Load)

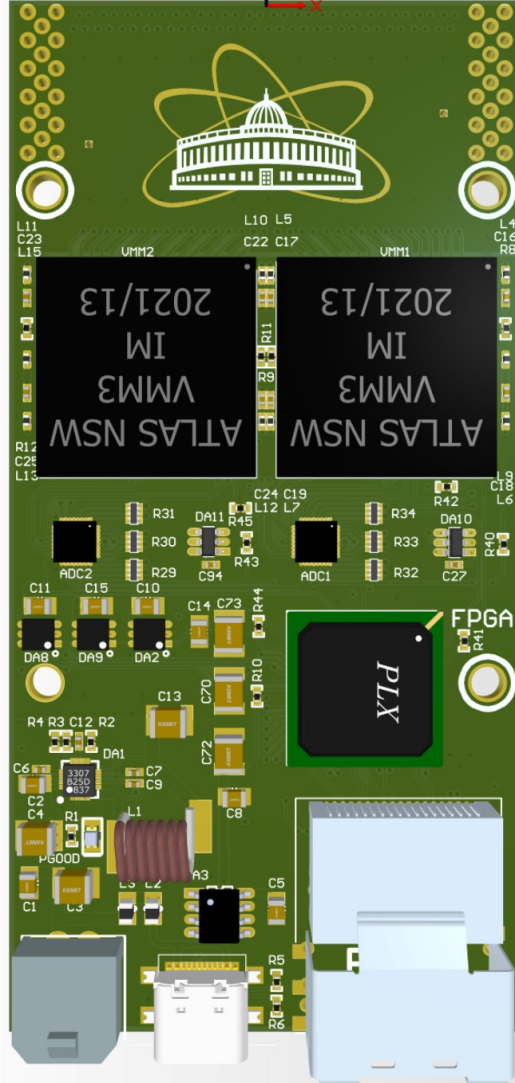
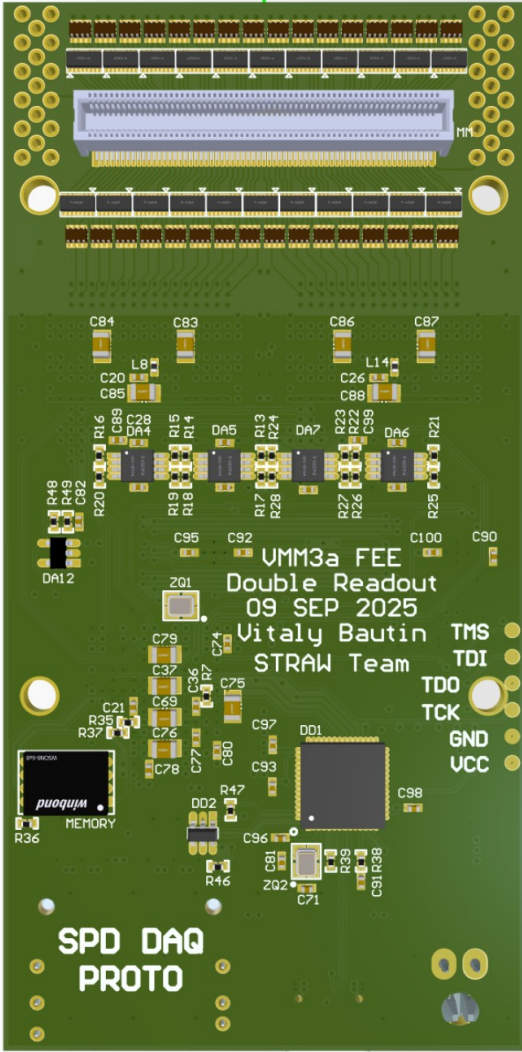


DC/DC Input Current (600mW Load)



Without DC/DC VMM3a consumption is 600mW @ 1.2V (500mA)

A new high-rate FPGA-based design



A new high-rate FPGA-based design

Compact 128-channel Panasonic connector and protection circuitry

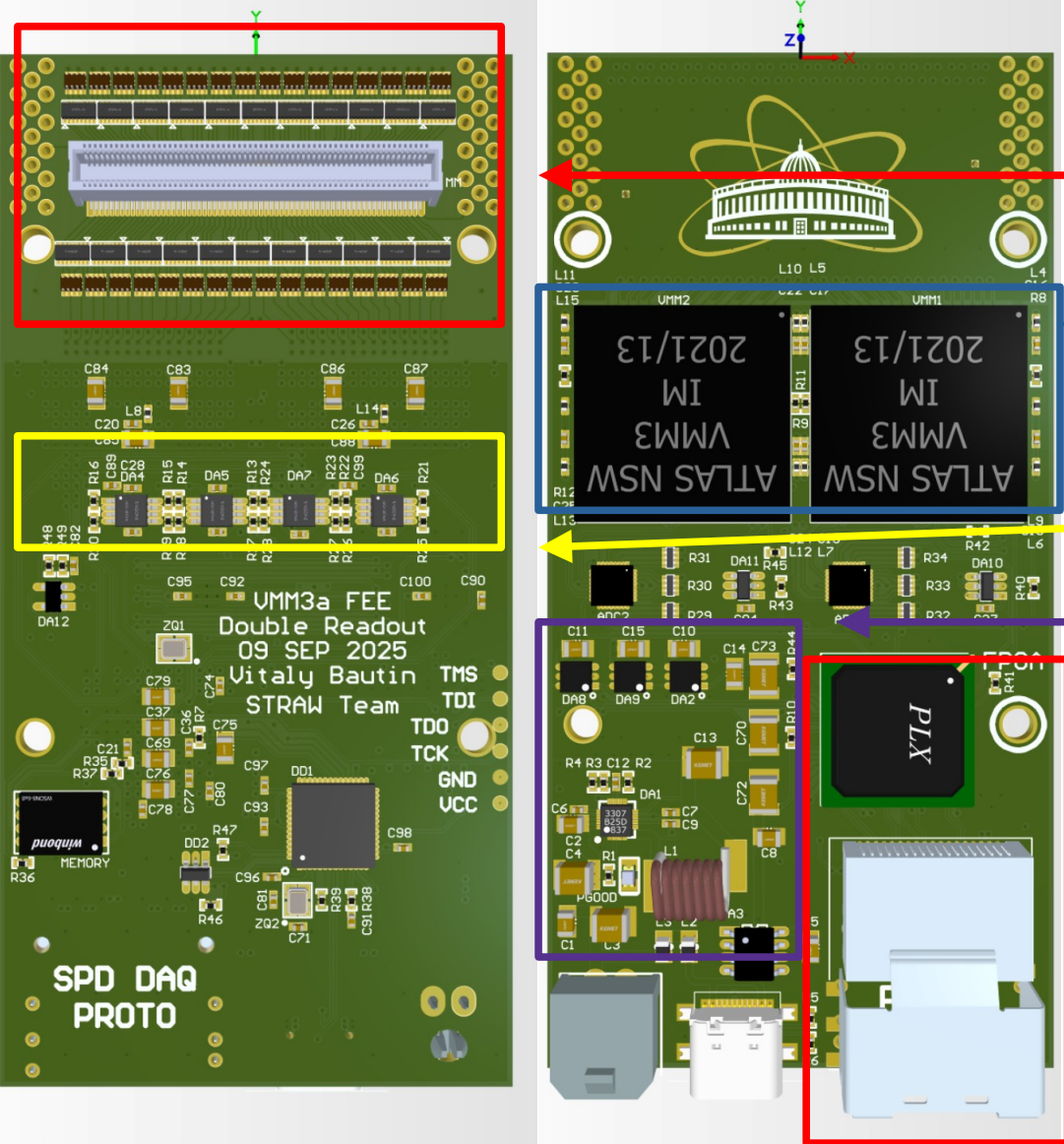
Double VMM3a readout

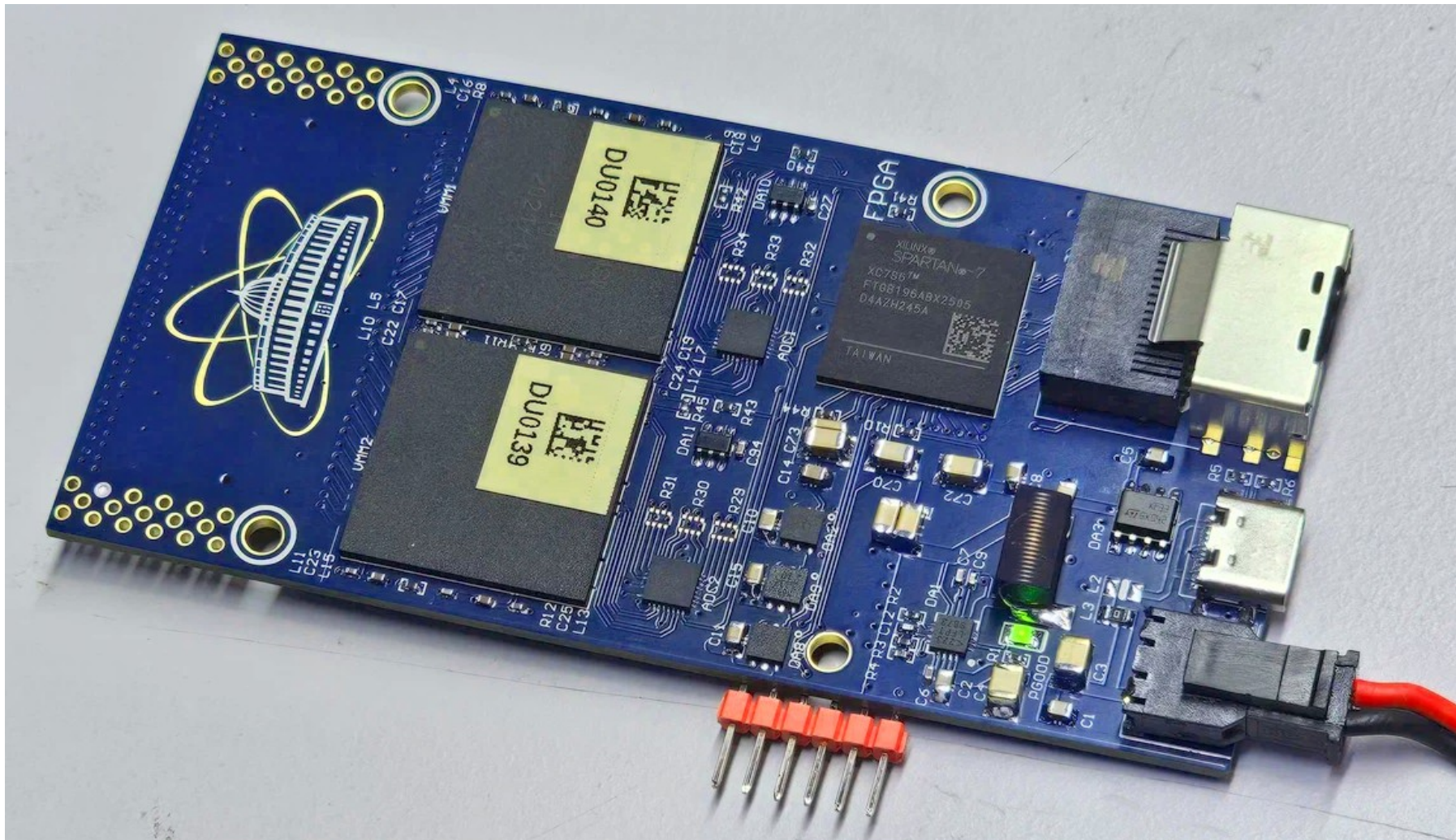
Bufferized differential external ADC circuitry for Time and Charge

High efficiency DC/DC working in magnetic field with separate LDOs for each VMM3a and FPGA, and separate shut-down options

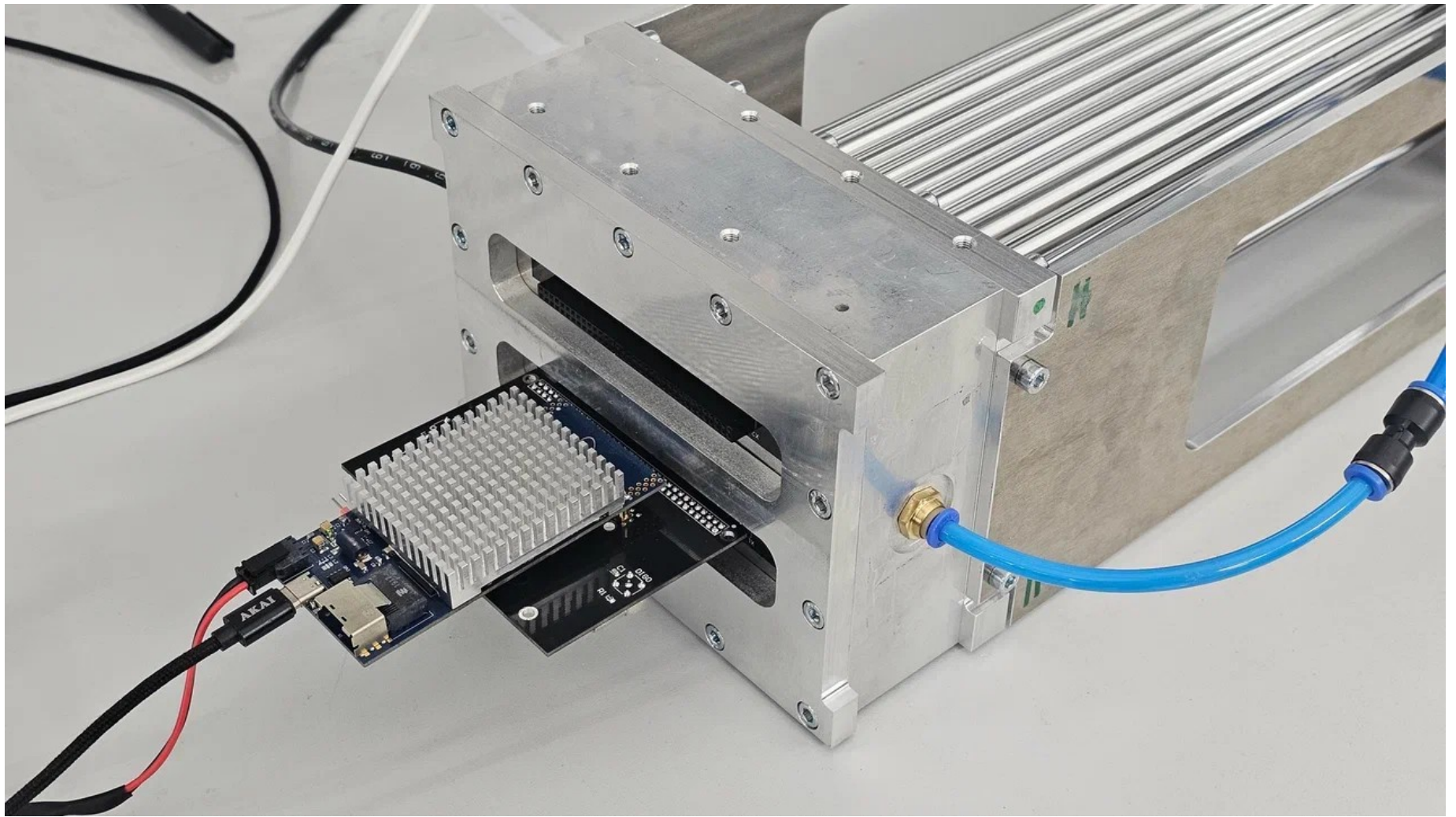
Standard SPD DAQ 1.25Gbps link for slow-control, configuration and data taking

Type-C for calibrations, tests and stand-alone operation

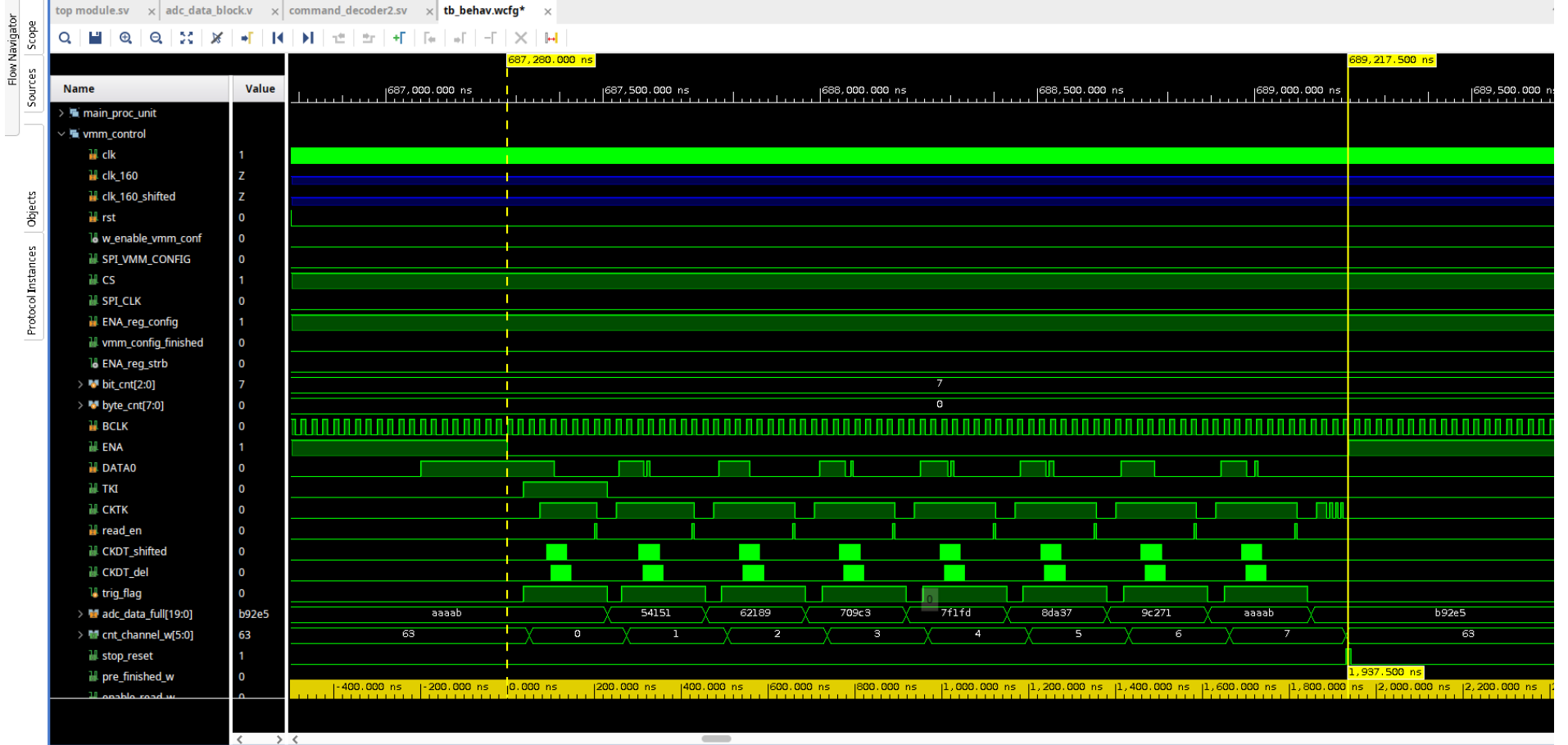




The first prototype has been produced during this autumn. Tests ongoing



The first prototype has been produced during this autumn. Tests ongoing

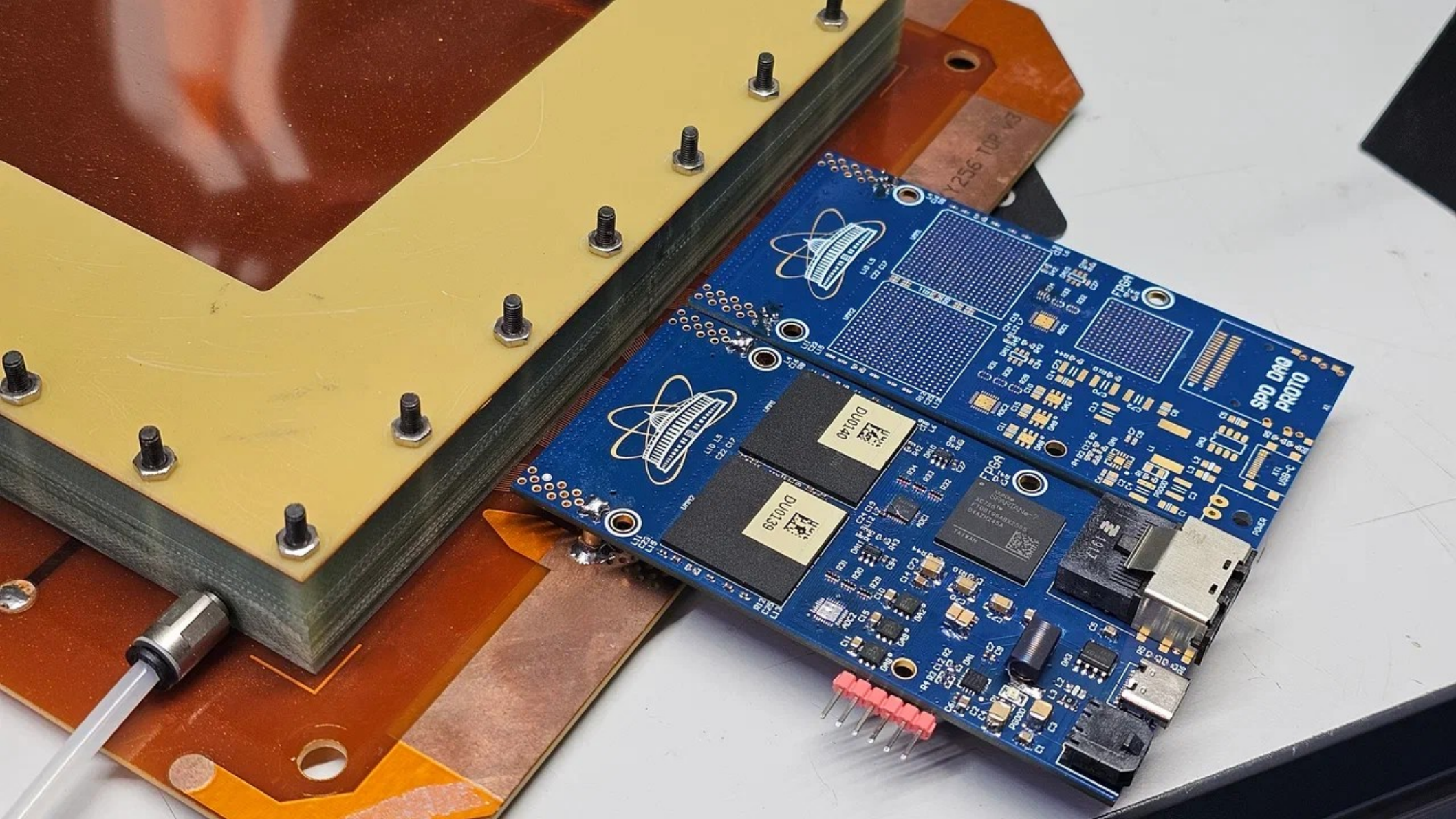


The main challenge was to achieve reasonable dead time. Typical event size in the straw tracker cell will be 8 channels. As shown on the plot above, in our new design with Spartan-7 FPGA we managed to reduce the dead time to less than 2 μ s. While this time is still worse than the one in normal Continuous readout mode of the VMM3a ASIC, it is more than enough to operate with the hitrate of 10-20 kHz per channel which is reasonable for the **SPD Stage-I**.

Conclusions

- A new front-end electronics solution has been designed for the first stage of **SPD-NICA** Straw Tracker
- In order to achieve the best performance for the straw tubes, we have developed completely new schematic including differential buffering and external ADCs
- We managed to utilize the existing VMM3A ASIC originally designed for ATLAS Micromegas detector
- That helped us to achieve a low-cost design with a price of ~3-5\$ per channel and a power consumption of about 20-30mW per channel
- The device is a complete multichannel solution for collection, amplification and digitization of incoming signals

Backup

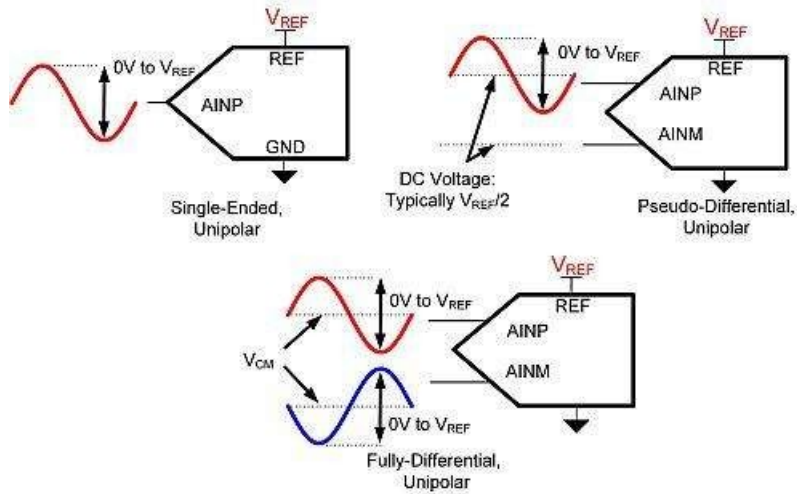


Summary table of SPD Straw Tracker parameters

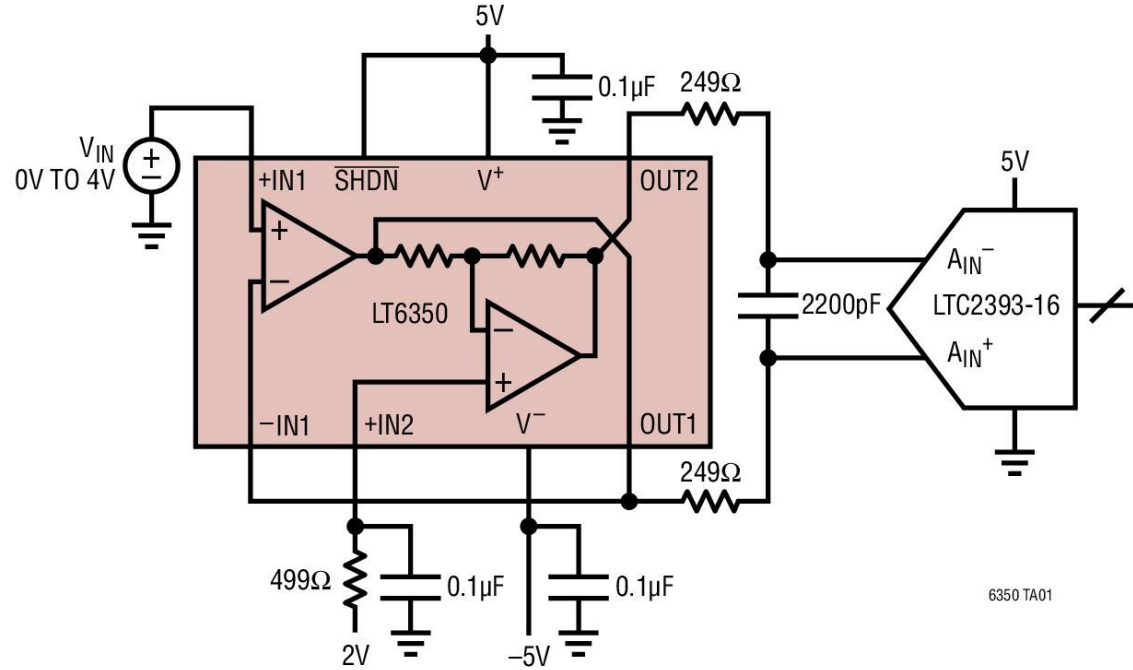
Detector type	barrel	end-cap
Detector tasks	dE/dx	xy coordinates, dE/dx
Working mode	triggerless	triggerless
Detector inner diameter, mm	540	
Detector outer diameter, mm	1700	
Number of layers	30 (double layer)	2x, 2y, 2u, 2v
Number of stations, sections	8 sections	12 stations
Number of channels	32288	8192
Tube diameter, mm	10	10
Maximum tube length, mm	2400	1700
Central core diameter, mm	0.03	0.03
Maximum detector capacitance, pF	26	18,5
Gas detector	70 Argon, 30 CO ₂	70 Argon, 30 CO ₂
Operating voltage, V	+1650	+1650
Multiplication factor, HV=1750	4.5E4	4.5E4
Charge from the first electron, fC	7.7	7.7
Electron drift velocity, $\mu\text{m}/\text{ns}$	65	65
Electron drift time, ns	120	120
Ion drift time, μs	100	100
Spectral resolution, μm	150	150
Maximum load, kHz per tube	150	

See A. Solin report at SPD Coll. Meeting: https://indico.jinr.ru/event/3189/contributions/17520/attachments/13230/22121/14_Development%20of%20an%20ASIC%20for%20straw%20and%20micromegas%20detectors%20of%20the%20NICA-SPD.pdf

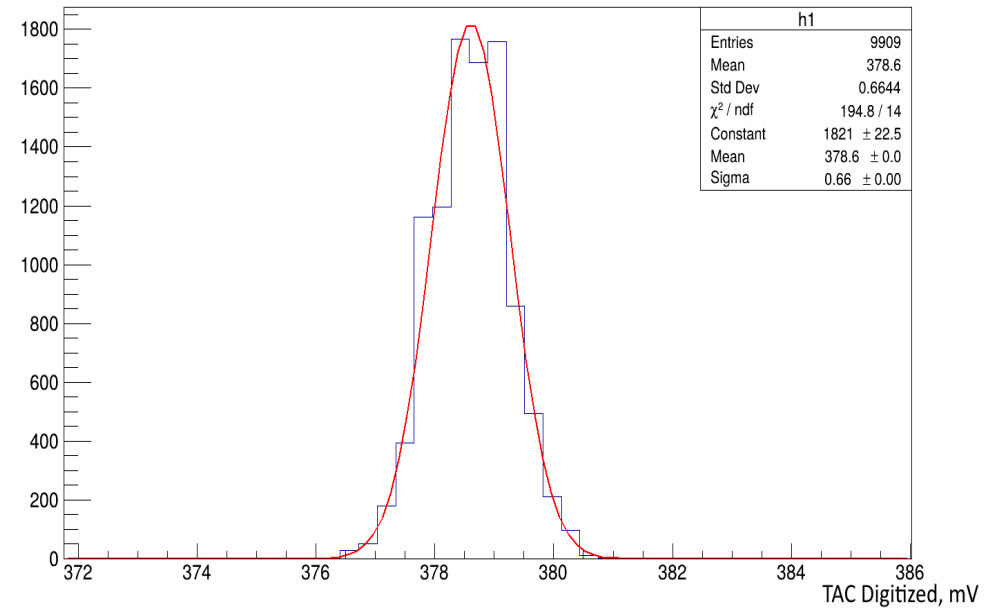
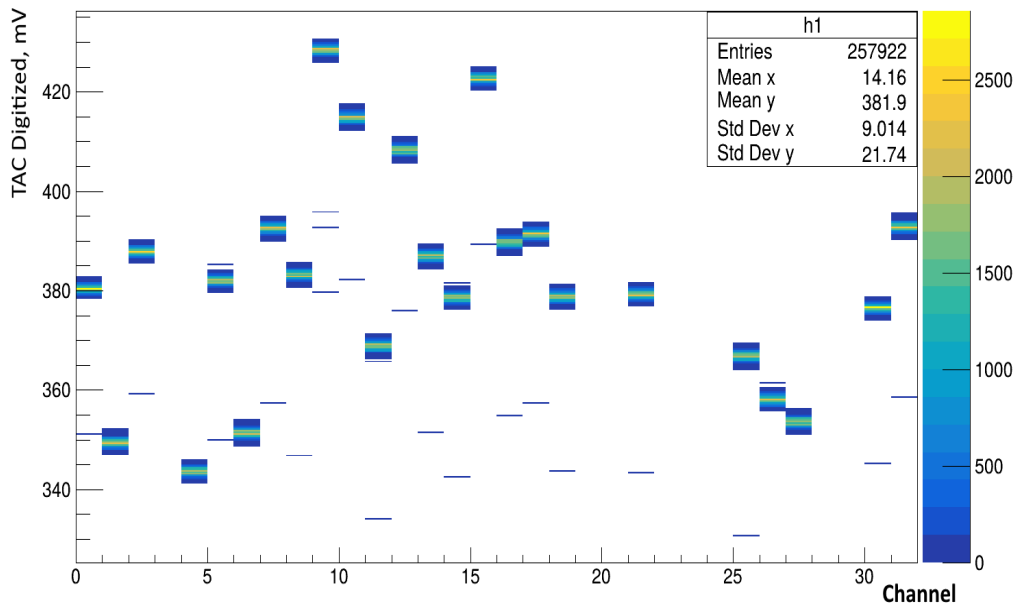
Single Ended vs Differential ADC



ADC Driver: Single-Ended Input to Differential Output



The real benefit of differential signals is in noisy environments, because of increased common mode rejection

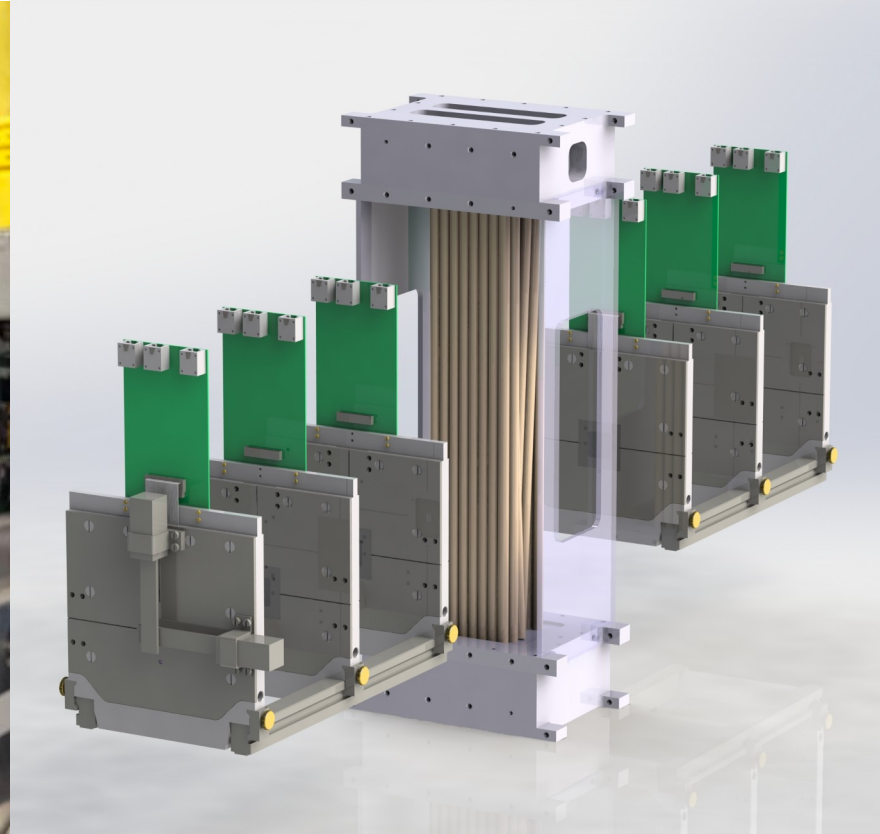
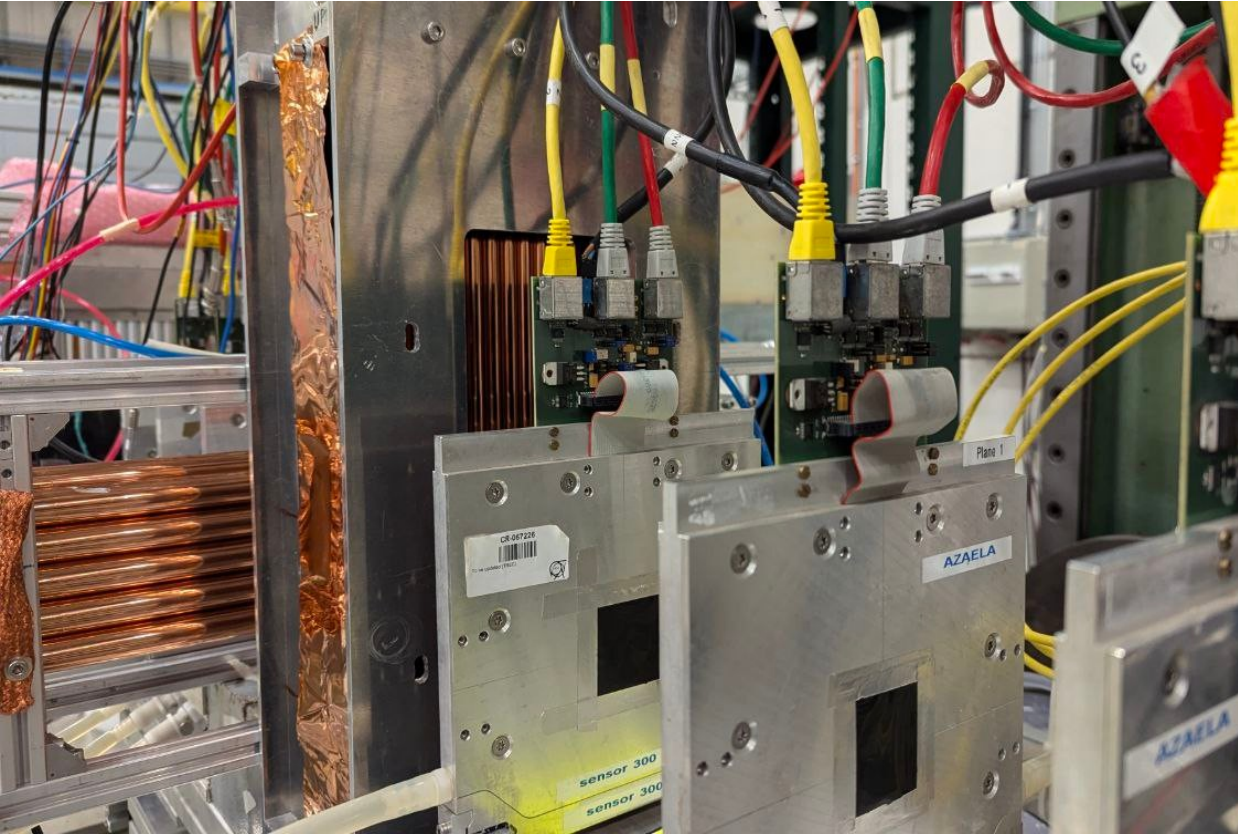


Timing resolutions obtained from a readout board equipped with VMM3a, MCU, and differential drivers for the internal ADC of the MCU with test pulses (300 fC) and different TAC slopes.

	TAC slope 100 ns	TAC slope 350 ns	TAC slope 650 ns
Slew rate	10 V/ μ s	2.8 V/ μ s	1.5 V/ μ s
Bin size	30 ps	110 ps	200 ps
Timing resolution	70 ps	230 ps	440 ps

Extremely Preliminary

Test beam setup evolution



CERN, H8 + H4 (2024)
6x Si planes
VMM / TIGER/ ATLAS ASD readout

