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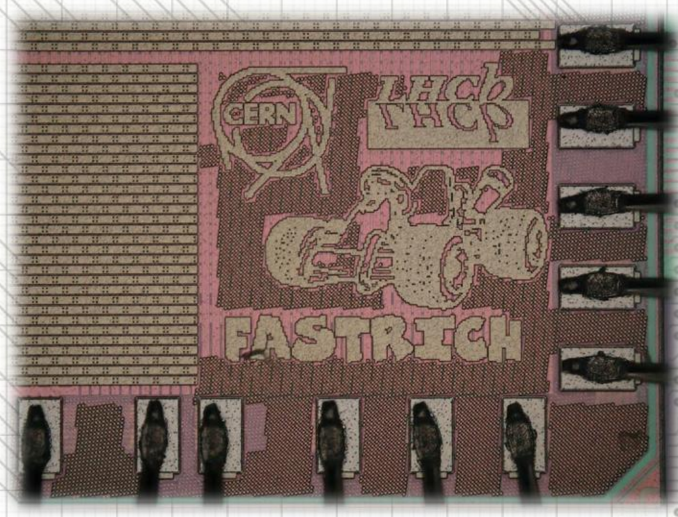
Novel Concepts for RICH Fast-Timing Electronics in View of the LHCb LS3 Enhancement Program



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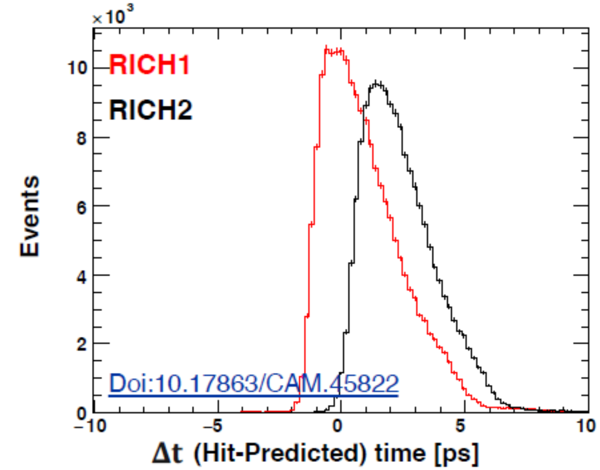
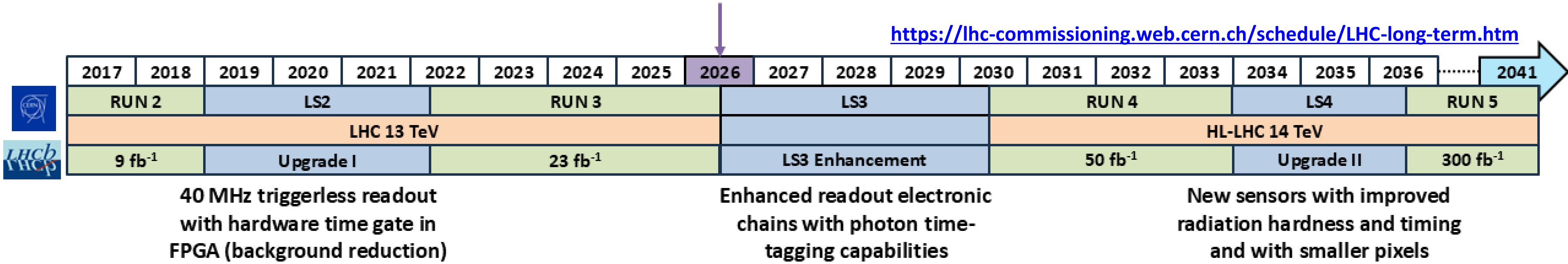
Introduction

- Cherenkov photons arriving on the RICH detector planes can be predicted with a time-of-arrival (TOA) better than 10 ps;

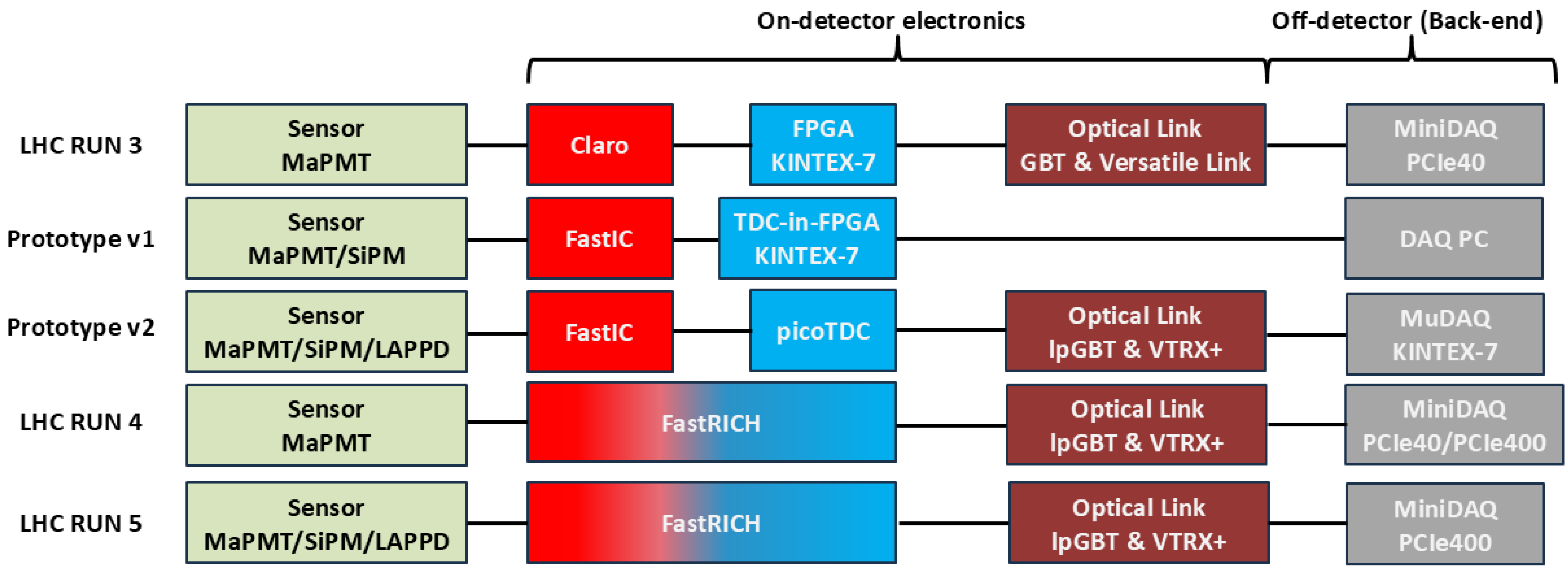
- In RICH reconstruction, the algorithm will compare the actual detector hit timestamp against its predicted TOA;

- The RICH detector performance will be enhanced by the addition of photon time-tagging capability;
  - improved background reduction;
  - better particle identification (PID) efficiency.





LHCb RICH electronics readout chains

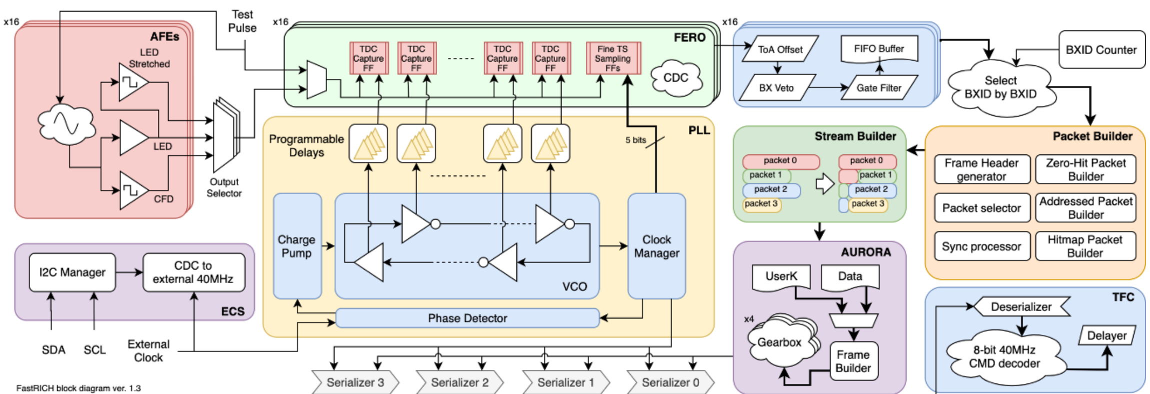


- **RICH opto-electronics chain will be improved in two phases:**
  1. **LS3 Enhancements => redesign of the readout electronics chain with fast timing capabilities (introduction of the FastRICH ASIC);**
  2. **Upgrade II => replacement of sensor technology.**

https://fastrich.docs.cern.ch/

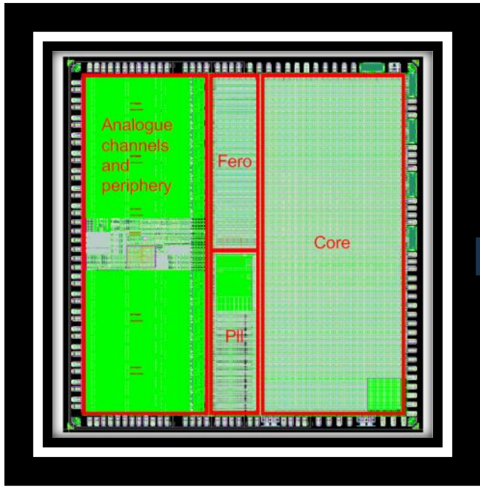
FastRICH

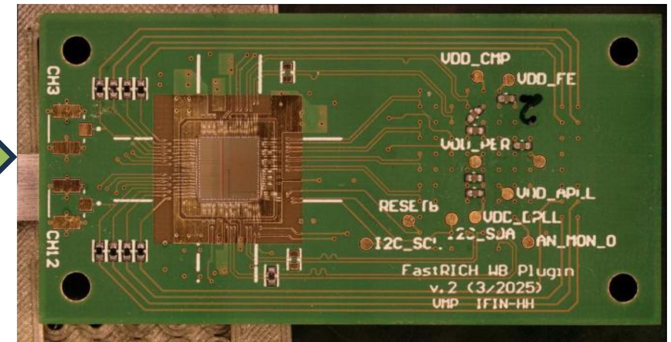
- ➢ Designed by CERN EP-ESE and in collaboration with University of Barcelona:
  - ❖ digital-on top design;
  - ❖ analogue recovery time better than 10 ns;
  - ❖ configurable hardware gate;
  - ❖ compatible with the LHCb Timing and Fast Control (TFC) and Experimental Control System (ECS) framework; (allows direct connection with lpGBT)
  - ❖ self-triggered 40 MHz readout rate.
- ➢ Radiation hard by design:
  - ❖ triple modular redundancy (TMR) for configuration;
  - ❖ enclosed layout transistors (ELT) for analogue blocks.

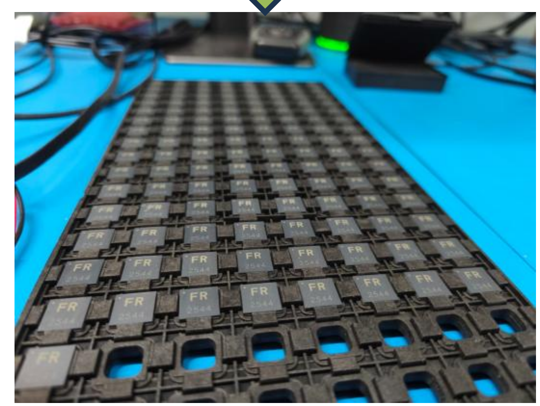


Specification	FastRICH ASIC
Target application	LHCb-RICH
Technology	CMOS 65 nm
Die	5 mm x 5.25 mm (146 pads)
Final package	QFN88 (10 mm x 10 mm)
Sensor coupling	MaPMT, SiPM, MCP
Channels	16 (single ended)
Input polarity	positive or negative
Input dynamic range	~ 30 µA – 2 mA
Discriminator	Leading edge discriminator (LED) and constant fraction discriminator (CFD)
TDC bin	TOA: 24.41 ps or 97.64 ps TOT : 390.625 ps
Bits per hit	~ 10 bits, dynamic length
Data encoding	Aurora 64b/66b
Data rate	0.32 Gbps – 5.12 Gbps
Power	~ 11 - 13 mW/ch
Target radiation environment	~2 Mrad; 7×10^{12} HEH/cm^2; 1 MeV n eq. 2×10^{13}/cm^2

FastRICH: Roadmap





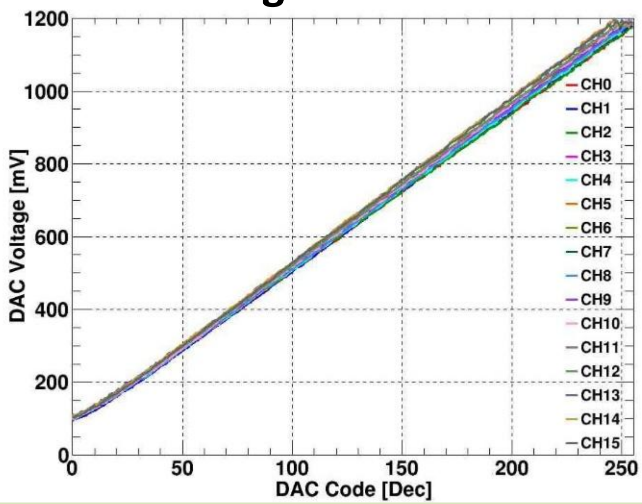


- FastRICH design was submitted in February 2025;
- Naked-dies received on 15th of May 2025;
  - wire-bonded dies to test PCBs available by the end of May 2025;
  - QFN88 “open-lid” package available in July 2025;
  - QFN88 ceramic package available in January 2026;
- Single-ASIC and multi-ASIC functionality tests have been performed since then;
  - a first FastRICH-based photon detector module prototype has been studied during the October 2025 SPS beam tests.

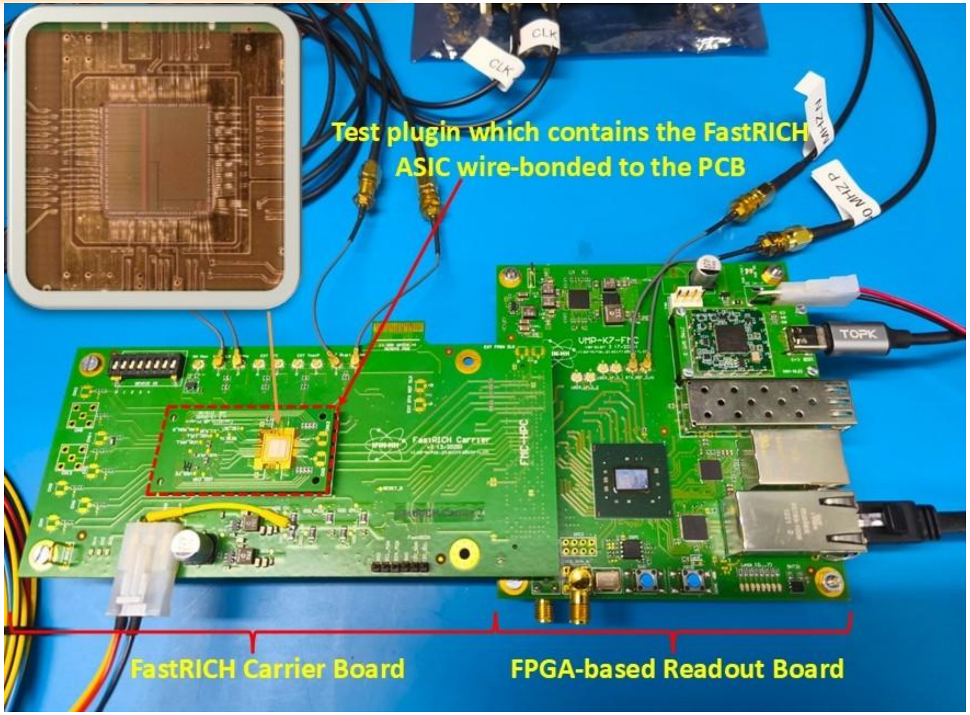
FastRICH: Single-ASIC tests

- In-house FPGA-based test system:
  - allow to enable full functionality of the ASIC;
  - acts as a small-scale readout system.

- The system is multi-purpose:
  - lab testing;
  - irradiation testing;
  - mass testing.

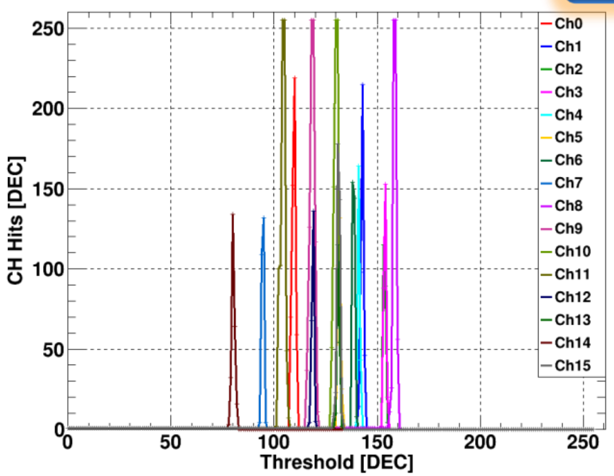


Linearity measurements of an internal rail-to-rail DAC (16 channels)



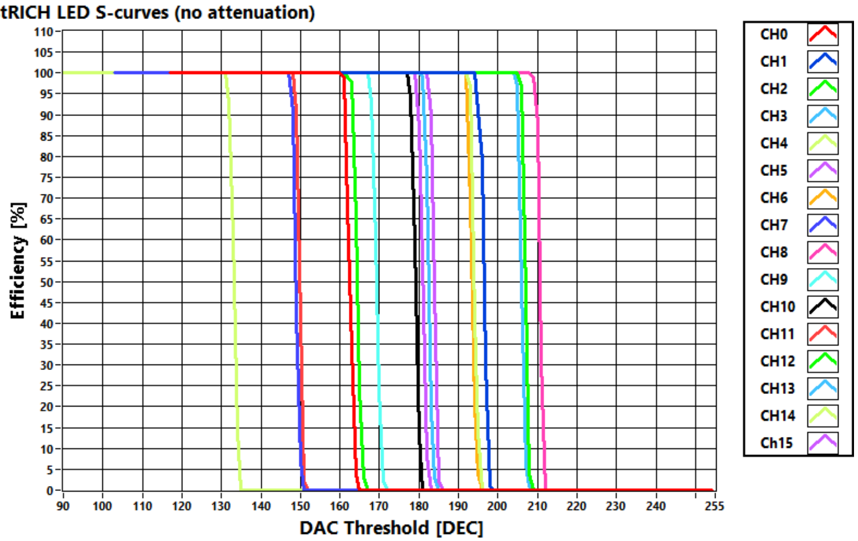
- More than 20 samples have been tested:
  - all have passed the power-up and basic testing;
  - all the interfaces (ECS, TFC, aurora lanes) are working ok and responding accordingly to the user inputs.

FastRICH: Single-ASIC tests



Threshold scans measurements (internal AFE feature)

- Build-in threshold scan function inside the ASIC:
  - measurements to establish the electronic noise levels in the analog processing paths;
  - counts the number of discriminator rising edges triggered by the electronic noise;
  - this can be done only via ECS, thus not relying on the entire readout chain.

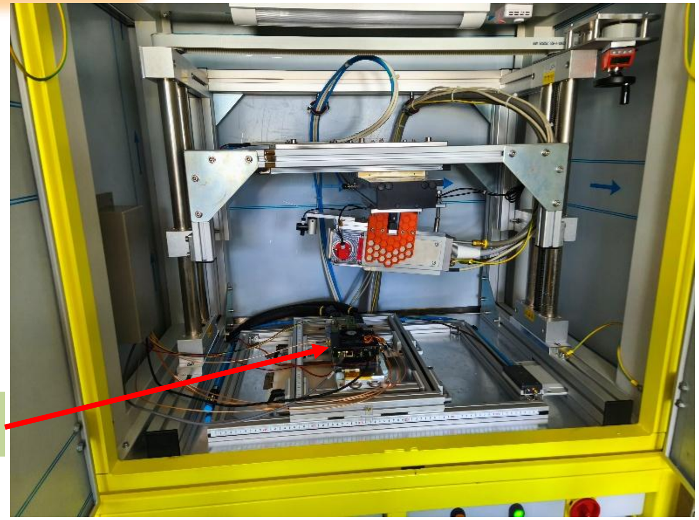


- TDC testing results:
  - DNL std deviation: < 6 ps (on average across all the channels);
  - INL value range: ~+/- 24 ps (on average across all the channels);
  - for LS3E the MaPMT σ is ~ 180 ps.

- Measurements with the entire readout chain and with internal test pulse injection have been performed successfully;

FastRICH Radiation Testing: TID

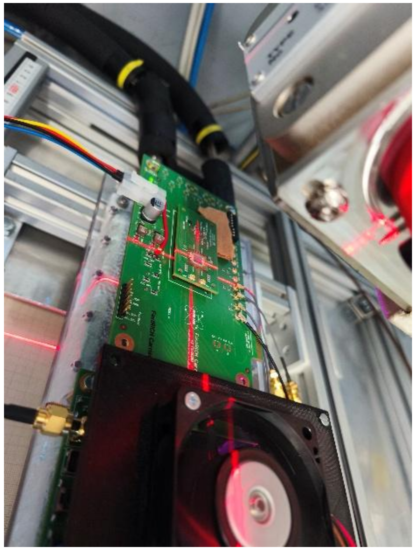
- **2 FastRICH samples were tested for TID with X-rays:**
  - **“Obelix” X-ray facility of CERN EP-ESE (July 2025);**
  - **room-temperature irradiation;**
  - **test was more focused on the analogue side.**



FastRICH setup installed

- **Sample 1: <u>total dose of 2 Mrad</u> delivered in 2 steps:**
  - **200 krad + 1.8 Mrad; (dose rate of 0.53 Mrad/h)**

- **Sample 2: <u>total dose delivered of 12 Mrad</u> in 3 steps of 4 Mrad each (dose rate 2.04 Mrad/h);**

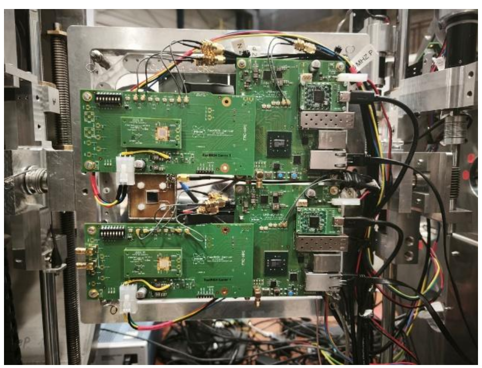


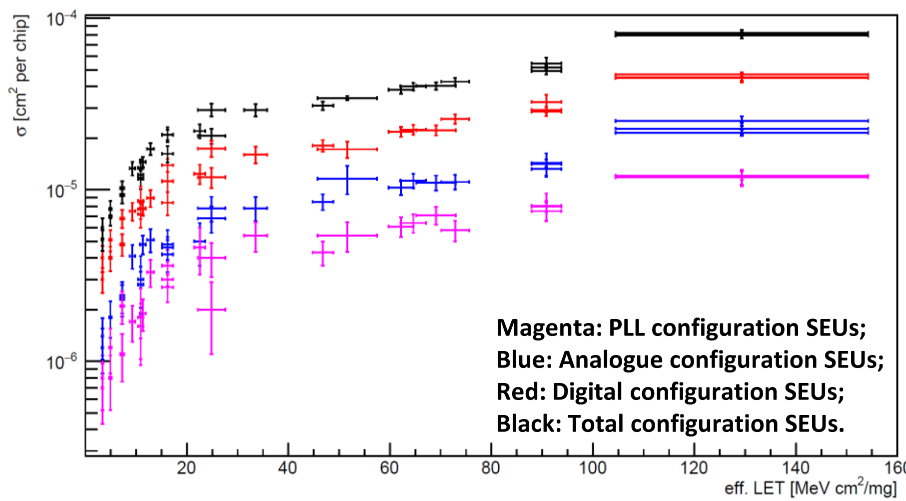
- **The ASIC seem to tolerate very good the TID, even at high and unrealistic dose rates;**
  - **no failures were observed and no visible effects were recorded in the power consumption after 12 Mrad;**
  - **all 67 DACs have kept their transfer curves with no visible effects after 12 Mrad of TID.**

Expected TID in RICH during RUN 4 is 200 krad and 2 Mrad during RUN 5.

FastRICH Radiation Testing: SEE

- **Single Event Effects (SEE) testing with heavy ions beam (October 2025):**
  - 4 samples tested at UCL-HIF in Louvain Belgium;
  - no SEL recorded up to 125 MeV cm^2/mg;
  - threshold SEU cross-section in configuration is lower than 3.2 MeV cm^2/mg;
  - configuration SEUs are mitigated by the TMR logic with no effect on the functionality;
  - no functional or global failures were observed;
  - signs of data corruption were observed in the output data, but most of them were self-mitigated (transient).

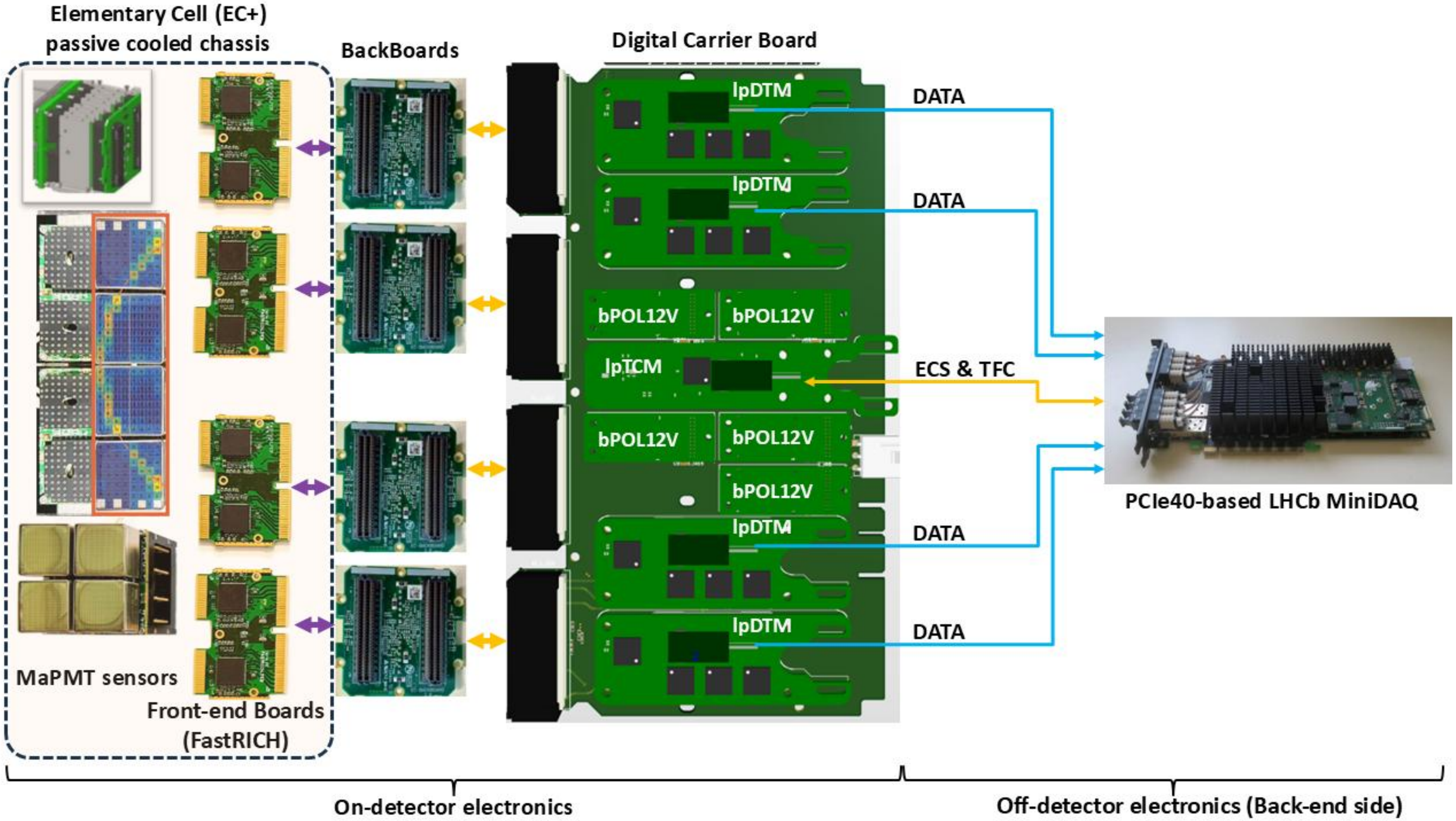




Configuration SEU cross-section at different LET values

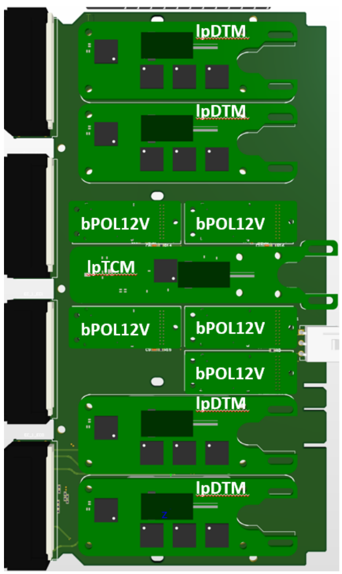
- **Beam settings:**
  - ion flux: 15000 particles/cm^2/s (maximum);
  - fluence per run: 0.8*10^7 – 3*10^7 particles/cm^2;
  - LET between 3.2 – 125 MeV cm^2/mg.

Towards a LHCb RICH Electronics Readout Chain

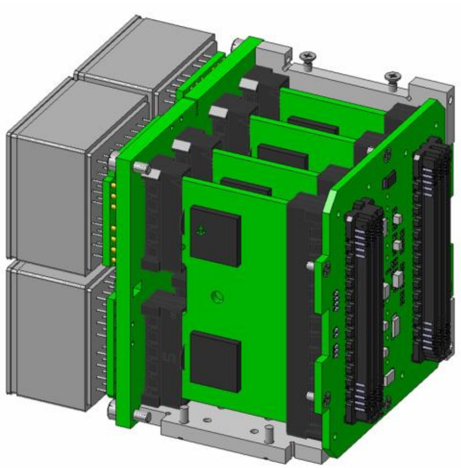


- **A proof-of-concept design was already tested with success during the October 2025 SPS test beam campaign;**
  - **now a first RICH LS3E electronics chain prototype is being designed.**

Towards a LHCb RICH Electronics Readout Chain

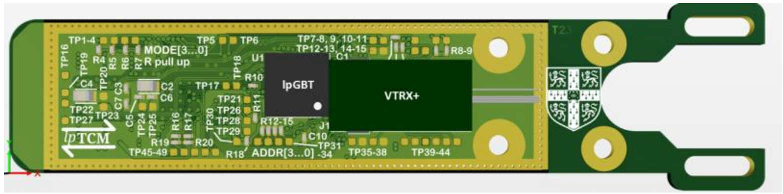


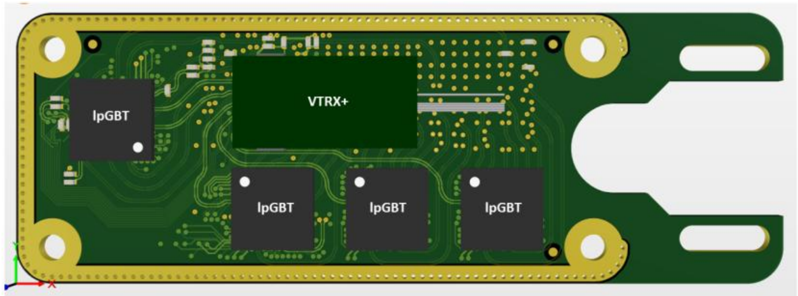
- **Digital carrier board is a largely passive integration board:**
  - **distributes the power across the chain;**
  - **it routes the signals (control, monitoring and high-speed) between the FastRICH ASICs and the lpDTM/lpTCM plugins (e.g., lpGBTs);**
  - **multiple variants will be designed to be used in high and low occupancy RICH regions;**
    - **to optimize component usage and bandwidth.**



- **The elementary cell (EC+) holds together multiple components:**
  - **MaPMTs mounted on the baseboards;**
  - **4x front-end boards (FEB) with 4x FastRICH ASICs on each;**
    - **2 variants of FEBs with be designed;**
  - **backboards used to connect to the digital carrier board;**
  - **everything is integrated in a passive cooled chassis.**

Towards a LHCb RICH Electronics Readout Chain



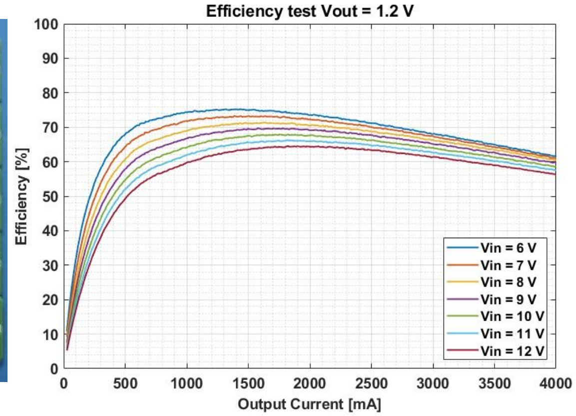


- **lpGBT Timing and Control Module (lpTCM):**
  - **acts as a master at carrier board level;**
  - **it controls the lpDTMs (EC links);**
  - **provides the TFC to the FEBs.**

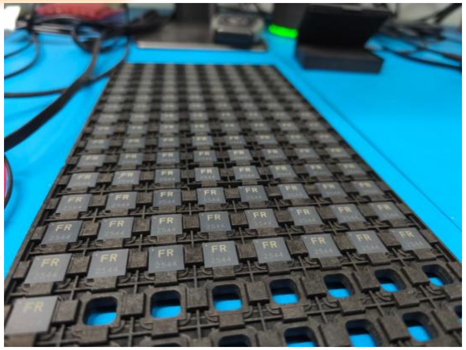
- **lpGBT Data Transmission Module (lpDTM):**
  - **reads the FastRICH output serializer lanes;**
  - **provides some control signals to the FEBs (reference clocks, ECS, resets, etc.).**

- **bPOL12V prototype modules have been build and intense studied in the lab;**
  - **1.2 V and 2.5 V power rails are needed.**

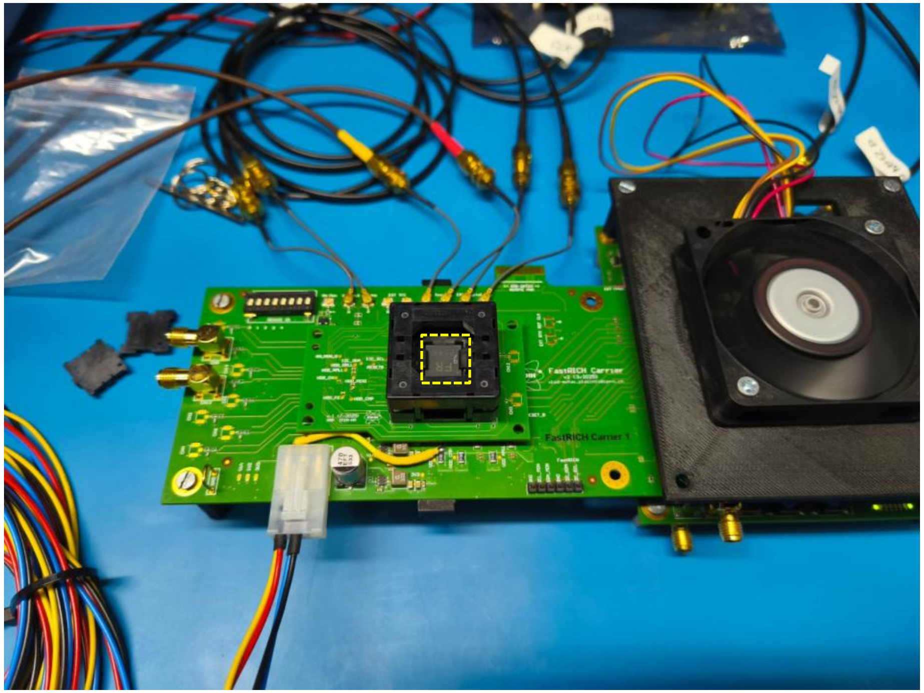
- **A working scenario suitable for RICH electronics has been identified:**
  - **input voltage 7 - 8 V, load 25-75%, cooling mandatory;**
  - **overall efficiency: 70-75%.**



FastRICH: Preparation for Socket Testing



- **Socket testing is mandatory:**
  - **to identify bad ASICs before assembly them on PCBs.**
- **Plans are in preparation to use the existing single-ASIC testing system:**
  - **a new plugin with QFN88 testing socket has been designed.**



- **The strategy foresees the connectivity testing of the package wire-bonds;**
  - **all the interfaces, control and monitoring pins are included;**
  - **input channel pads are also tested;**
  - **includes also measurements of power consumption, bandgap reference etc.**
- **First batch testing results (pre-production):**
  - **150 packaged ASICs received;**
  - **149 good ASICs and 1 bad ASIC;**
  - **tests take ~ 90 s per ASIC.**

Conclusions and Future Plans

- The FastRICH ASIC, one of the RICH major milestones, seem to behave as expected, with no design problems reported to this date;
  - so far, everything is working according simulations;
  - it has been successfully coupled to MaPMTs in test beam (October 2025 SPS tests);
  - there is still work to be done.

- Radiation testing of the ASIC reveals very robust design against TID and SEE:
  - no visible TID effects were seen so far (up to 12 Mrad);
  - configuration SEUs have been mitigated by the TMR logic with no impact on the operation;
  - more radiation tests in 2026: X-Rays (CERN), heavy ions (UCL-HIF), neutrons (JSI-Slovenia) and CHARM (CERN).

- Work in progress to design a first prototype of a RICH photodetection module:
  - this will demonstrate the concept of having multiple ASICs connected together;
    - FastRICH, lpGBT, bPOL12V and VTRX+.