Microchannel Cooling Substrates

Bart Verlaat, Oscar Augusto de Aguiar Francisco, Burkhard Schmidt and Paolo Petagna on behalf of the DRD8 Collaboration

TIPP2026 – Mumbai, India

Presented by Bart Verlaat on behalf of Oscar Augusto de Aguiar Francisco (Who could not make it to Mumbai)

Microchannels cooling

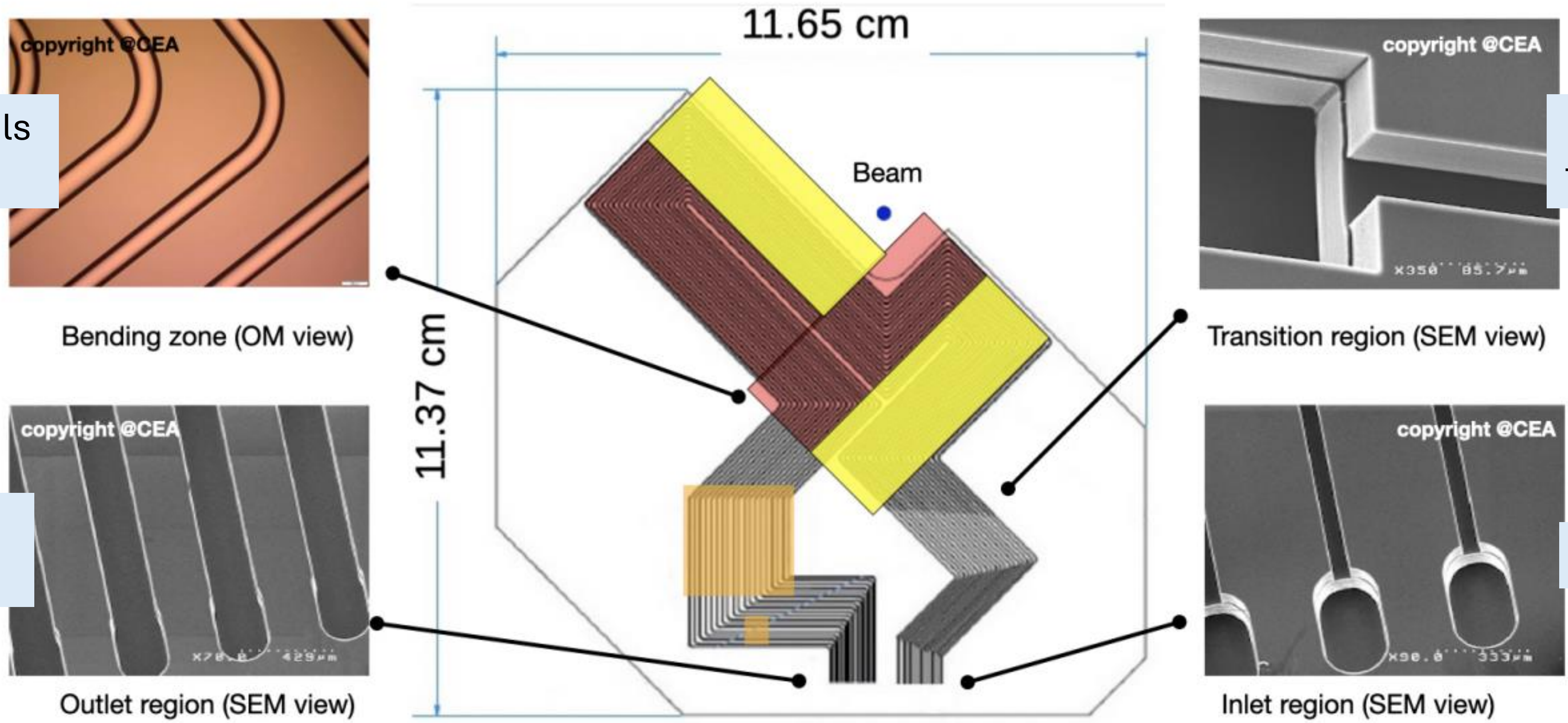
LHCb VELO Upgrade 1 (j.nima.2022.166874)

Boiling channels (400 micron)

Output and main channels

Restriction transition to boiling channel

Input and restrictions

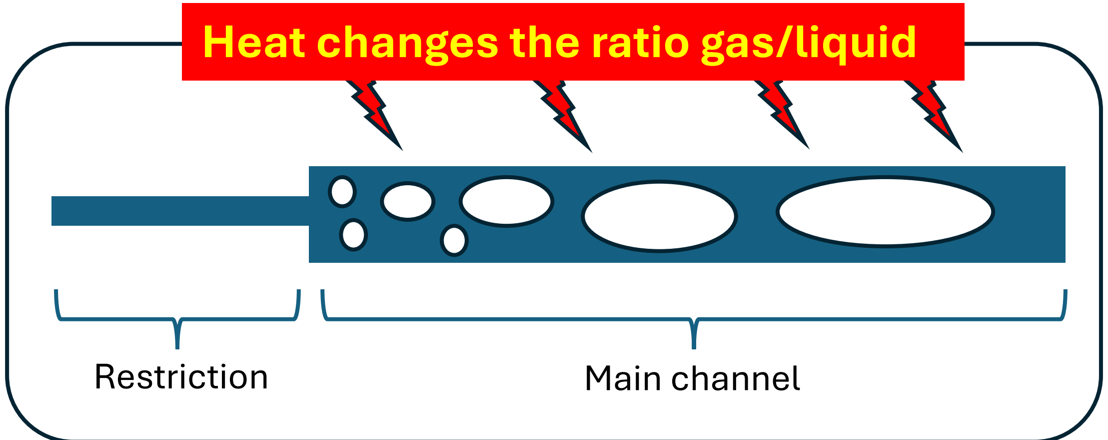


Bending zone (OM view)

Transition region (SEM view)

Outlet region (SEM view)

Inlet region (SEM view)



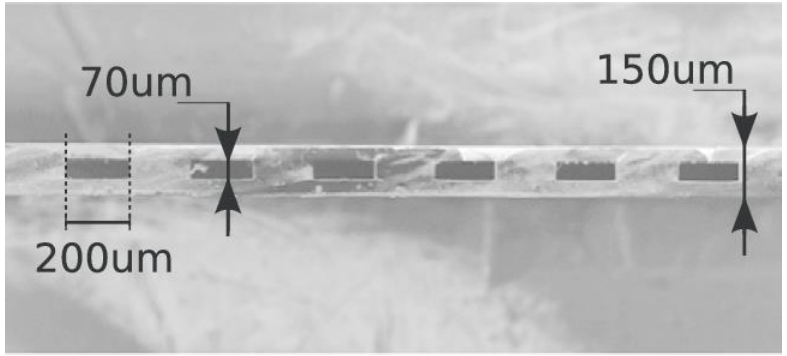
- Micro channels are small cooling channels embedded inside a detector support plate or the sensor it self
- Channels or more advanced structures can be made using different manufacturing technologies.
- Micro channels can be designed for single or 2-phase cooling

Why microchannels?

- Micro channel brings the cooling towards the heat source => limited conductive losses
- Different base materials (Si, Alumina, …)
- Compatible with single-phase and evaporative cooling (e.g.: $\mathrm{CO_2}$)
- Relatively high cooling power up to order of $> 1\mathrm{W/cm^2}$
- High thermal cooling performance due to the minimal distance to the coolant

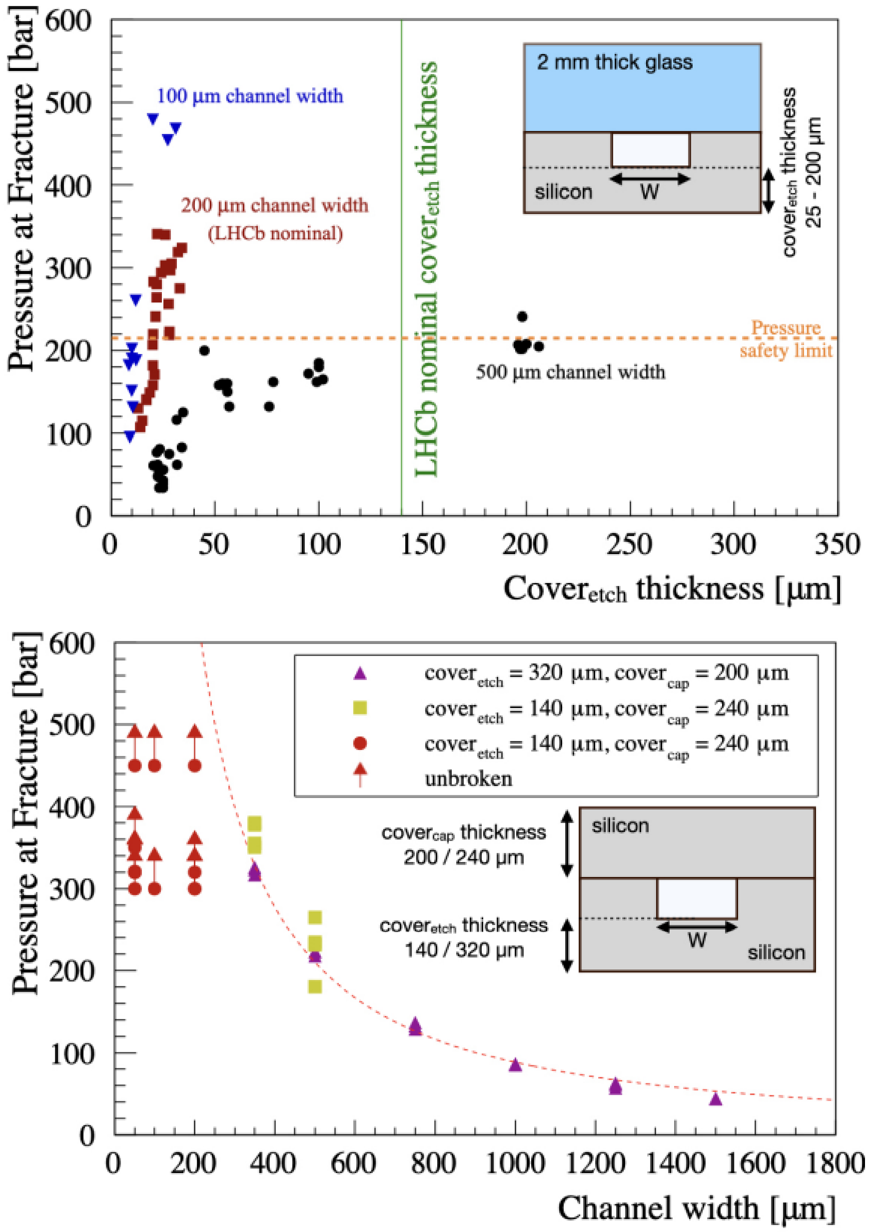
$$\mathrm{TFM} = \frac{\Delta T_{\mathrm{heater-output}}}{\mathrm{Power/cm^2}} =< 1.5\mathrm{K/(W/cm^2)}$$

- Vacuum compatibility (if needed)
- Very thin / Very low material budget $0.15 - 0.5\% X_0$
- Able to hold high pressure



The N62 Giga Tracker (j.nima.2016.06.045

How thin can it be? (Pressure resistance)



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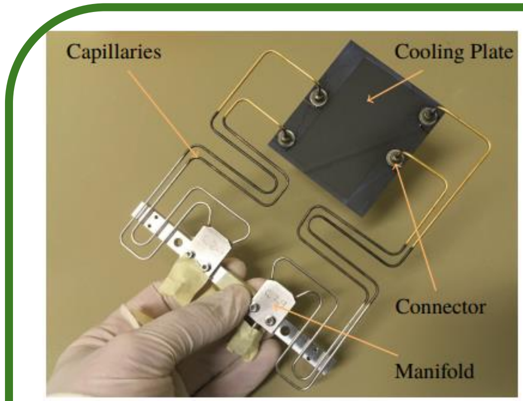
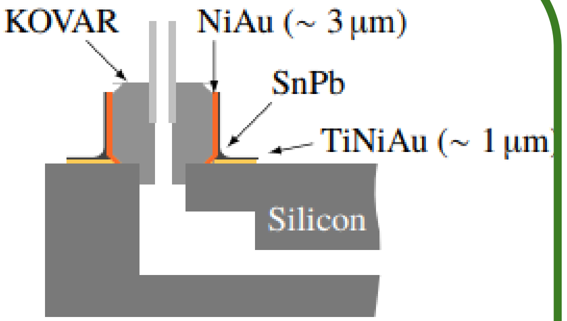
Past microchannel projects at CERN

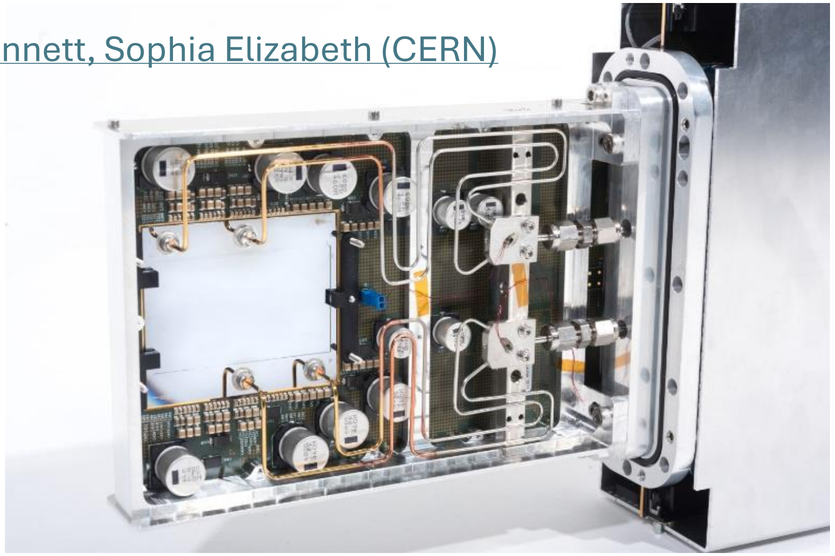




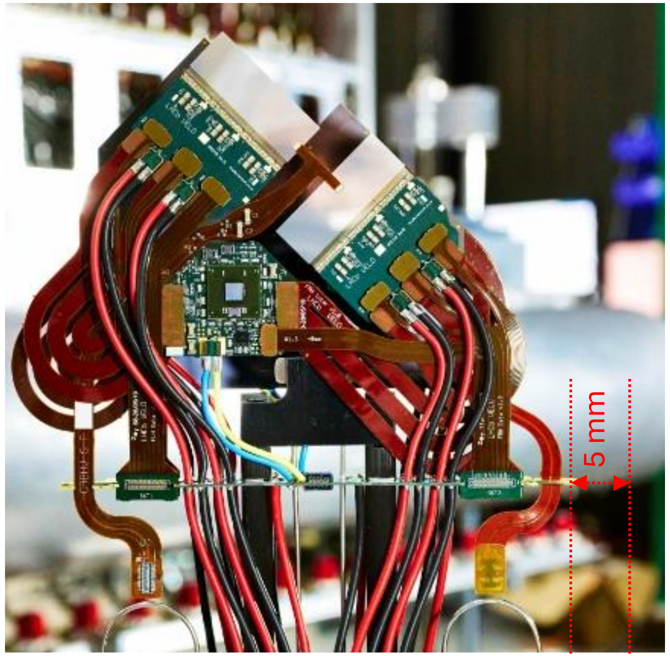
JINST **14** P07010

NA62 GTK

Bennett, Sophia Elizabeth (CERN)



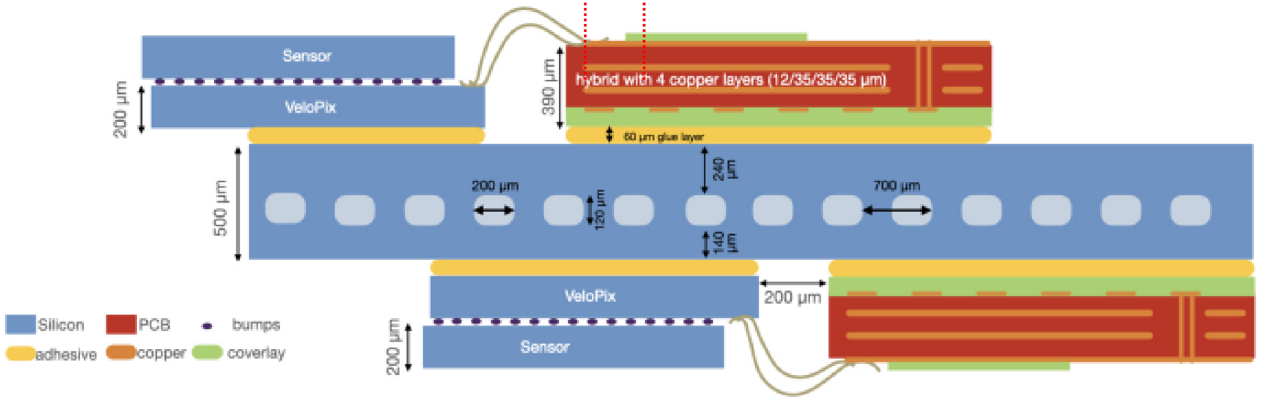
0.5% X_0, 200x70 μm^2 micro-channels, C6F14 liquid coolant, vacuum, 0.32 W/cm2 in the pixel matrix, < 5C



0.4-0.9% X_0 (innermost region)
ASIC/Sensor overhangs by 5 mm
Micro-channels 120x200 μm^2,
CO2 bi-phase, $1 W/cm^2$,
Sensor < $-20°C$, vacuum

j.nima.2022.166874

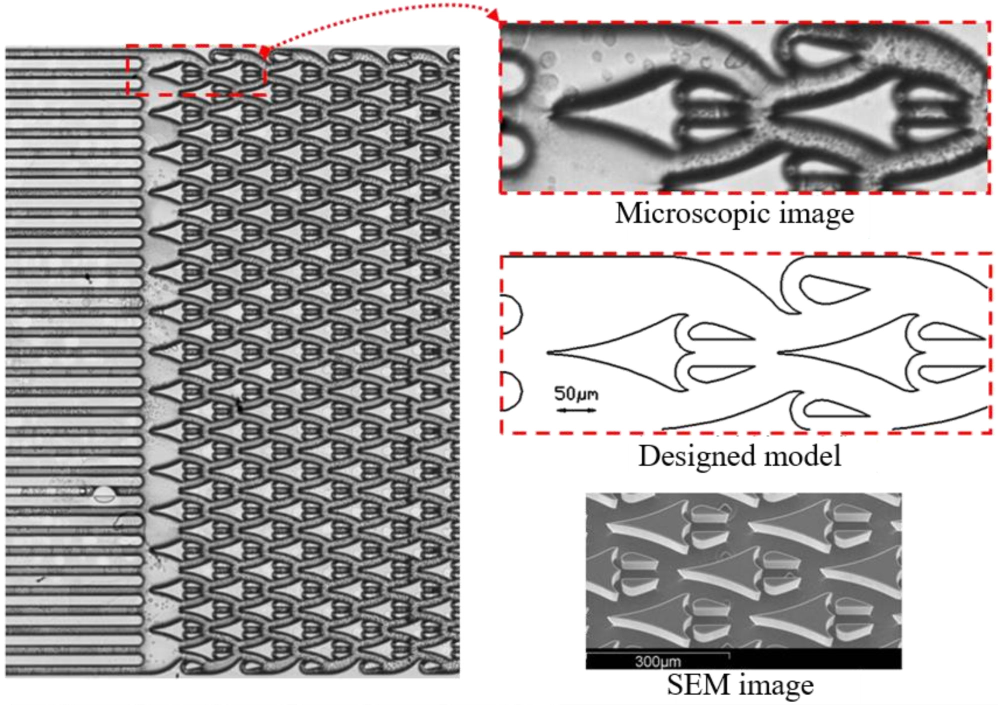
Brice, Maximilien; Ordan, Julien Marius (CERN)



LHCb VELO Upgrade I

Standard DRIE microchannels (Deep Reactive Ion Etching)

More information here



Microscopic image

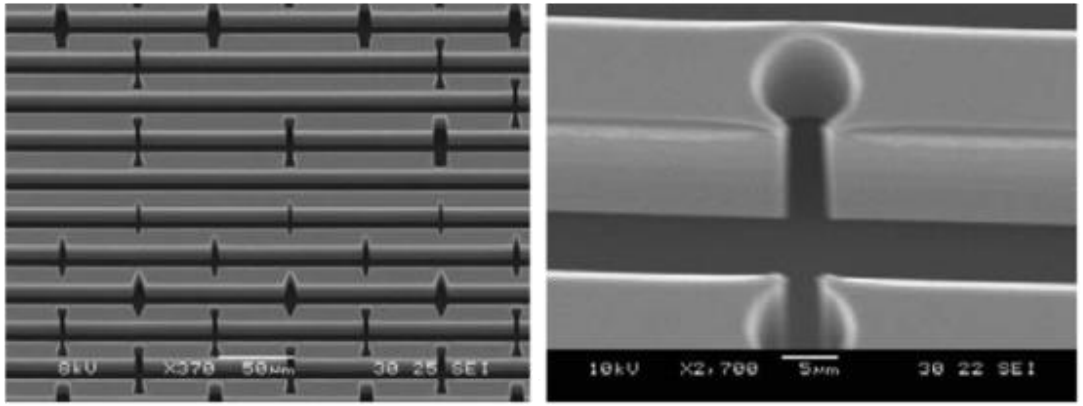
Designed model

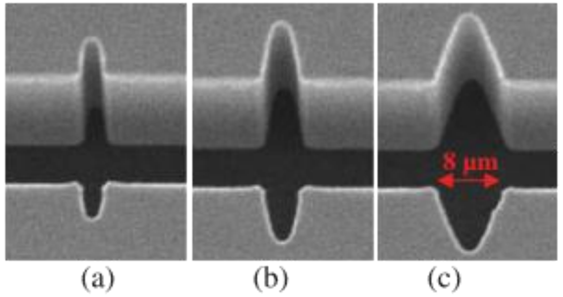
SEM image

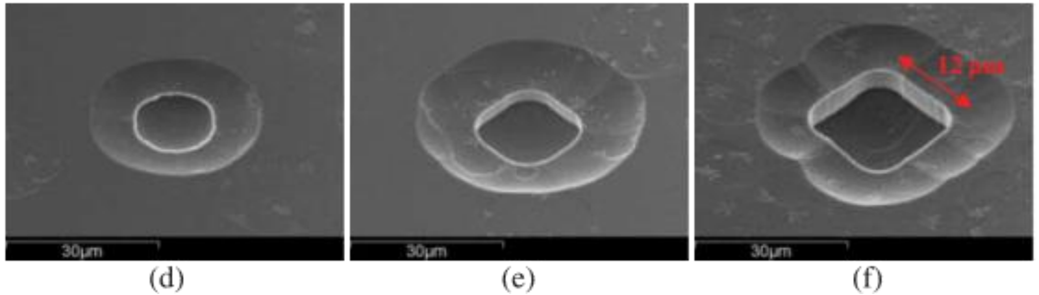
Standard DRIE process

- Higher material budget
- Cover plate needed and bonding required
  (Silicon to glass / silicon to silicon)
- Complex 2.5D structures are possible

Structural improvements (restrictors, nucleation sites…)





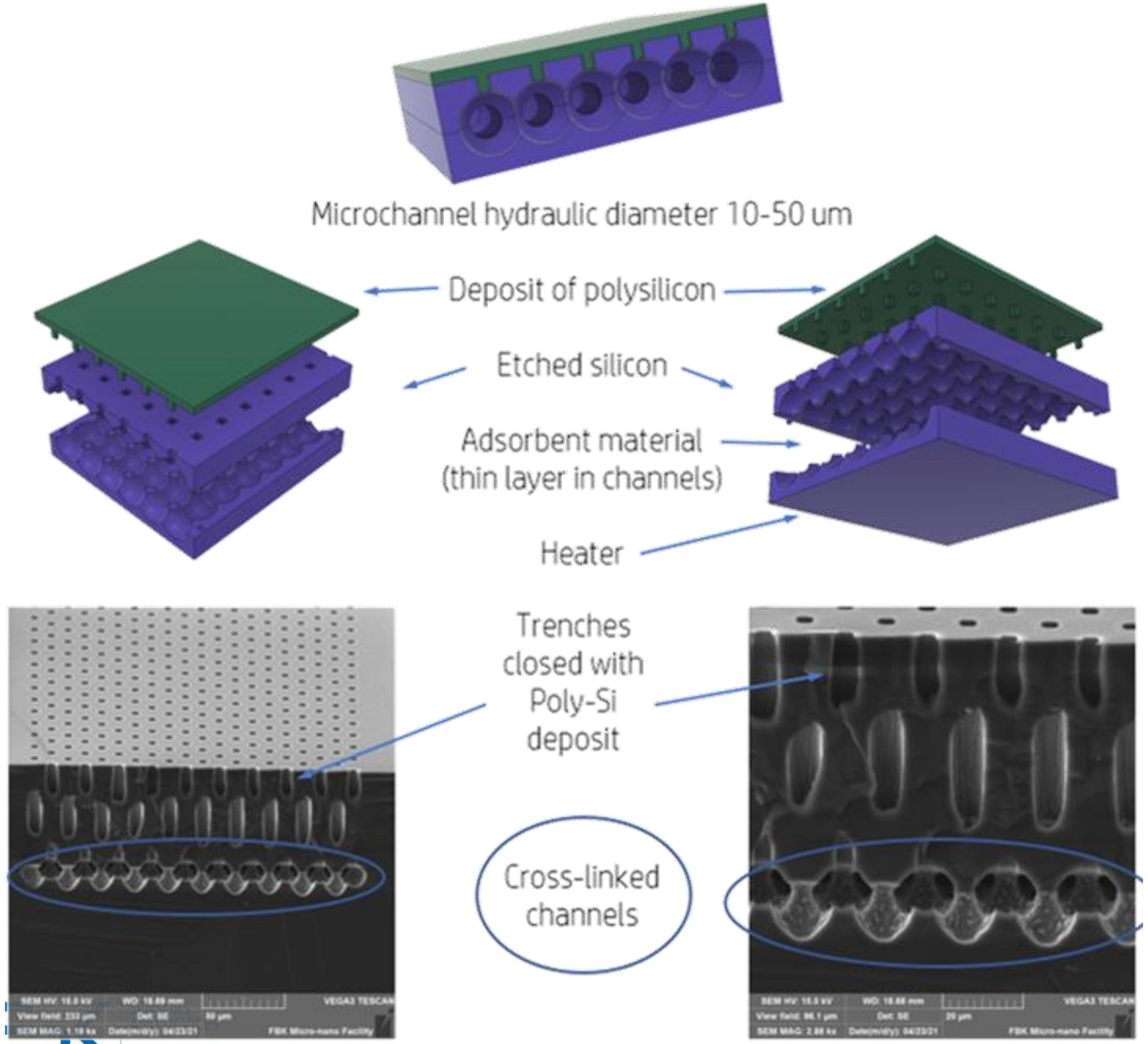


asitar@fbk.eu

More information here

Buried microchannels (BCT – Buried Channels Technology)

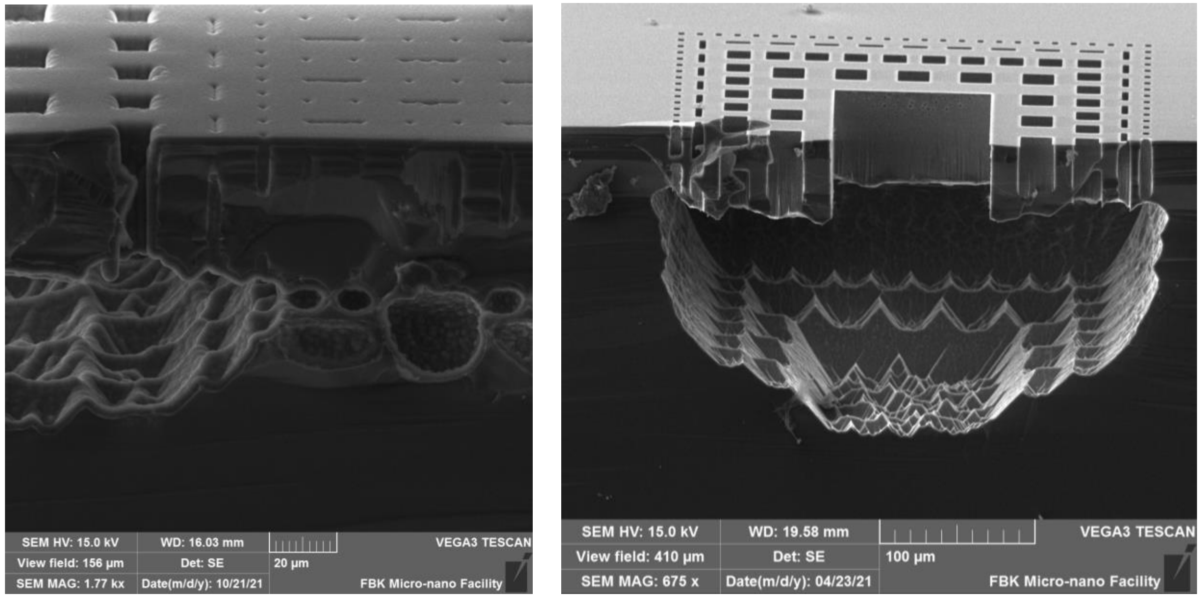
Large surface area in a cross linked micro fluidics to enhance solid/gas interaction.



Buried microchannels

- Low material budget
- No bonding required
- Round structures are possible
- A 3D method

Interconnected channels, interconnections / ports



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DRD8.3.2: Microchannels

- Improved microchannel developments are in the DRD8-WG3.2
- Cost reduction, integration of additional features to microchannels cooling plates and innovative cooling techniques
- R&D phase space:
  - Low material budget (from $\sim 0.5\% \mathrm{X}_0$ to below $0.2\% \mathrm{X}_0$)
  - Different power densities: low $(10 - 100\mathrm{mW/cm^2})$, high-power ($\gtrsim 2\mathrm{W/cm^2}$) and ultra-high-power densities ($> 100\mathrm{W/cm^2}$)

1 Silicon microchannels: integration

IMB-CNM, IFIC, DESY

- ‘Belle II’-like ladder prototype
- ‘active interposers’ and CMOS compatible process

2 Silicon microchannels: hyperbaric bonding

CPPM, LEGI, LPNHE, LPSC

- Alternative bonding process to reduce manufacturing cost

3 Ceramic microchannels

University of Manchester, CERN

- Manufacturing via low temperature co-firing ceramics

4 Jet impingement cooling

Purdue University, CERN

- Very high heat transfer coefficient
- Compatible with high-power density

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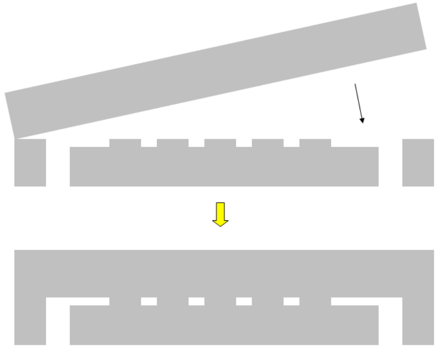
Snapshot Status at IMB-CNM, DESY, IFIC

Previous Work

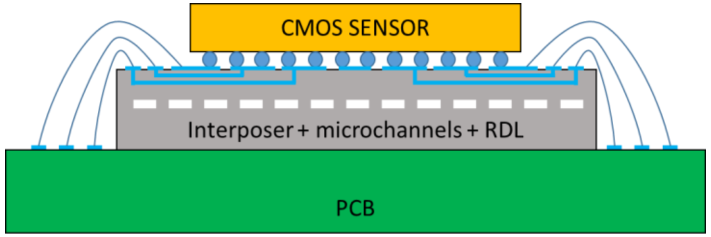
- Base embedded microchannel technology developed at IMB-CNM, using DRIE and wafer bonding techniques
- Exploring different technological options compatible with CMOS sensors for applications in heterogeneous and monolithic integration
- Full mechanical characterization of anodic and eutectic wafer bonding



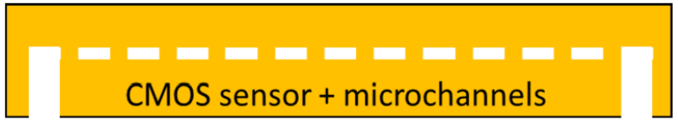
Anodic: Borosilicate Glass – Si
-High V (1000 V)
-Low T (~350 ºC),
-PYREX®, MEMpax®

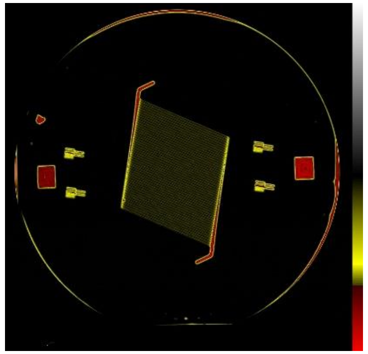
Eutectic: Si – Metal Layer – Si
-Low T (~400 ºC)
-Au layer

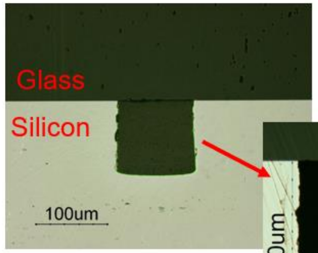
Heterogeneous Integration

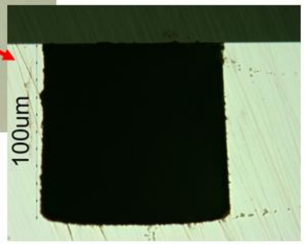


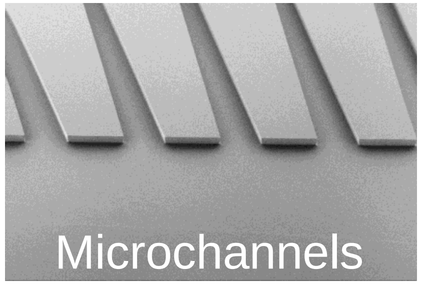
Monolithic Integration

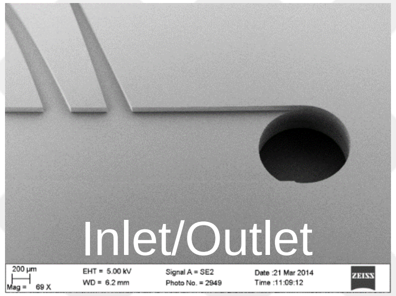












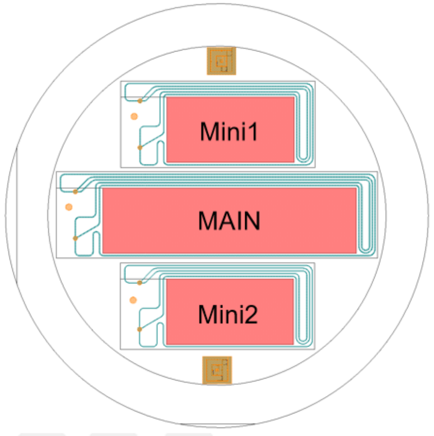
1 Snapshot Status at IMB-CNM, DESY, IFIC

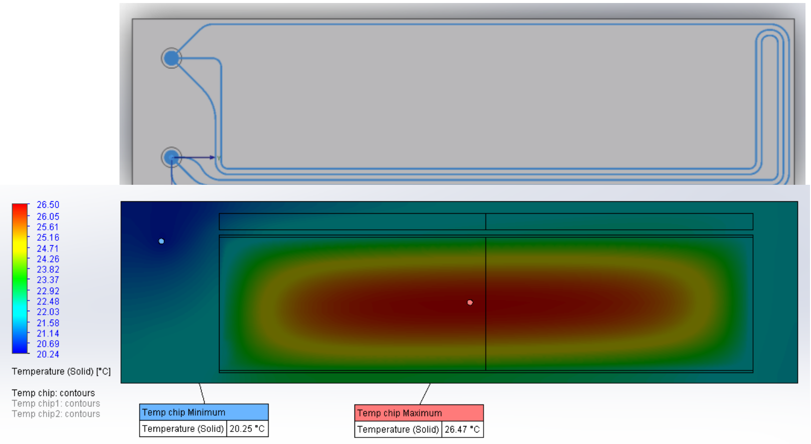
On-going Work

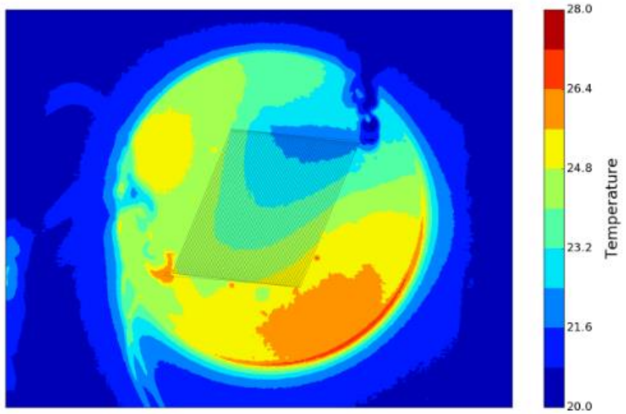
- Upgradse testing setup at DESY for fluidic and thermal characterization, and developing new capabilities (IR thermography, Fluorescence measurements, CFD simulations)
- Exploring different solutions for the development of cooling microchannels fully compatible with CMOS sensors
  1. RDL and microchannels on different wafers. Several fabrications on-going at IMB-CNM
  2. RDL and microchannels on same wafer. Fabrication concluded last week, characterization on-going
- Developing a ‘Belle II’-like all-silicon ladder prototype with embedded cooling microchannels, in collaboration with IFIC
  - Chip area thinned to 50 um, microchannels embedded in periphery
  - Optimization of cooling microchannels through simulations
  - Currently working on wafer layout, and definition of fabrication process

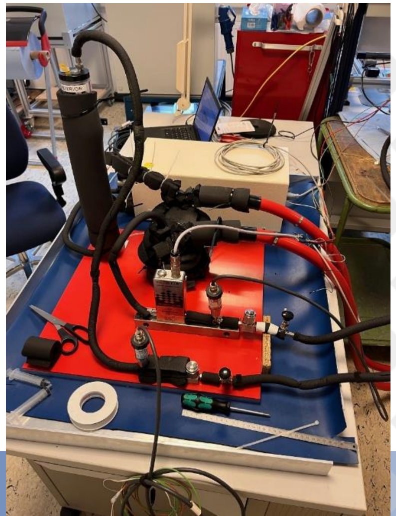
Future Developments

- More advanced interconnection technologies, such as RDL with several layers, Through-Silicon Vias (TSV), etc.







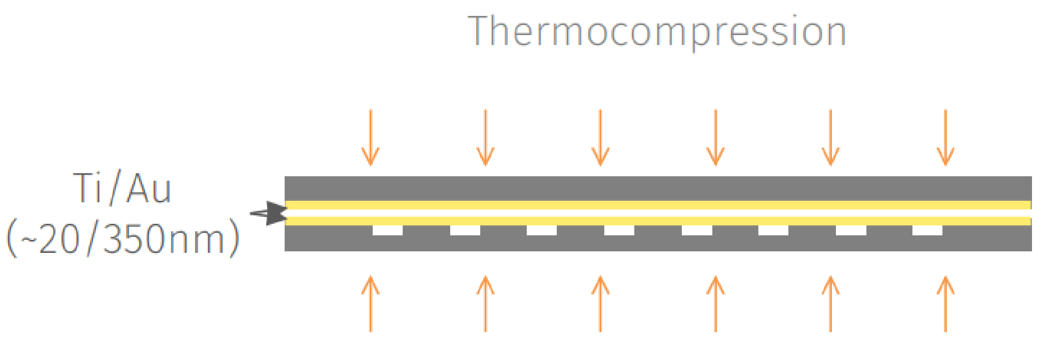


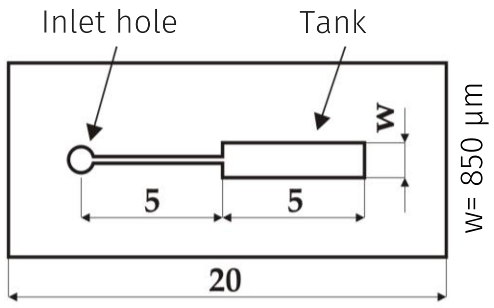
Silicon microchannels: thermocompression 2

In2p3 R&T on micro-cooling

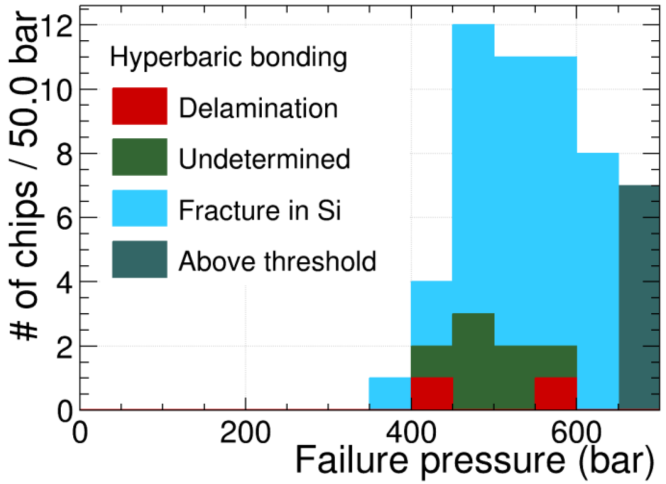
Focus on fabrication processes :

- Wafer « hyperbaric » bonding
  - Based on thermocompression of gold layers on both sides
  - Small samples containing a tank used for the high pressure validation
  - Even relative wide channels (850µm) can withstand very-high pressures (>350 bar)
  - Satisfies the minimum pressure for evaporative CO_2 cooling (186 bar)





Thickness : 2 x 0.5 mm



See the report at the last DRD8 collaboration meeting for more details on the full R&T program,

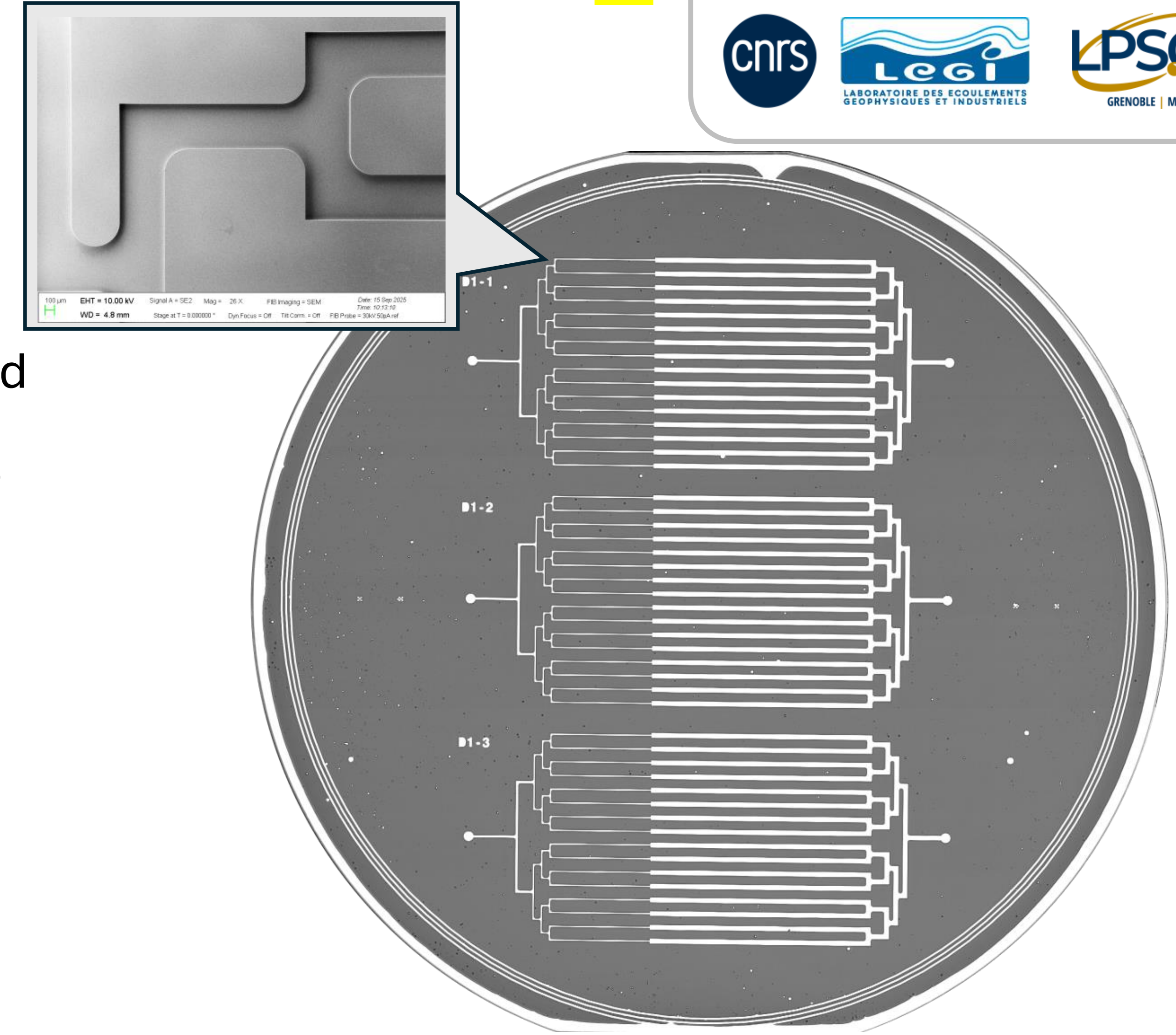
Silicon microchannels: thermocompression

2

In2p3 R&T on micro-cooling

Focus on fabrication processes :

- Wafer « hyperbaric » bonding
  - Very good bonding strength
  - Small remaining defects being worked on
  - 1st set of functional cooling plates to be tested in LPSC this year
- Fluidic connectors
  - Hyperbaric process nor standard thermocompression with gold succeeded (required flatness too high?)
  - Plans : new approach with anodic bonding of glass connectors (BF33) – more news soon in 2026

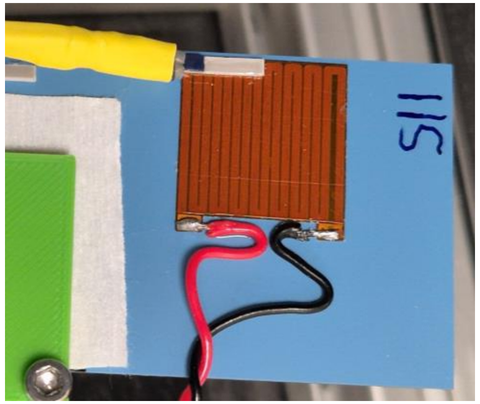


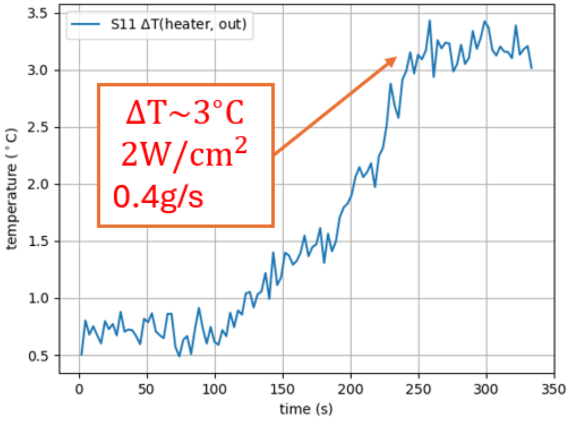
See the [report](#) at the last DRD8 collaboration meeting for more details on the full R&T program,

LTCC ceramics 3

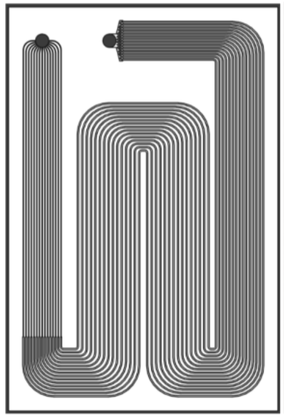
- **L**ow **T**emperature **C**ofiring **C**eramics (LTCC)
- Manufacturing through two companies: IKTS Fraunhoffer and Micro-Epsilon με
- Same substrate Dupont 951 (Alumina/Glass - 1:1)
- Summary:
  - Pressure tests successful up to 400μm channel wide samples up to 186 bar – CO$_2$ validation level
  - Pressure tests after irradiation up to 10^16 neq/cm^2 proton fluence (pressure > 350 bar)
  - Ultra-high vacuum compatibility verified by the CERN vacuum group
  - Good thermal performance measured in dry air box (1.5K/(W/cm^2))
    - Restriction 50 x 85 um
    - Main channel 85 x 180 um

Proof of principle with CO2 cooling



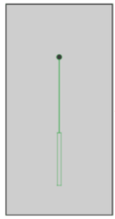


ΔT~3°C
2W/cm^2
0.4g/s

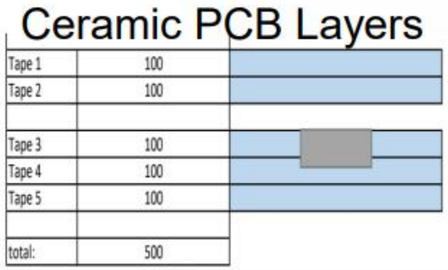


Circulation sample (40 x 60 mm2)

High pressure sample



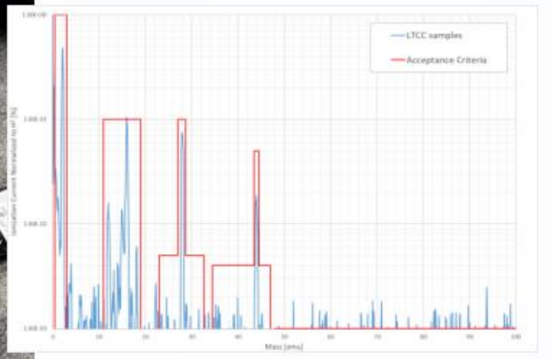
High pressure tests



Ceramic PCB Layers

Tape 1	100
Tape 2	100
Tape 3	100
Tape 4	100
Tape 5	100
total:	500

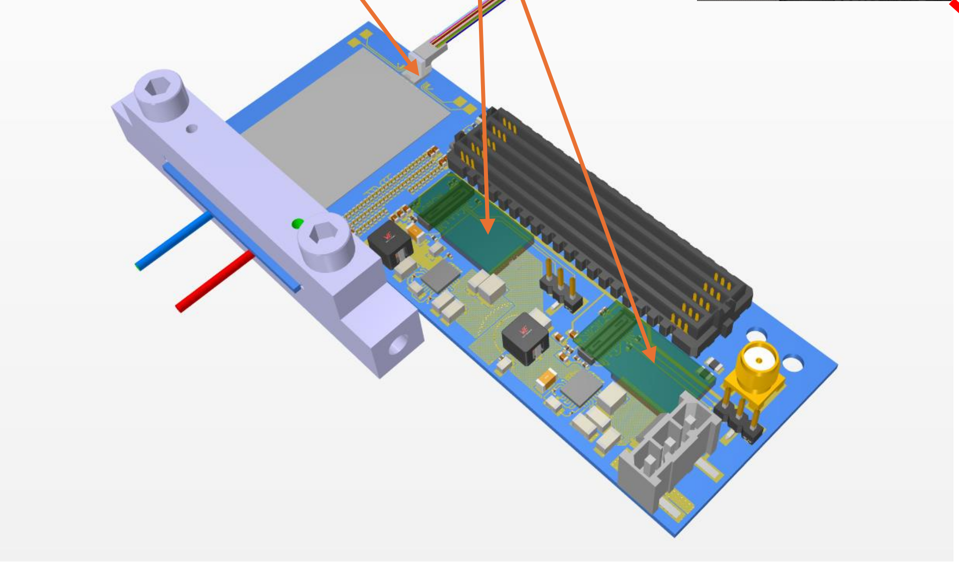
Ultra-high vacuum validation



Towards integration of electronics and cooling 3

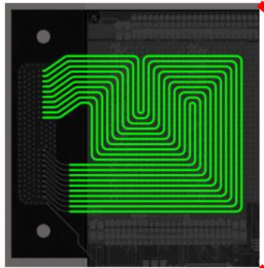
Design finished, in process of validating signal / power integrity with simulations

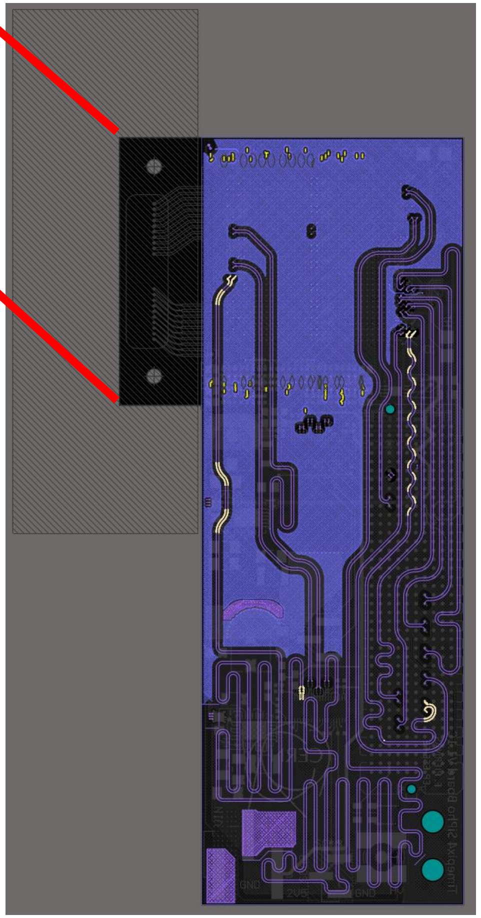
Two data transmission possible in this prototype: SiPhotonics or VRTx+



Through silicon vias Timepix4 on Top Layer

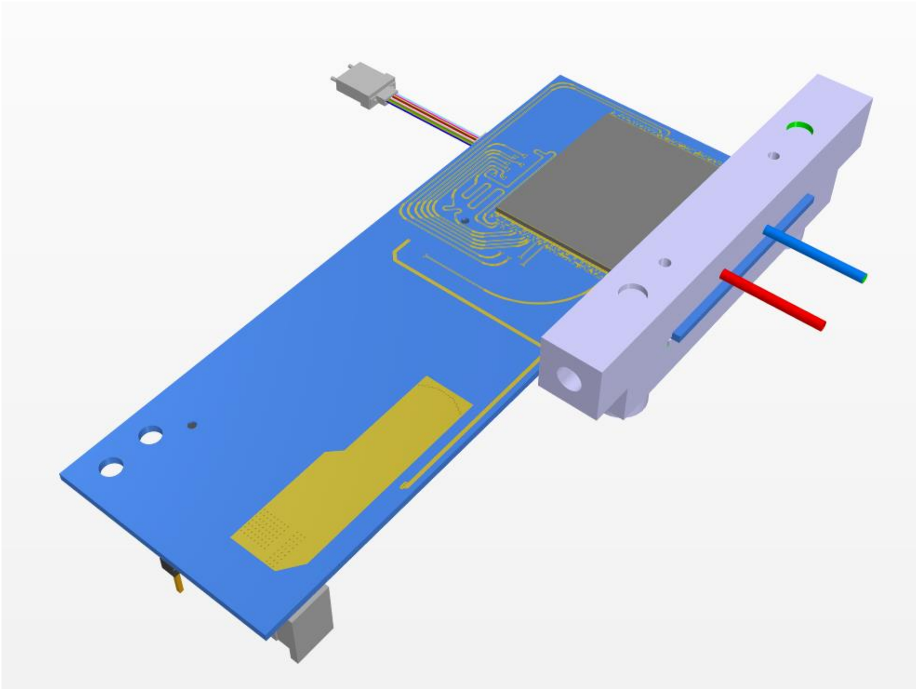
Cooling channels





Routing Layer

With long tracks for channels (to test signal integrity)
Layer also used for VDD_1V2A



Wire-bonds Timepix4 on Bottom Layer

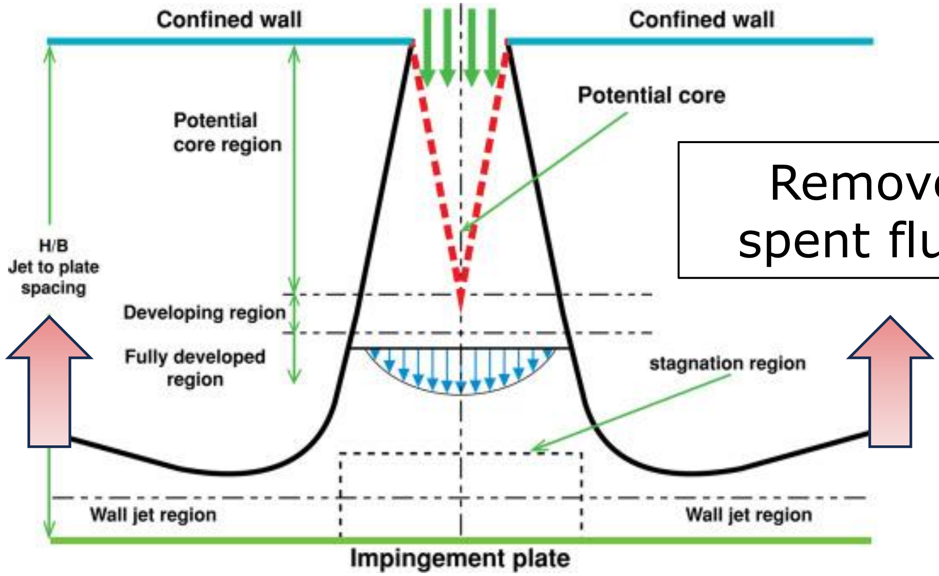
Work in progress!

EP-ESE
ELECTRONIC SYSTEMS FOR EXPERIMENTS

Francisco Piernas, fran.piernas@cern.ch

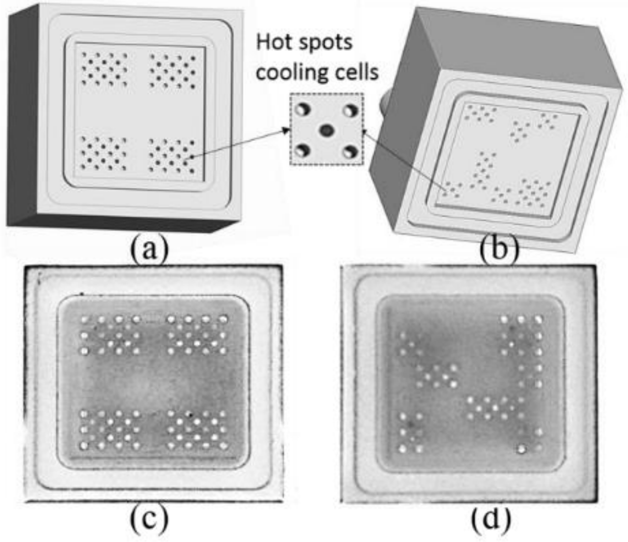
4 Jet Impingement

- Jet impingement is a cooling method that developing boundary layers to remove large quantities of heat in the stagnation region
  - As jets spread from the stagnation region to the wall jet region, they become less effective at removing heat
- Jets are arrayed to have cooling over large surfaces and reduce the poor heat transfer of the wall jets
  - When using large arrays, the jets begin to interfere with each other
  - This reduces heat transfer where two jets meet
- Alternating inlets and outlets are used to remove spent fluid to avoid jet interference and maintain good heat transfer performance
- Jets can be used to target hotpots for efficient cooling of uneven heat sources i.e. silicon in physics experiments
  - Compatible with very-high-power densities: larger than $100 \mathrm{W/cm}^2$ (j.applthermaleng.2011.03.017)



Remove spent fluid

S. Deshmukh et al., A review on liquid jet impingement for industrial cooling applications.

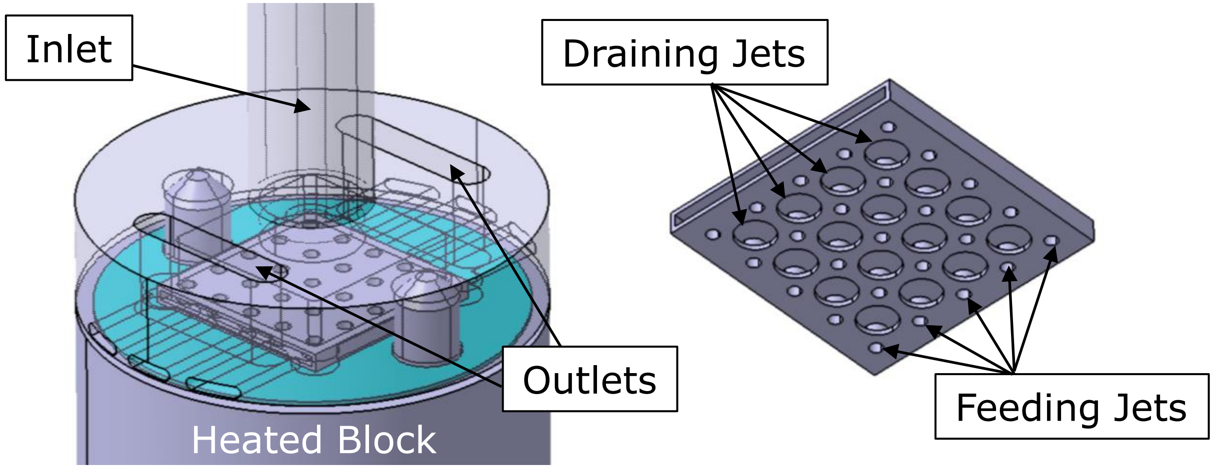


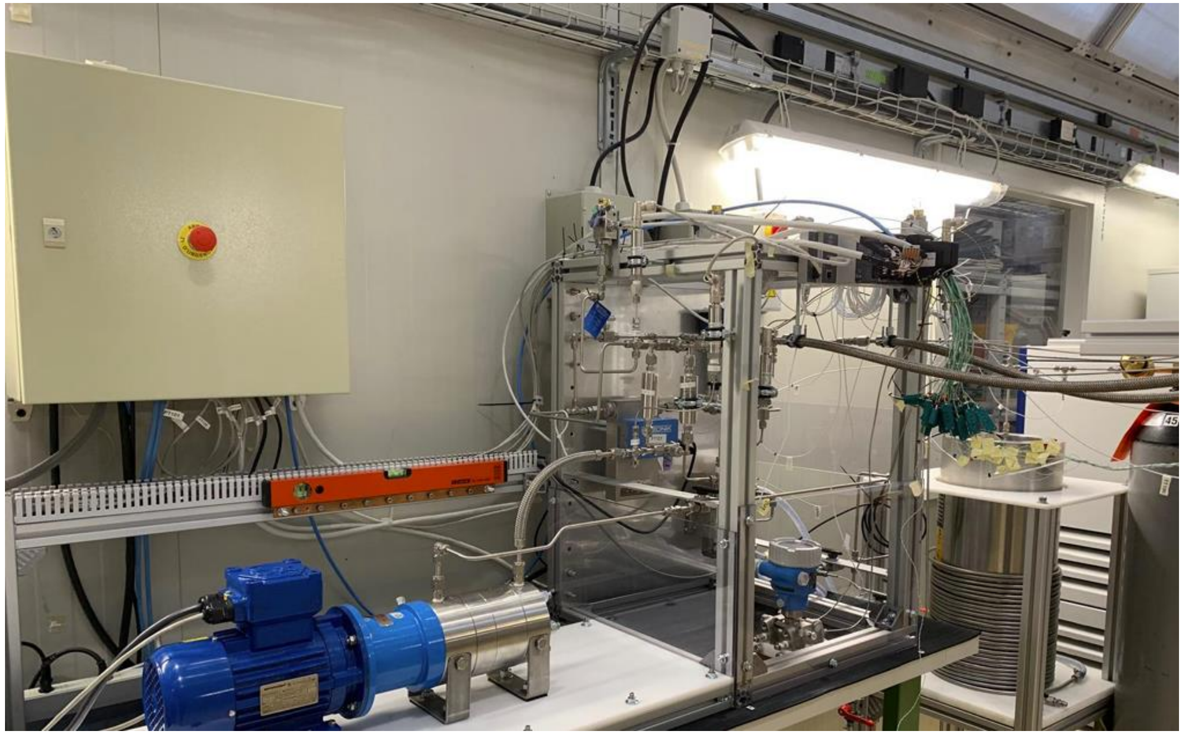
T. Wei et al., Low-cost energy-efficient on-chip hotspot targeted microjet cooling for high-power electronics

4

Test Setup

- Simulations of single-phase jet arrays are completed
- Testing apparatus is designed with heat source, pressure and temperature data
- Simulation validation and two-phase CO2 exploration will occur at CERN using the SASS (Scientific Assessment of Supercritical State) setup.
    - Minimum temperature of 5C
    - Pressures between 50bar – 120bar
    - Flow rates between 0.5g/s – 11g/s
- Operation points are between 50-60 bar and 5C to saturated liquid conditions
    - This allows investigation of single and two-phase jets





SASS Setup - Camila Pedano-Medina

Conclusion

- Cooling requirements leads to different solutions
  - Depends on total area/cost, thermal figure of merit, maximum operating temperature, vacuum, and integration aspects
- Microchannels cooing plates are a high thermal performance, low material budget and potentially vacuum compatible solution
  - Such structures can be manufactured in different base materials (Si, Ceramics, …)
- DRD8.3 cooling work package
  - Silicon microchannels
    - *Targeting low coolant pressure operations and aiming for better electronics integration via active-interposers and a CMOS compatible process (IMB-CNM, IFIC, DESY)*
    - *Cost reduction via alternative bonding technique: hyperbaric process (CPPM, LAPP, LPNHE-Paris, CNRS, LEGI, LPSC)*
  - Low temperature co-firing ceramics
    - *Alternative substrate with promising electronic integration capabilities and ultra high-vacuum compatibility (UoM, CERN)*
  - Impinging jets
    - *Aiming to achieve extremely high heat transfer coefficient between the heat source and* CO_2 *(liquid or evaporative) (Purdue University, CERN)*

Thank you very much for your attention! Questions?

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