

# A System-on-Chip (SoC) based High Resolution Time-to-digital converter (TDC) in Artix-7 FPGA

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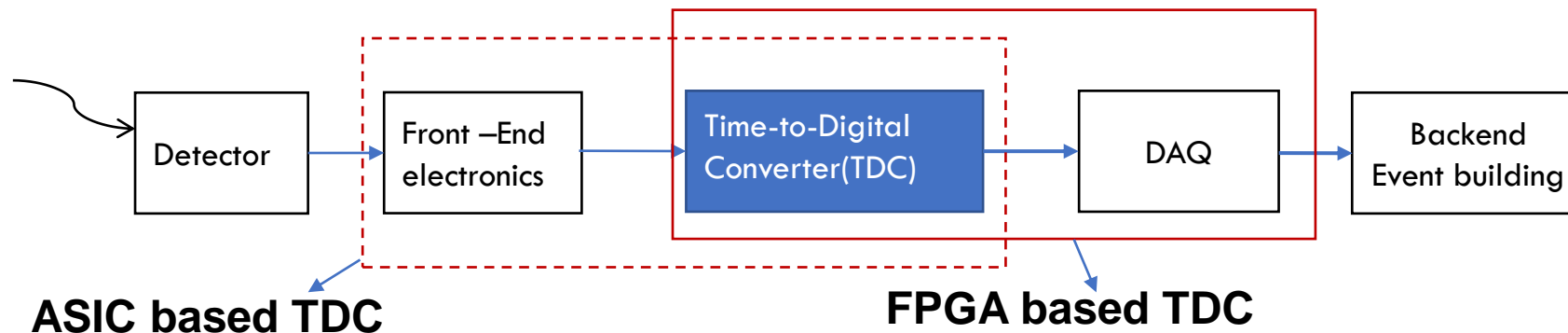
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- Introduction
  - Requirements
  - Applications
  - Time measurement techniques
- Spartan-6 FPGA-based TDC
- Moving Forward
  - Migration to 7-series FPGA
  - SoC Approach
  - High resolution: ~ 62 ps
  - Very-high resolution: ~ 32 ps
  - Ultra-high resolution: ~ 16 ps
  - Long range TDC : 1.5 seconds
- Conclusion

# Introduction: TDC Requirements

- Time interval (TI) measurement is an important requirement in various physics experiments
- Increased readout channels, improved timing specifications ( $<100$  ps).
- This increases the complexity of readout electronics in terms of time resolution, readout channels, space, and power consumption.
- These complex requirements are well complemented by advancements in integrated circuit technology in the form of Application Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs).



# Introduction: TDC Applications

Application/ specification	High-energy physics experiments	Nuclear physics experiments	TOF Mass spectroscopy	Laser range finding (LIDAR)	TOF-PET
<b>TOF detector</b>	Silicon strip and pixel detectors, MWPC, straw tubes, drift tubes, RPC, TPC	Scintillator, Semiconductor detectors	Microchannel plate (MCP)	Laser transmitters and optical detectors, SPAD	Fast scintillators like LYSO: Ce, LSO, and LaBr3
<b>Time Resolution</b>	~ sub-100 ps	~ 400 ps	< 100 ps	< sub-100 ps	~ 400 ps
<b>Dynamic range</b>	~ 10 to 100s of $\mu$ s	500 ns	10's of $\mu$ s	100 ns (meters)	10 ns
<b>No. of channels</b>	large	less	less	less	large
<b>No. of hits</b>	4 to 8	1	128	1	1
<b>Mode</b>	Trigger matching mode	Normal START-STOP	Common START	Normal/STARTS TOP	Normal/START-STOP

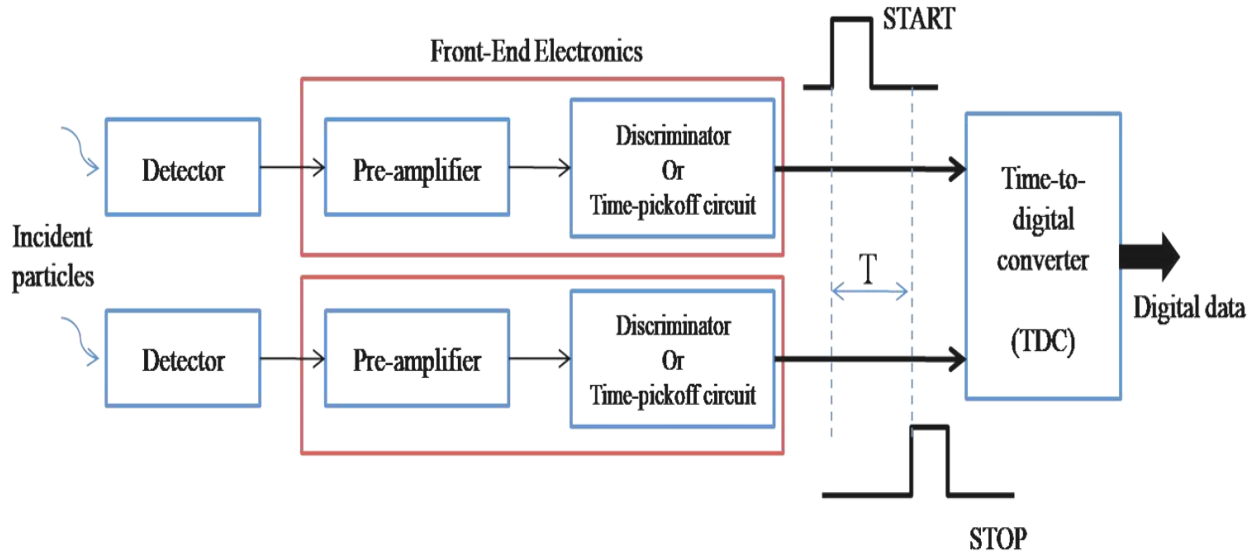
Raman fluorescence spectroscopy, Time-correlated Single Photon Counting(TCSPC)  
&  
**Detector characterization ..**

# Introduction: TDC Definition

## Definition

- Elapsed time interval between two or more events

A two-channel time interval measurement using TDC



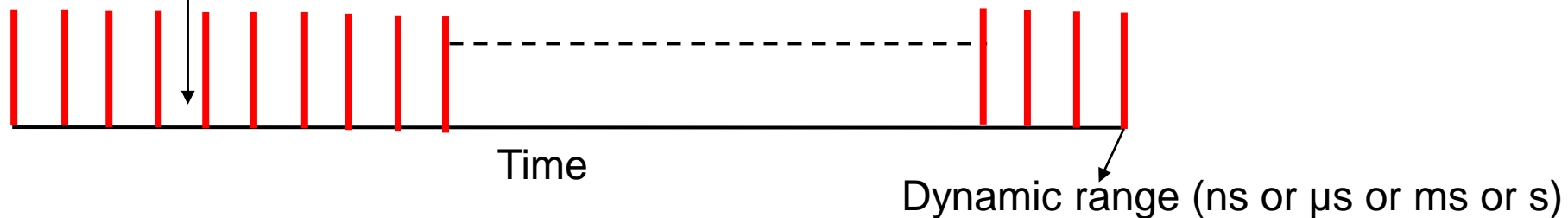
## Specifications

- Resolution (ps)
- Dynamic range ( $\mu$ s)
- Conversion time (ns)
- Linearity
- Precision (ps)
- No. of Channels
- No. of hits per channel
- Operation mode
- Power consumption

## Techniques

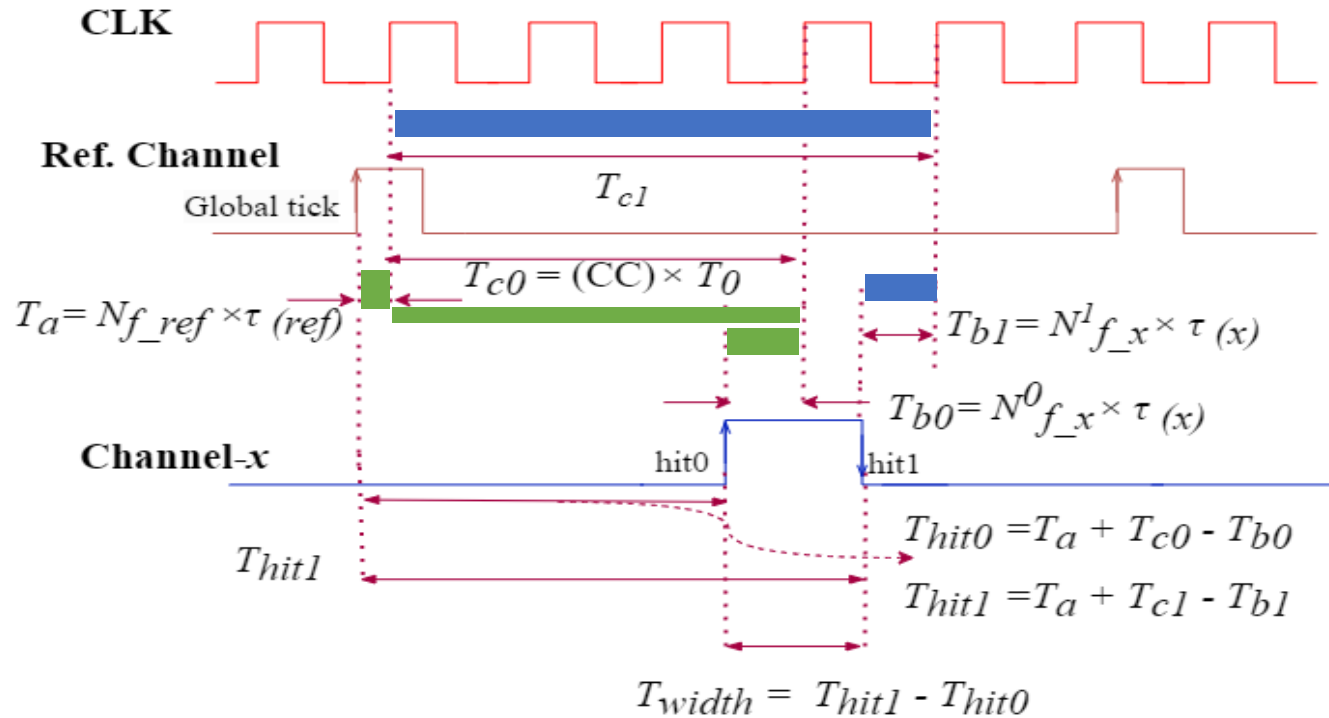
- Analog
- Vernier
- Interpolation techniques**
  - **Tapped delay line (TDL)**
  - Differential delay line
  - Multi-phase clock

Resolution (LSB) (ps)      Representation (time scale)



# Introduction: FPGA TDC: TDL Interpolation Technique

## Timing diagram for dual hit time measurement



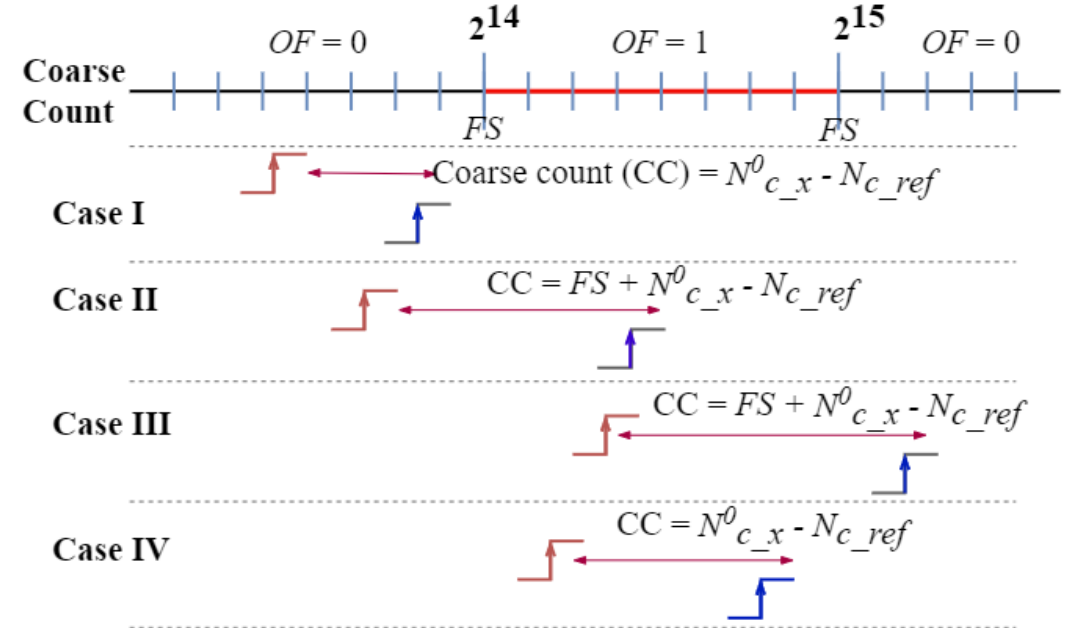
## Equations

$$T_{hit0} = (CC) \times T_0 + (N_{f\_ref} \times \tau_{(ref)}) - (N^0_{f\_x} \times \tau_{(x)})$$

$$T_{hit1} = (CC) \times T_0 + (N_{f\_ref} \times \tau_{(ref)}) - (N^1_{f\_x} \times \tau_{(x)})$$

$$T_{width} = T_{hit1} - T_{hit0}$$

## A sliding scale technique

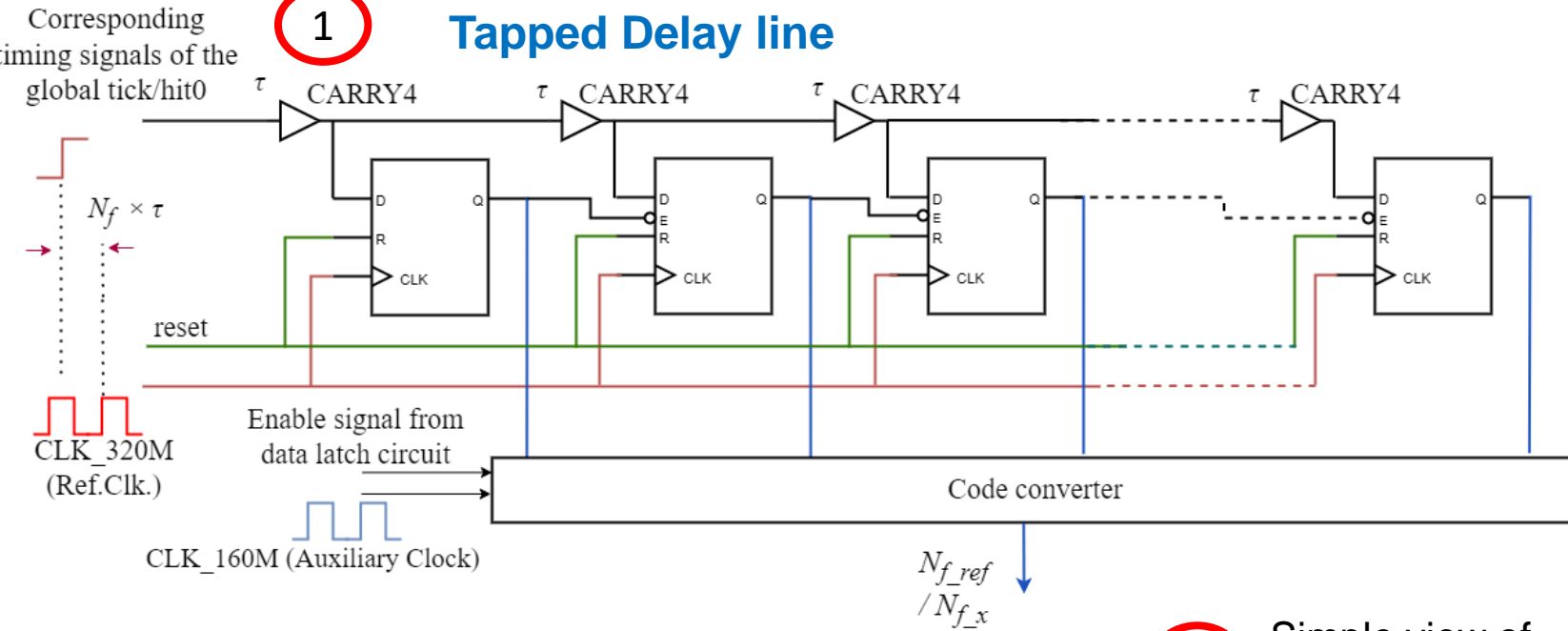


- Free running counter -no need to reset the counter
- **Sliding scale technique**
- Continuous measurement without loss of events
- Trigger Matching mode

K. Hari Prasad, et.al, NIMA, 168657, 2023

# Introduction: Key points in TDL Based FPGA TDC

## 1 Tapped Delay line



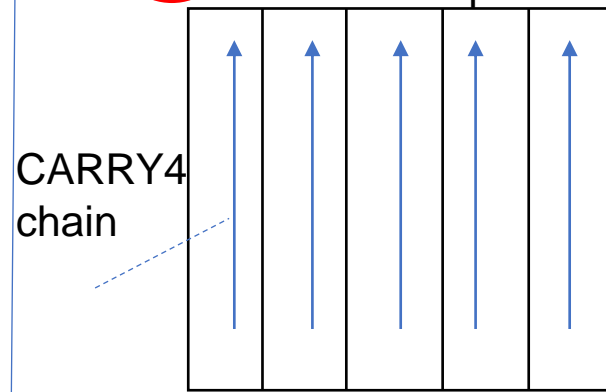
$$K_{max} \times \tau_{(x)} \geq T_0$$

$K_{max}$  : No of delay elements required to cover one  $T_0$

### Delay line calculations

**Trade-off** : Clock frequency Vs. No of delay elements  
Vs Power consumption

## 3 Simple view of FPGA floor plan



No. of columns decides No of channels to be accommodated

## 4 Calibration statistical code density test

### Average Bin-width calibration

$$\tau_{LSB} = T_0 / (K_{max})$$

Suitable for mid-resolution TDCs (~ 50 ps)

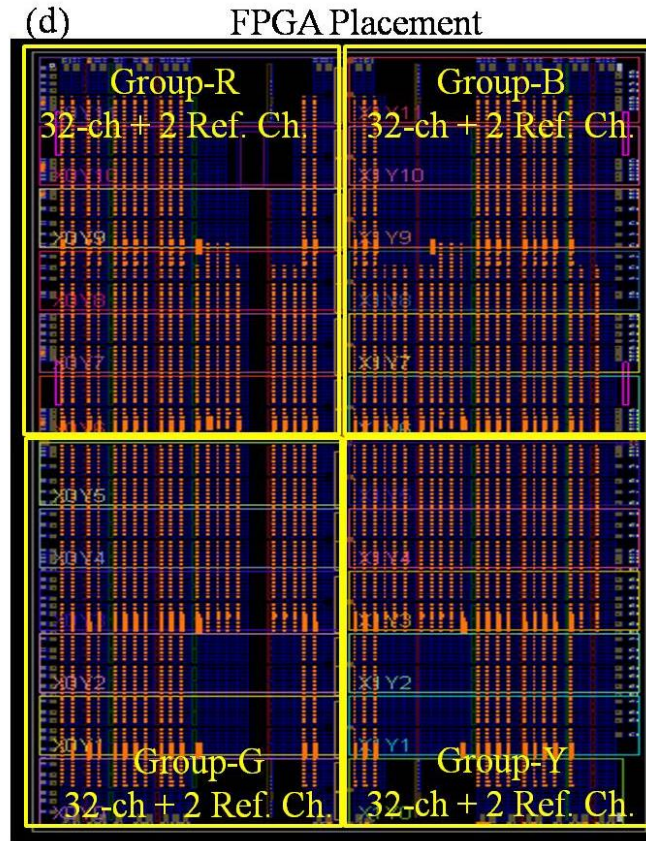
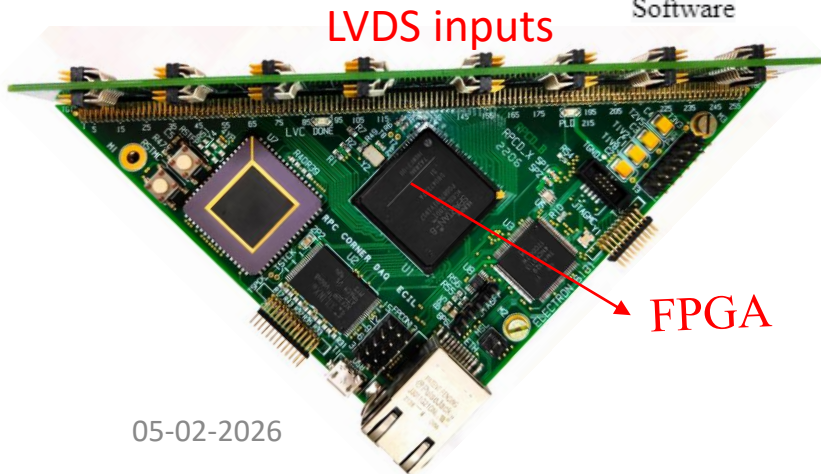
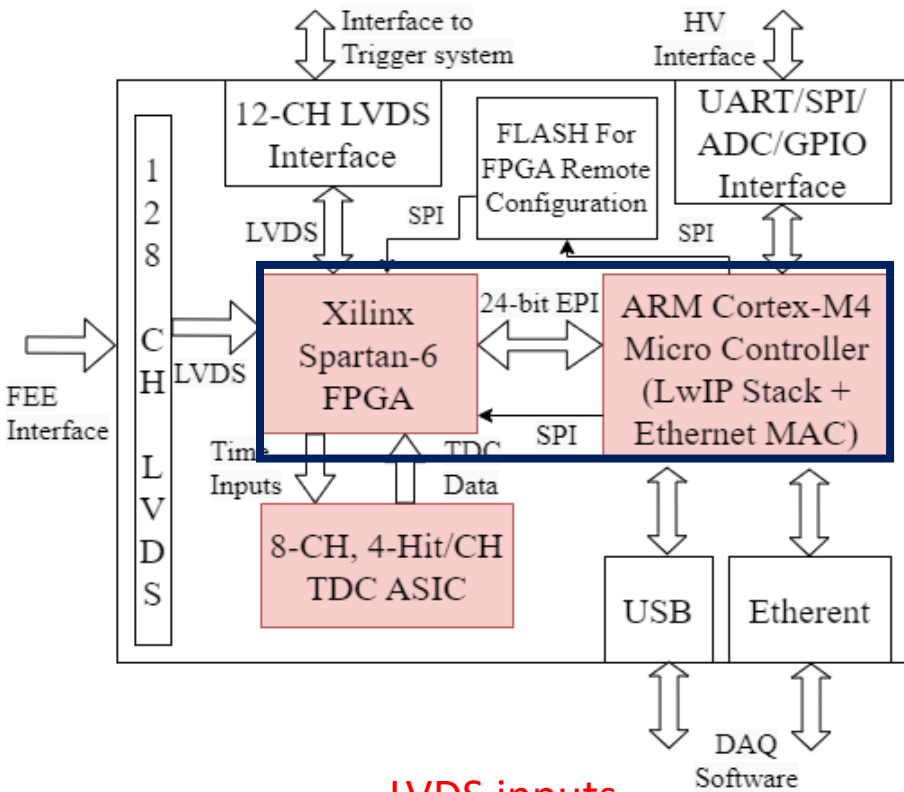
### Cell-to-cell or bin-to-bin calibration method

*Cumulative weightage of each bin*

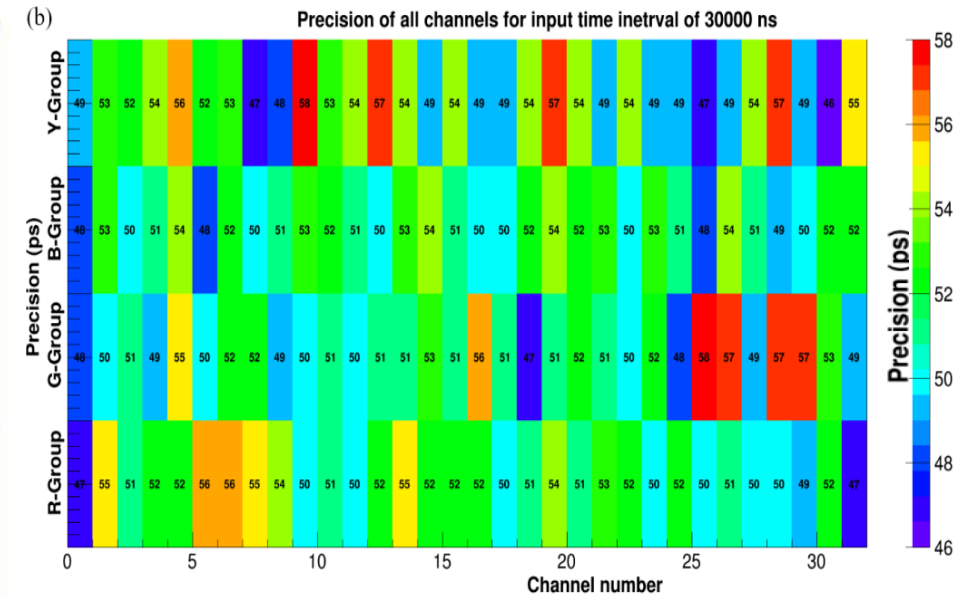
Required for Very high resolution TDCs (< 20 ps)

# Spartan-6 FPGA TDC: 129 channel TDC with 82 ps LSB

## System Block Diagram and Board



## FPGA Placement of 129-channel TDC



- Single-shot precision of 46 ps (0.49 LSB) to 58 ps (0.68 LSB) across channels at 30  $\mu$ s input.
- 7 mW/channel power consumption

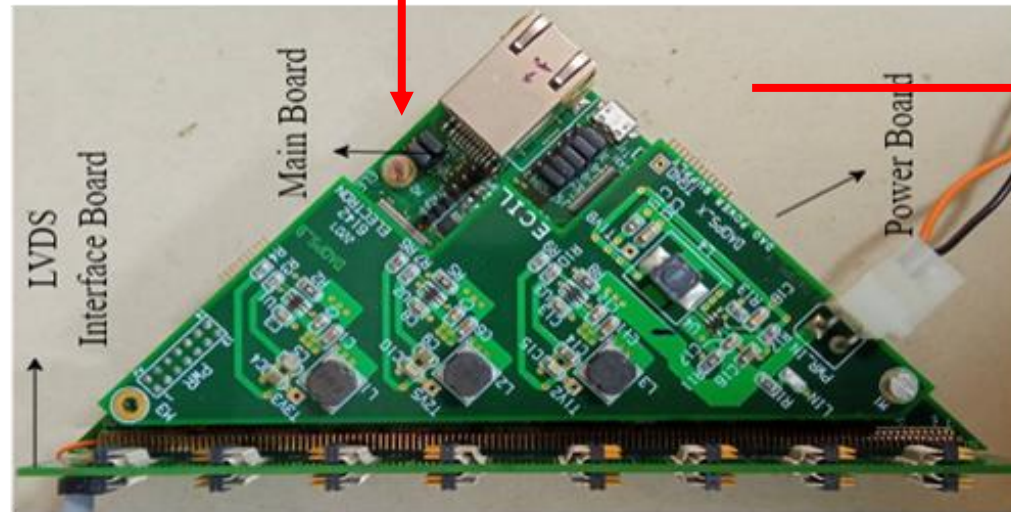
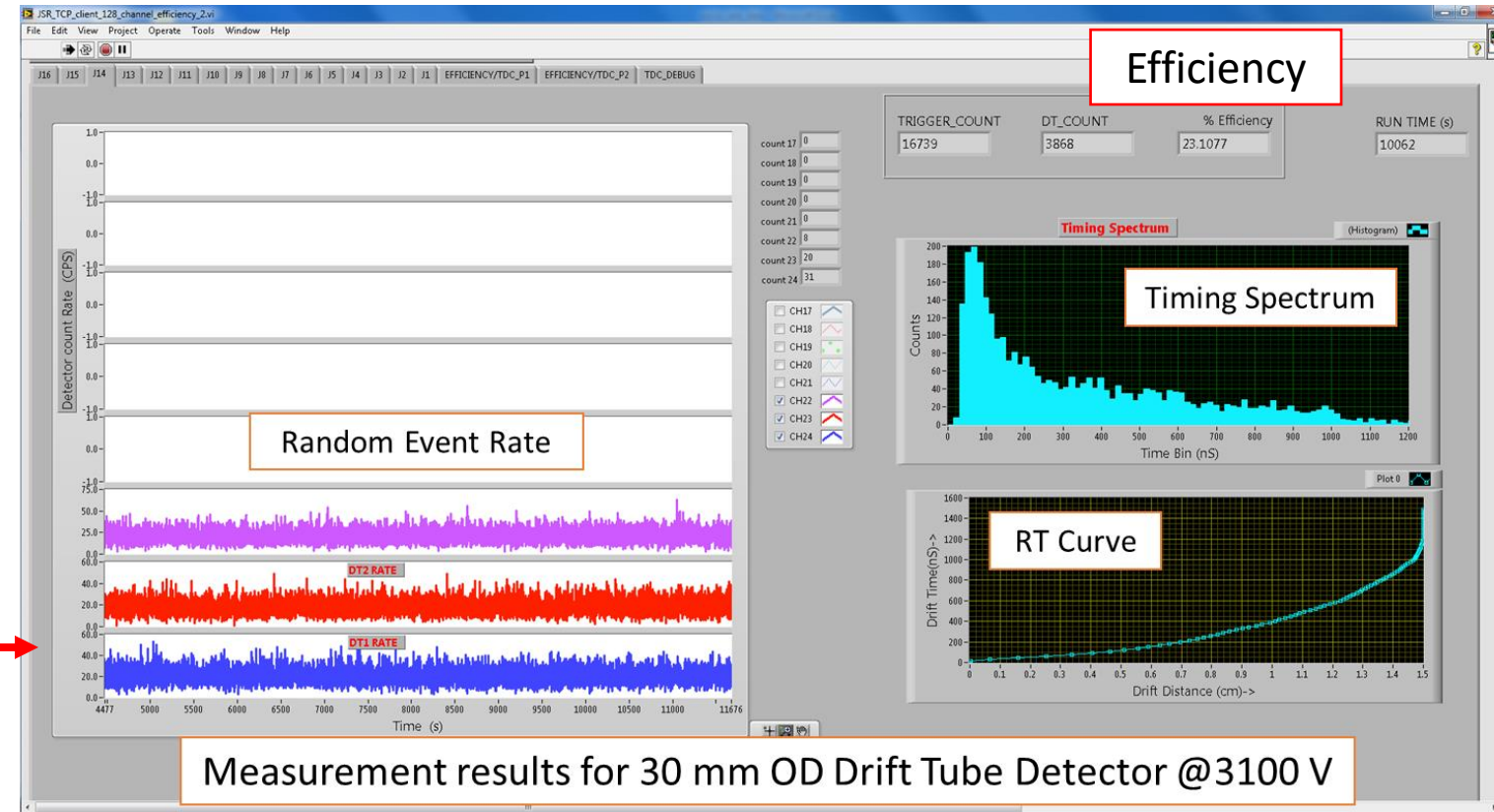
For detailed test results please see the slides 19-21

# Spartan-6 FPGA TDC based DAQ with drift tube detectors

## Drift tube stack with ANUSPARSH FEE



## User interface



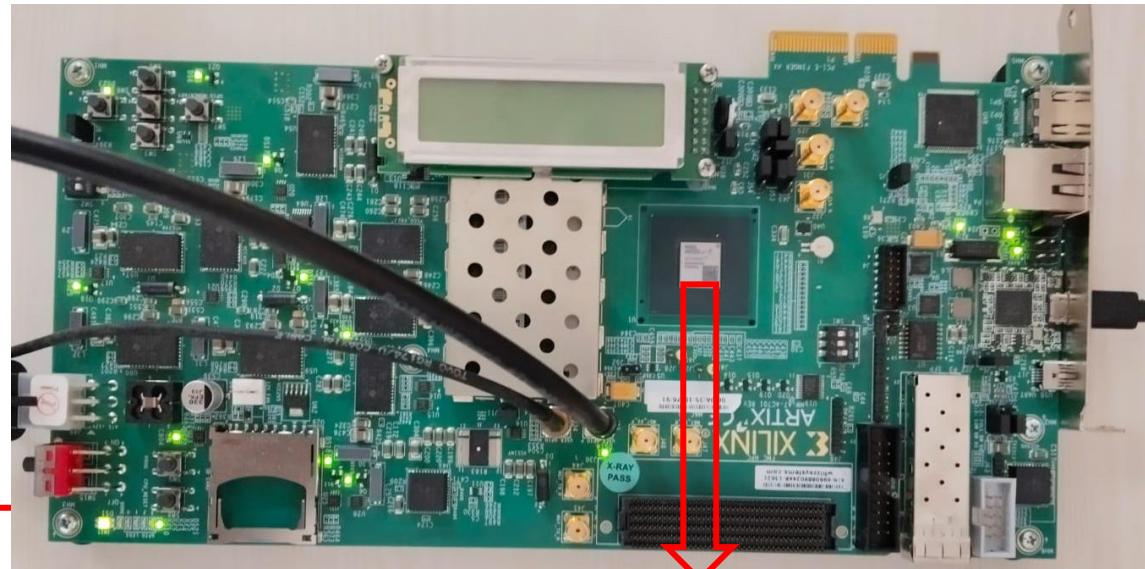
- DAQ parameters like rate, efficiency measurements, trigger processing along **with time measurement** in a single FPGA.

## 128-channel FPGA TDC based DAQ

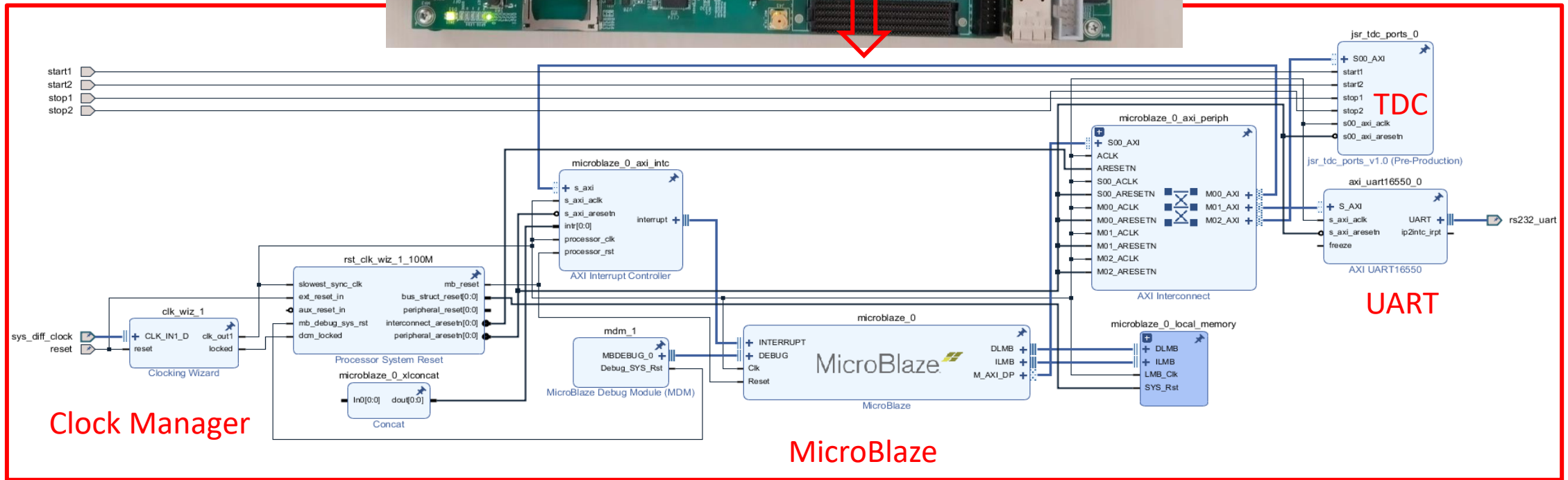
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# Artix-7 FPGA TDC : SoC approach

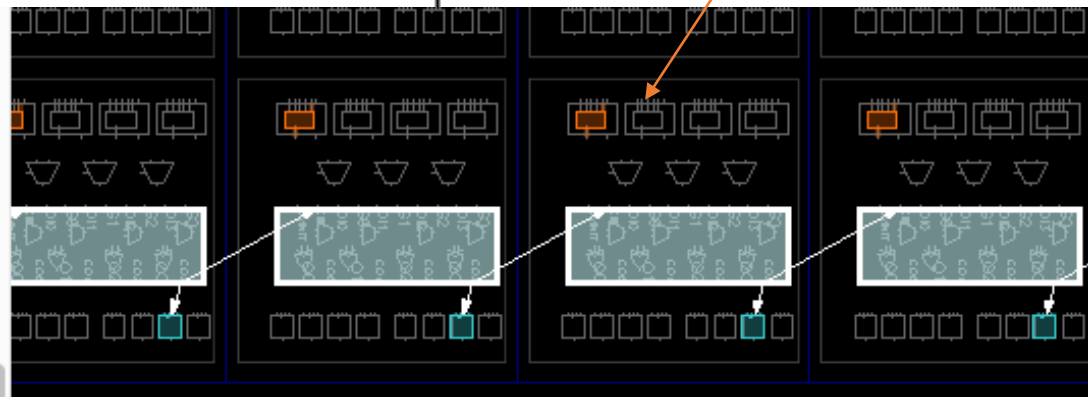
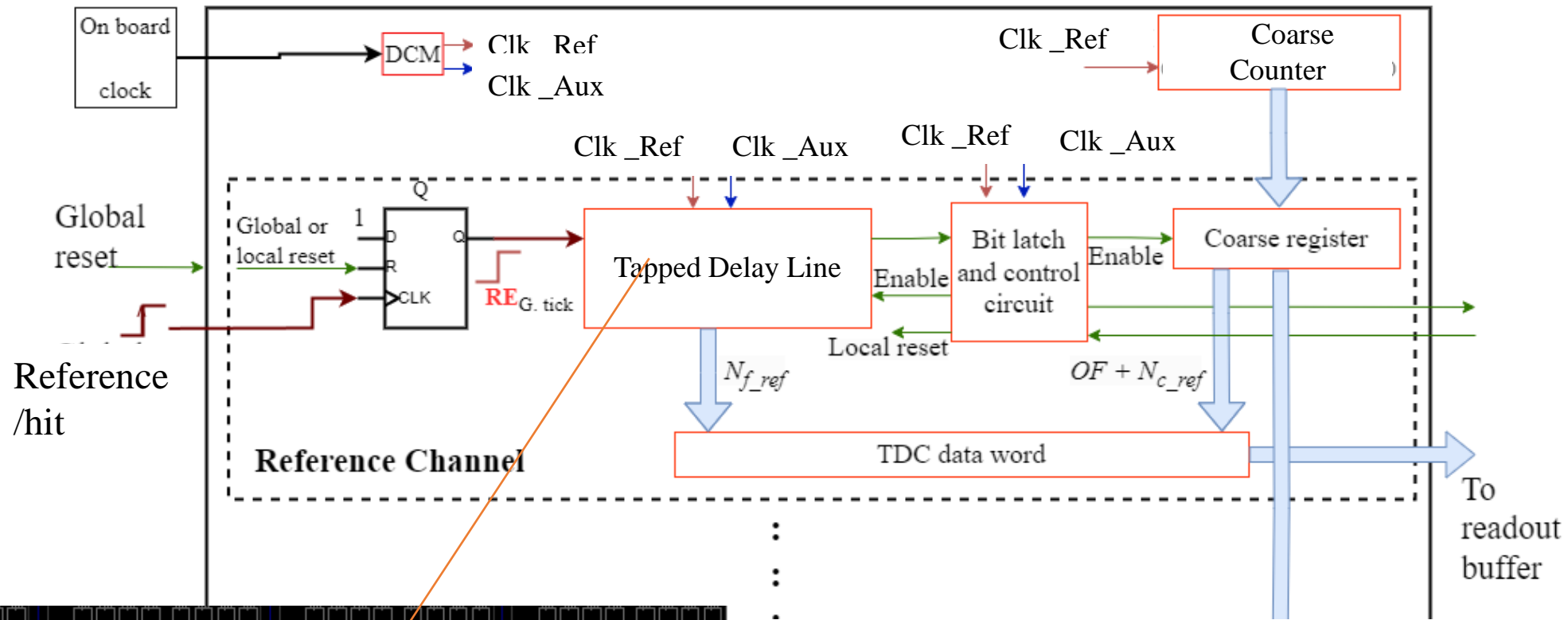
- Bring the processor, TDC and DAQ logic in the same FPGA



LabView Based Data Analysis



# Artix-7 FPGA TDC: High resolution (~62 ps(LSB))TDC



## Challenges:

- Synchronization between delay line and coarse counter data
- Capturing delay line data considering free running counter.
- Estimation of bubble errors

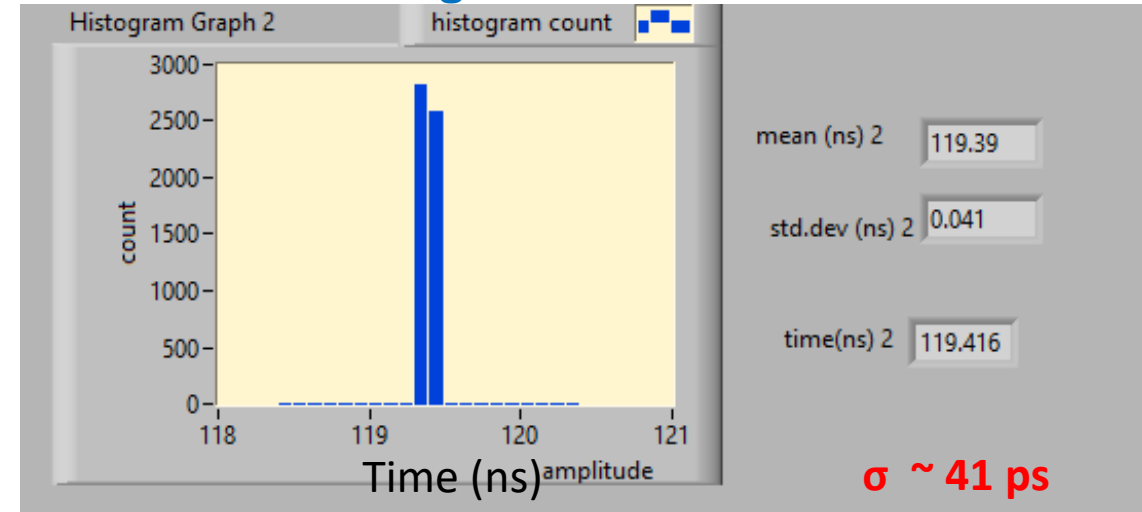
Carry chain structure in Artix-7 FPGA

# Artix-7 FPGA TDC: High resolution (~62 ps (LSB))TDC: Results

## Design Values:

- Reference clock frequency : 200 MHz
- Reference clock period ( $T_0$ ) : 5 ns
- No of delay cells firing to cover ( $T_0$ ) : ~ 80
- Resulting LSB across channels : ~ 62.5 ps

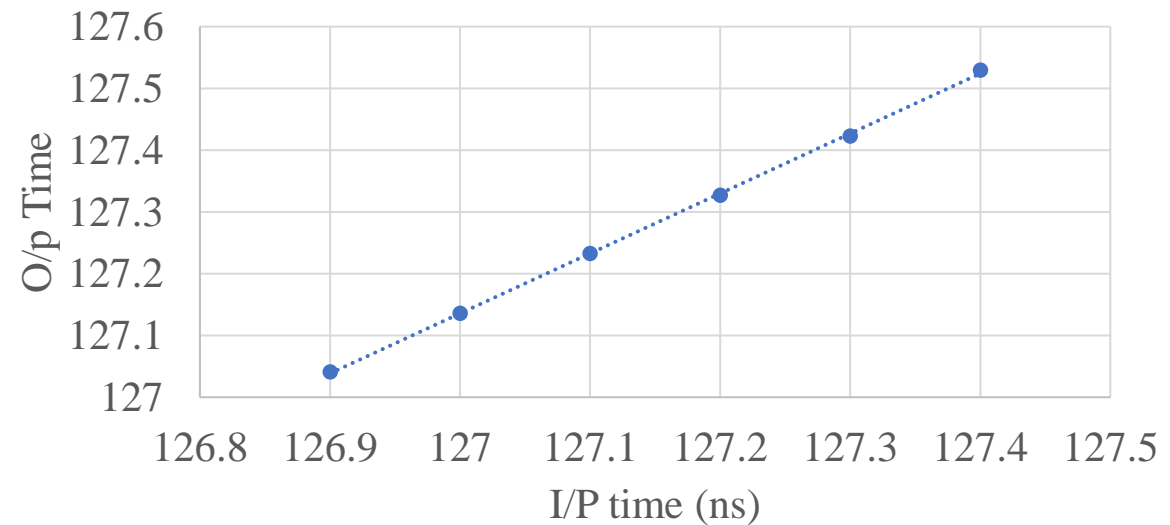
## Single Shot Precision



## Applied time vs measured time:

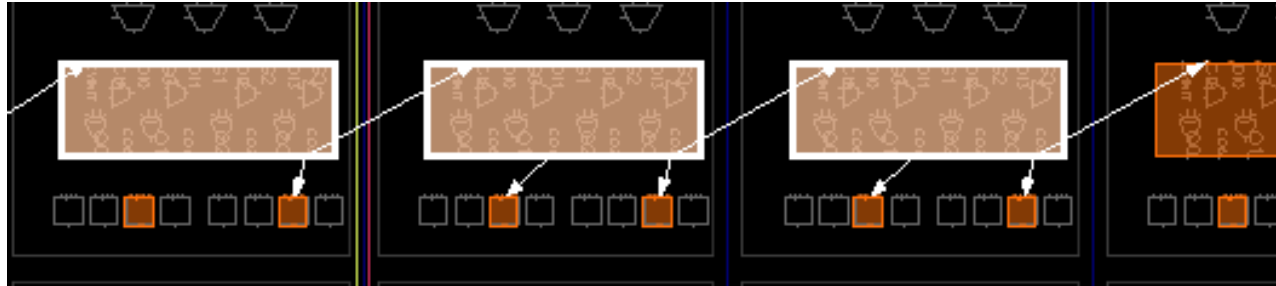
I/P time (ns)	O/P time (ns)
126.9	127.040
127	127.136
127.1	127.232
127.2	127.327
127.3	127.423
127.4	127.529

## Input time Vs Output time in ns



# Artix-7 FPGA TDC : Very High resolution (~32 ps (LSB))TDC

## Carry chain structure in Artix-7 FPGA



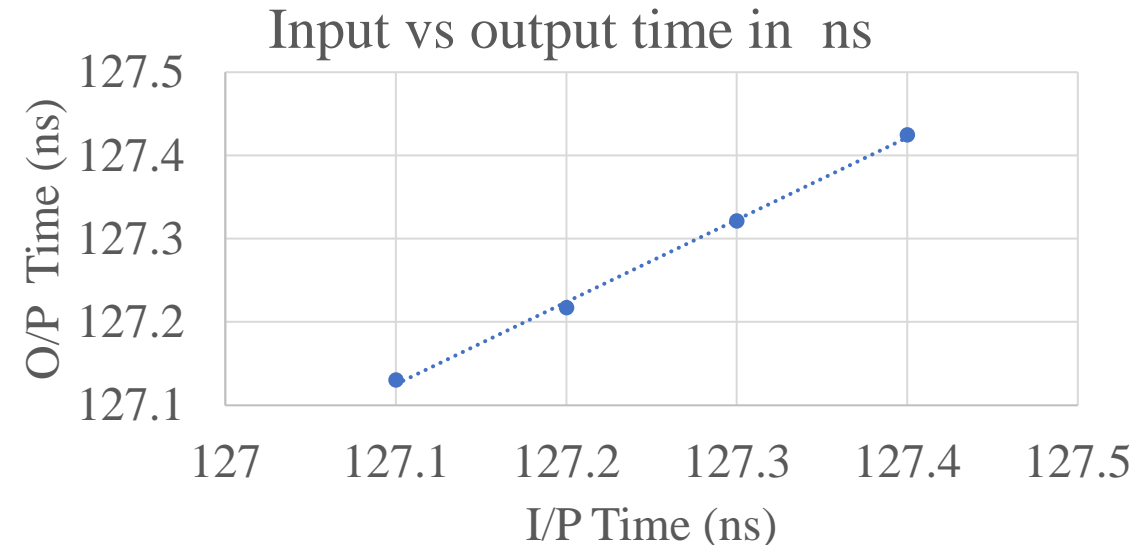
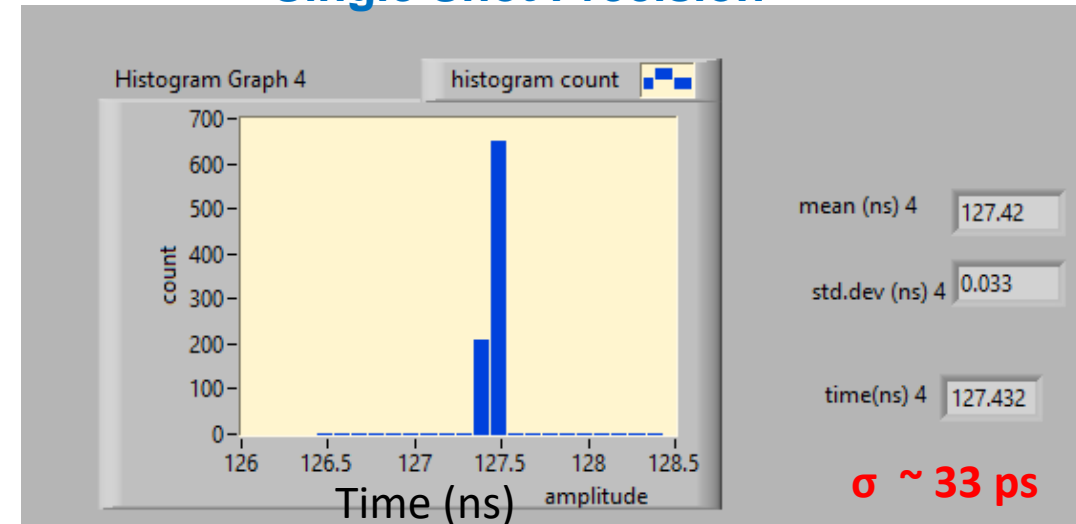
### Design Values:

- Reference clock frequency : 200 MHz
- Reference clock period ( $T_0$ ) : 5 ns
- No of delay cells firing to cover ( $T_0$ ) : ~ 158
- Resulting LSB across channels : ~ 31.6 ps

### Applied time vs measured time:

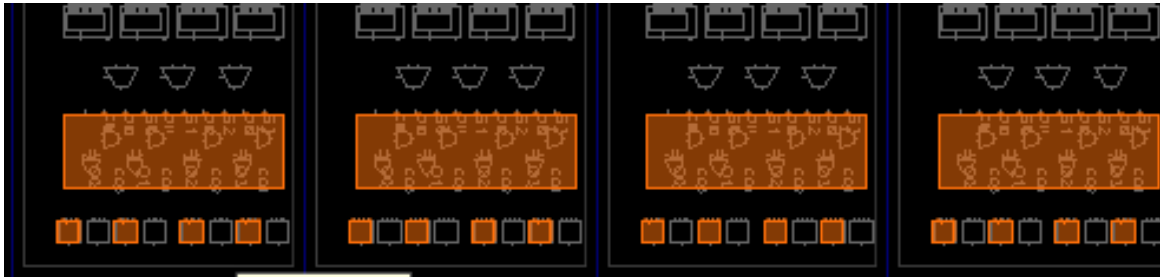
I/P time (ns)	O/P time (ns)	Std. Dev. (ps)
127.1	127.130	0.037
127.2	127.217	0.036
127.3	127.321	0.036
127.4	127.424	0.033

## Single Shot Precision



# Artix-7 FPGA TDC: Ultra high resolution: ~ 16 ps (LSB)

## Carry chain structure in Artix-7 FPGA



## Design Values:

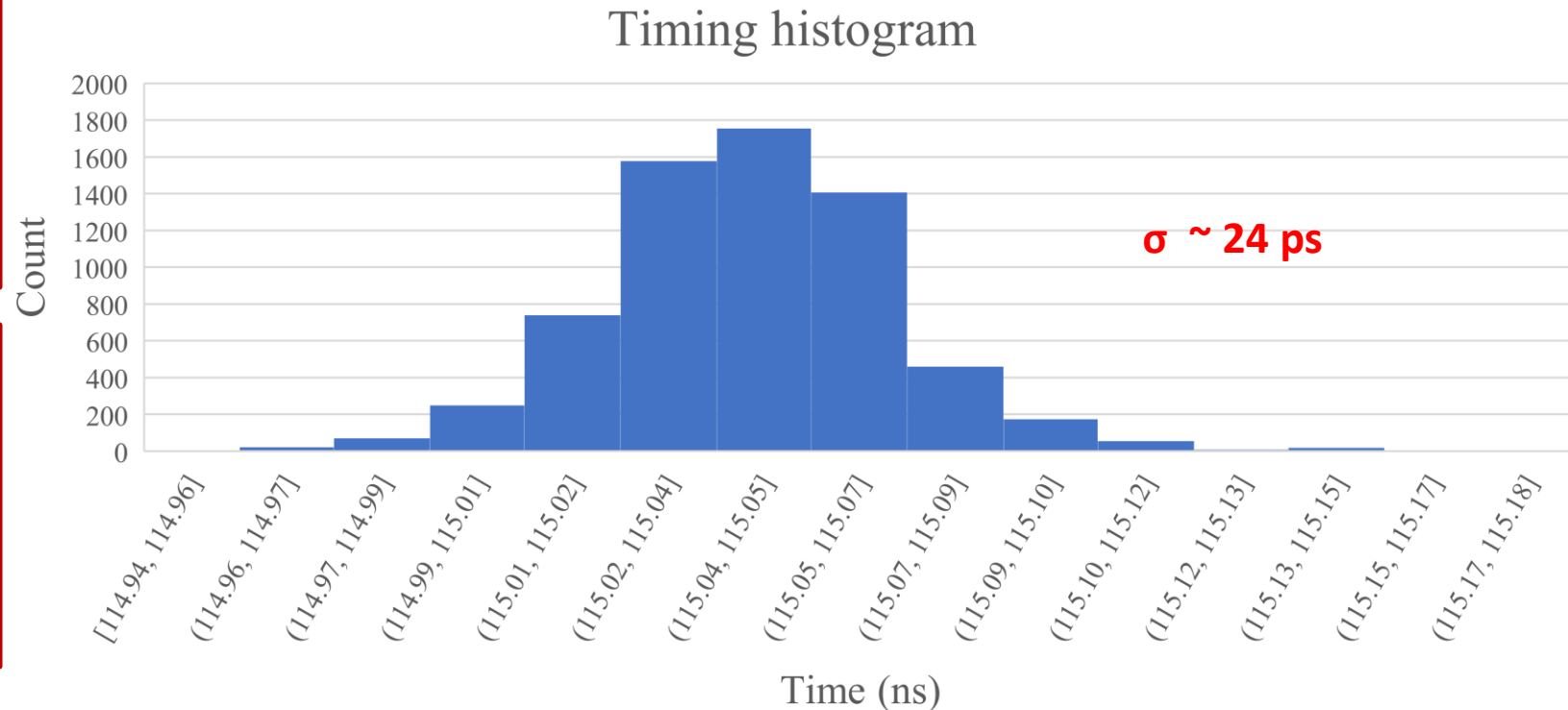
- Reference clock frequency : 160 MHz
- Reference clock period ( $T_0$ ) : 6.25 ns
- No of delay cells firing to cover ( $T_0$ ) : ~ 388
- Resulting LSB across channels : ~ 16.1 ps

## Challenges:

- Timing closure is difficult
- Synchronization between coarse and delay line data.
- Optimization of clock frequency and number of delay lines.

Time is calibrated using bin-to-bin calibration method using weighted average of each timing bin.

Ref: J. Y. Won et.al. IEEE Transactions on Instrumentation and Measurement, vol. 65, no. 7, pp. 1678–1689, 2016

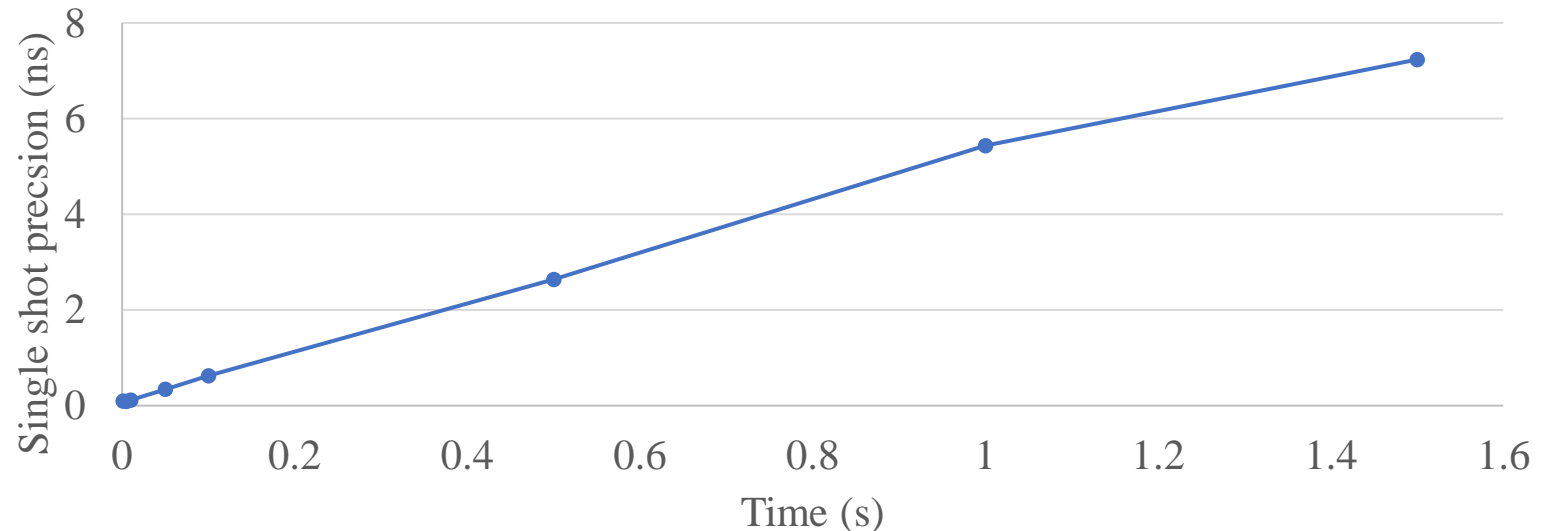


# Artix-7 FPGA : Long range TDC tested up to 1.5 s

- By increasing the coarse counter bits (to 32 bits), and keeping the same LSB (33 ps), the TDC was designed for large dynamic range
- For list mode continuous time tagging applications
- SSP( $\sigma$ ) less than 100 ps till 5 mS range.

Time (s)	Shot precision (ns)
0.001	0.088
0.005	0.086
0.01	0.111
0.05	0.33
0.1	0.622
0.5	2.635
1	5.433
1.5	7.235

Input time (s) Vs single shot precision (ns)



# Summary and Conclusion

During the development of high resolution TDCs following features required for many experiments are addressed

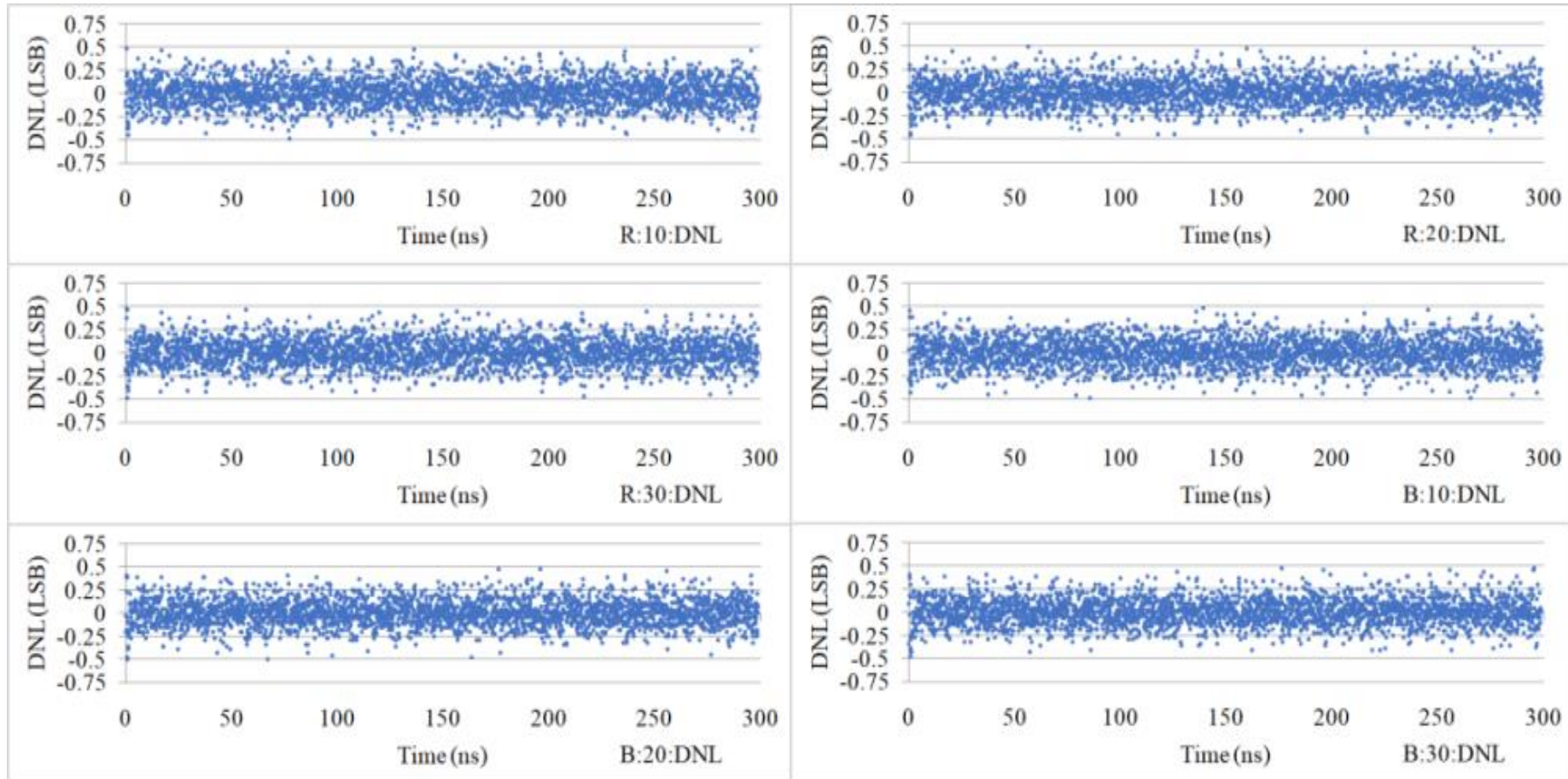
Parameter	Ticked
7-Series FPGA	✓
Integration with existing DAQ logic	✓
TDC resolution (LSB) (62 ps/31 ps /16 ps)	✓
Range (up to 1.5 second)	✓
Modes (Trigger matching)	✓
Multi-hits	✓
Multi-channel (up to 128)	✓
SoC Enabled	✓
Average bin width or cell-to-cell In system calibration	✓

**Thank You**

# Spartan-6 FPGA TDC: Detailed Test Results

## Linearity

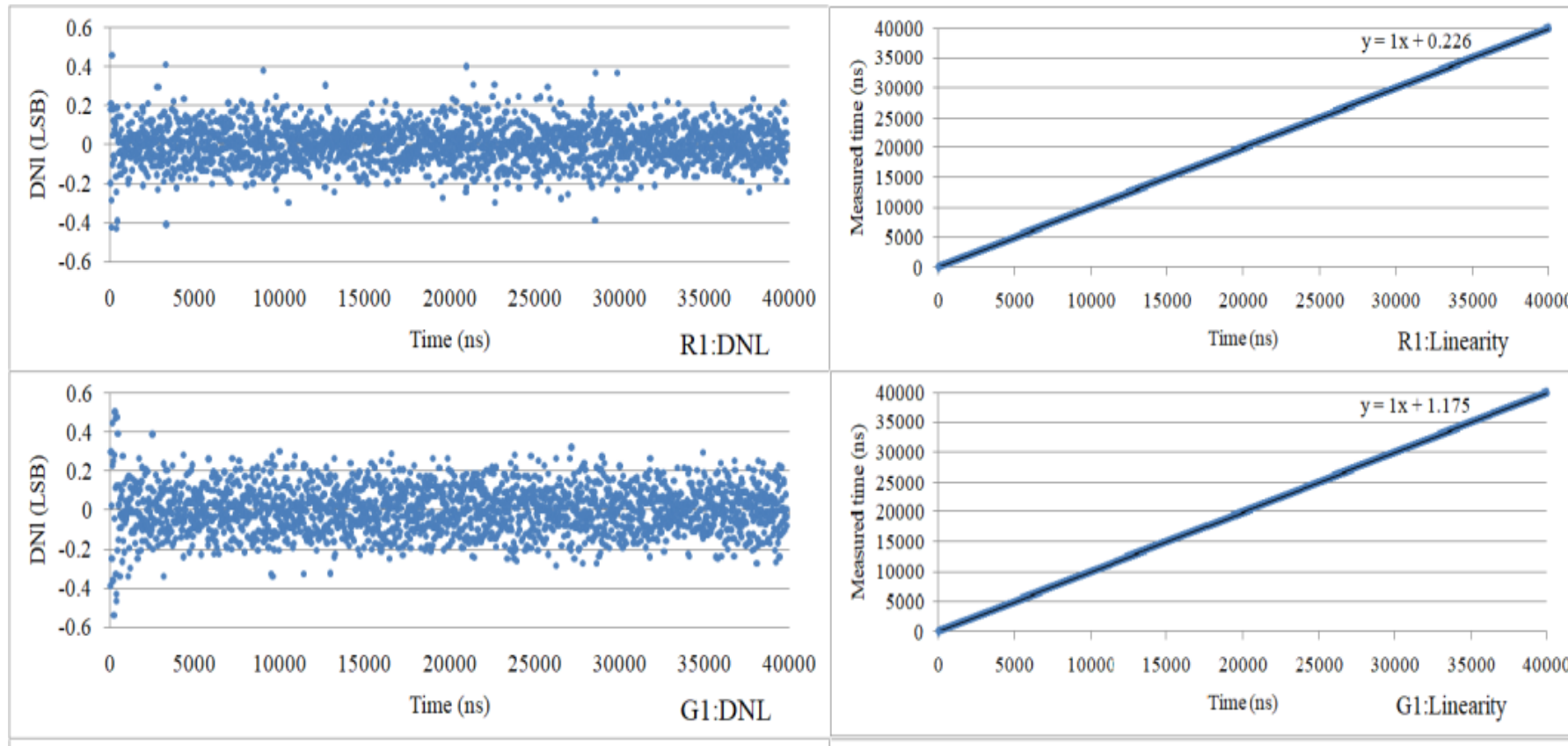
- Time inputs are swept insteps of LSB up to 300 ns
- DNL within  $\pm 0.5$  LSB
- A channel per decade in R & B groups is shown



# Spartan-6 FPGA TDC: Detailed Test Results

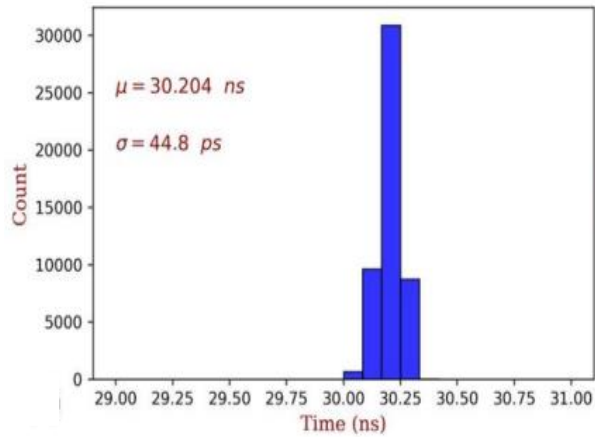
## Linearity

- Time inputs are swept insteps of 20 ns up to 40  $\mu$ s (DR)
- DNL of CH-1of R-,G-, B-, and Y-groups :  $\pm 0.45$ ,  $\pm 0.45$ ,  $\pm 0.35$ ,  $\pm 0.5$  LSB
- INL of CH-1: [-0.49, 0.84],[ -0.65, 0.70], [-0.59, 0.59], [-0.50, 0.83] LSB
- First channel of R & G groups is shown

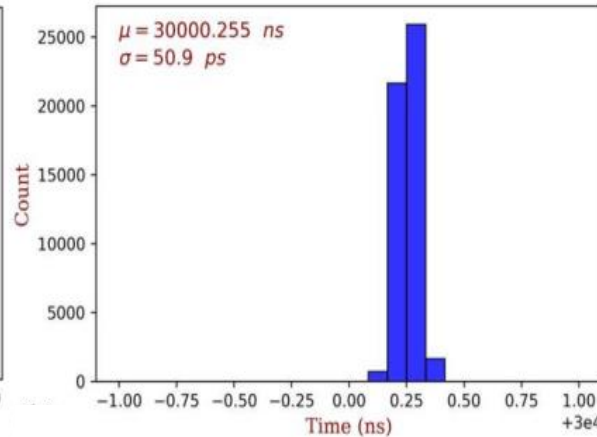


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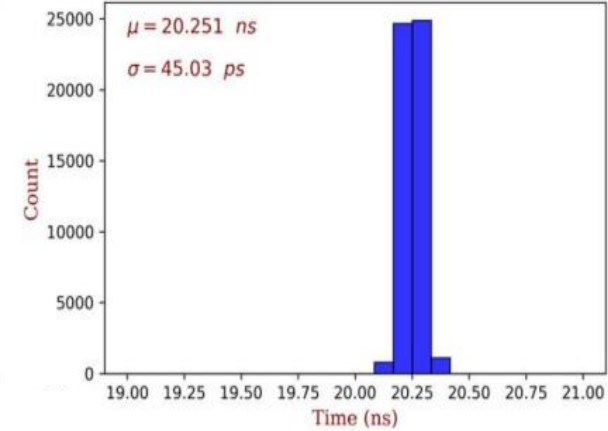
## Precisions: Time spectrums



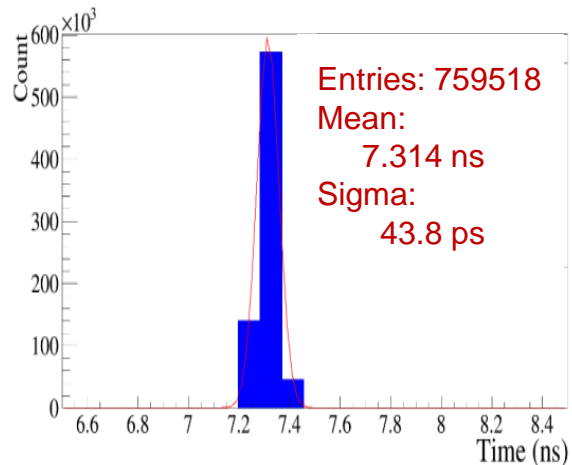
CH-1, R-Group @ 30 ns time input



CH-1, R-Group @ 30  $\mu$ s time input

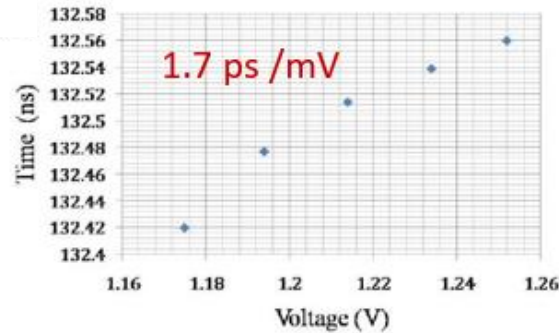


Pulse width measurement

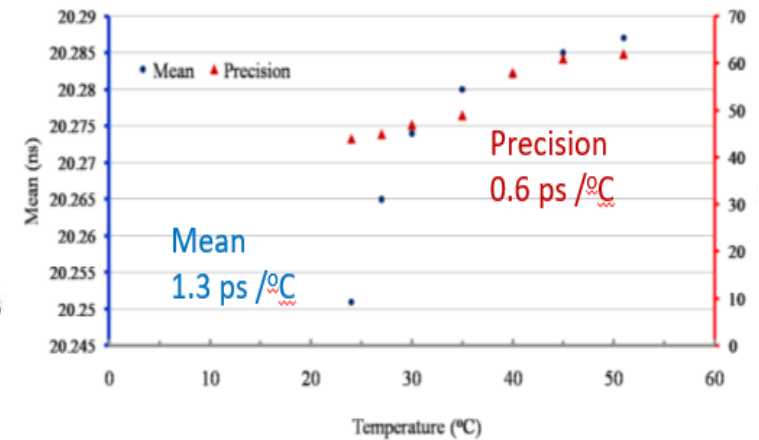


The long term (continuous operation of more than 8 Hrs) time spectrum of the TDC channel-1 of the Y group

## Variation with voltage and Temperature

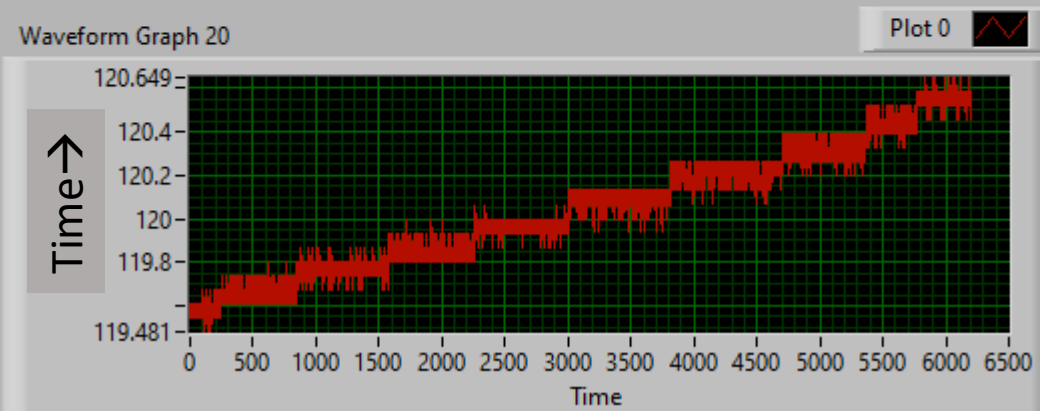
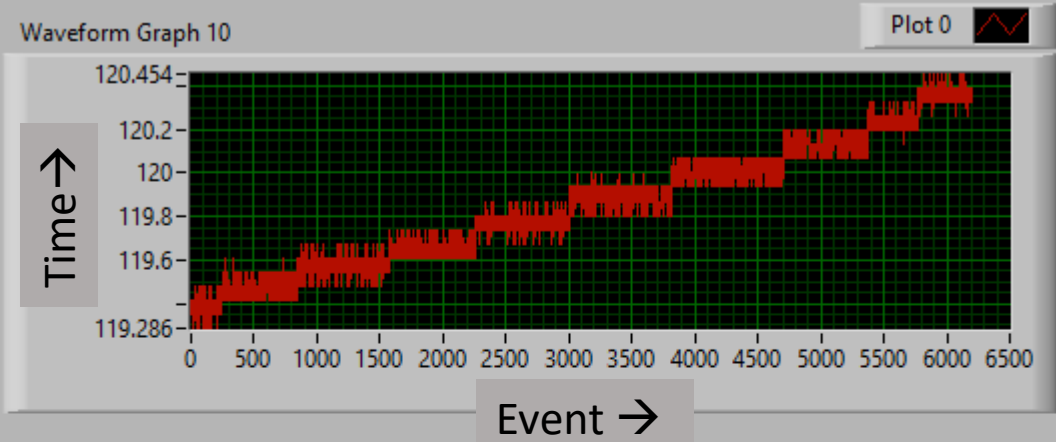


Measured Time with voltage

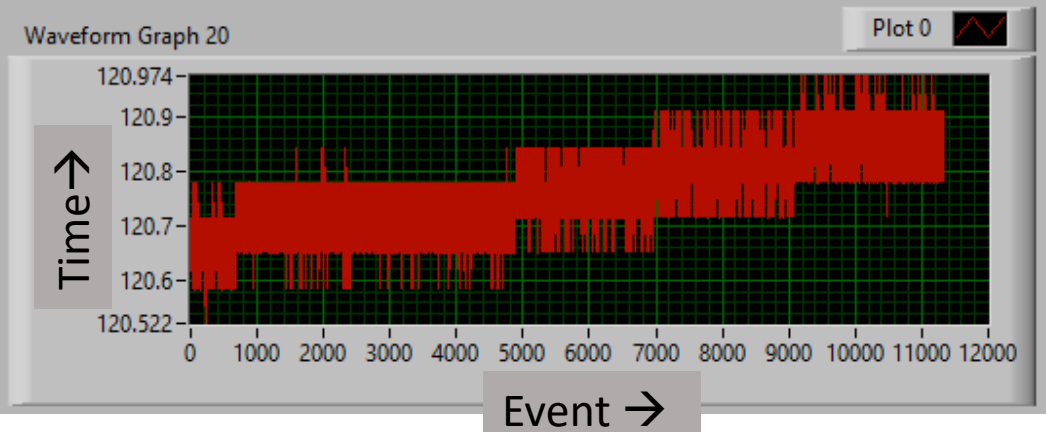
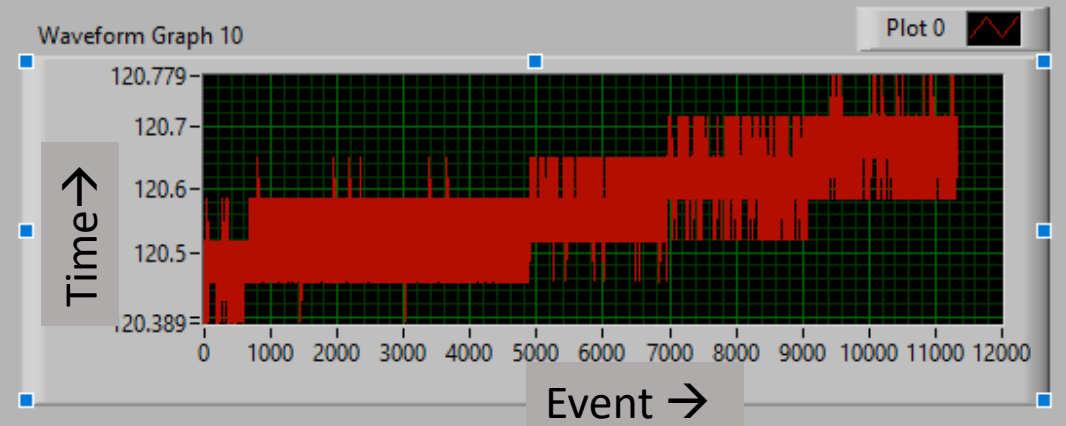


Measured Time and Precision with Temperature

# Artix-7 FPGA TDC: Characterization



*Input time swept insteps of 100 ps*



*Input time swept in steps of 50 ps*

*with LSB 62 ps*