

OCTOPUS

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The OCTOPUS Project: Development of a Monolithic Active Pixel Sensor for Future Lepton Colliders

The OCTOPUS (Optimized CMOS Technology for Precision in Ultra-thin Silicon) project, established within the DRD3 collaboration, aims to develop a Monolithic Active Pixel Sensor (MAPS) demonstrator to meet the stringent requirements of future lepton collider vertex detectors. This paper presents the architecture, design features, and preliminary simulation results of the first OCTOPUS prototype, named WOLFI, which is being developed as a demonstrator for future beam-telescope sensors.

The project follows a staged approach, allowing for adaptations of the final development targets depending on the future choice of the Lepton-Collider technology. The ultimate goal is to realize a full-sized vertex sensor demonstrator with a spatial resolution of $\leq 3 \mu\text{m}$, a time resolution of $O(5\text{ns})$, and a high hit rate tolerance of $O(100 \text{ MHz}/\text{cm}^2)$. The chip is being designed to be radiation-hard ($O(10^{14} \text{ n}_{\text{eq}}/\text{cm}^2)$) and to have a low power consumption ($< 50 \text{ mW}/\text{cm}^2$). The first test chip WOLFI aims for a time resolution of $O(100 \text{ ns})$, with a power consumption of $< 500 \text{ mW}/\text{cm}^2$. The demonstrator is being implemented in a TPSCo 65nm CMOS Imaging Technology, which allows for increased logic density and more in-pixel functionality, compared to larger-feature-size processes.

The OCTOPUS design benefits from the extensive experience gained with TPSCo 65 nm technology demonstrators produced and tested in various projects and collaborative frameworks (EP R&D, ALICE ITS3, Tangerine and others). This foundational work, along with ongoing TCAD and Allpix Squared simulations, informs the development of the WOLFI chip. A key feature of the design is a data-driven asynchronous readout architecture that utilizes an Asynchronous Priority Arbiter (APA) for efficient, conflict-free data handling. This approach is intended to reduce latency and provide finer control over data acquisition compared to traditional synchronous methods. The front-end circuit includes time-over-threshold (ToT) measurements for improved time walk compensation.

This contribution will introduce the project's objectives and development strategy. The latest simulation results will be discussed, showing the optimization of sensor layouts to balance efficiency, timing, and spatial resolution. The preliminary design work on the WOLFI prototype, its functionality, and the path towards a final vertex sensor demonstrator will be highlighted.