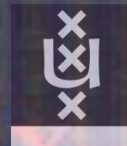


The RD50-MPW4: a radiation hard HV CMOS sensor for future colliders

Jory Sonneveld on behalf of the (former) CERN RD50 CMOS working group

jory.sonneveld@nikhef.nl

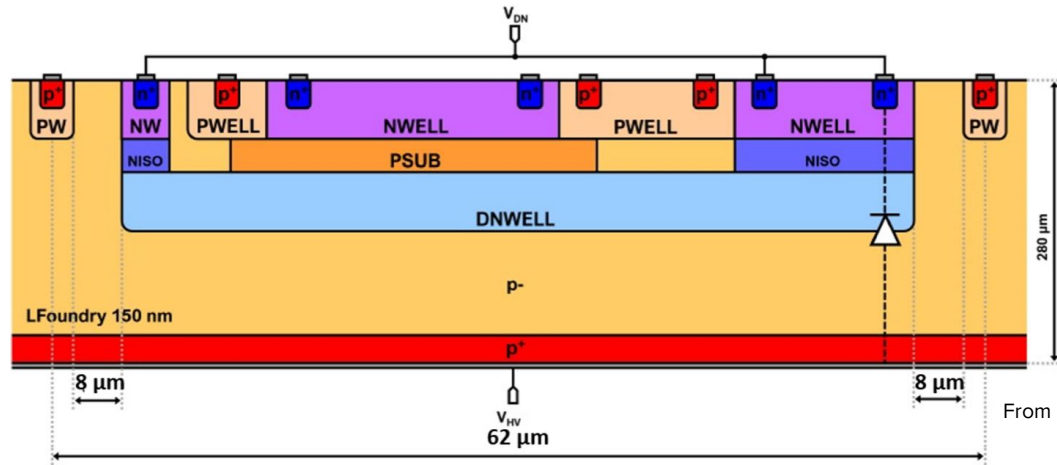


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RD50 HV CMOS: Large collection electrode

- Large charge collection electrode (deep n-well or DNWELL in p-substrate)
- In-pixel readout electronics embedded inside DNWELL
- Deep p-well (PSUB) for shielding → CMOS electronics can be used in pixel
- Can bias substrate with high voltage to improve NIEL radiation tolerance
- High voltage applied from the top side or back side after back side processing

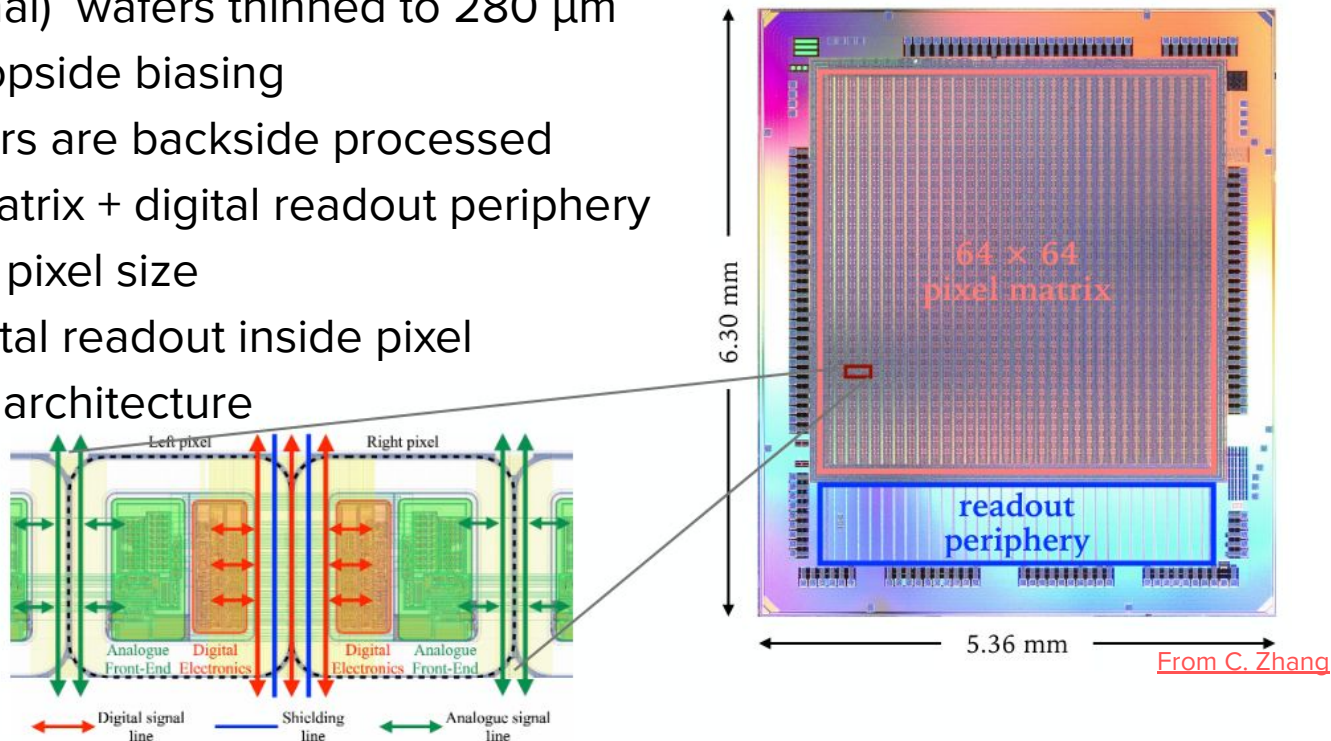
postprocessing →



From [E. Vilella et al 2025 JINST 20 C03044](#)

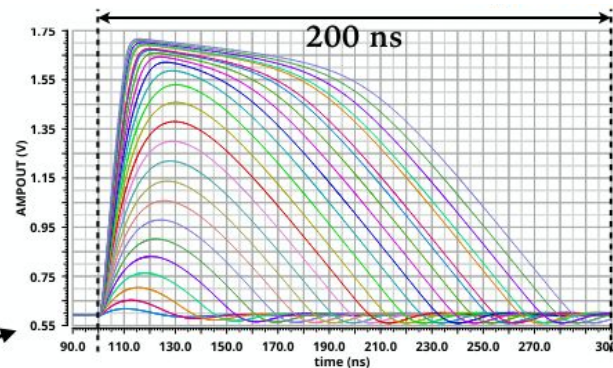
RD50-MPW4

- 3 k Ω ·cm (nominal) wafers thinned to 280 μ m
- 3 wafers with topside biasing
- 2 of these wafers are backside processed
- 64 \times 64 pixel matrix + digital readout periphery
- 62 μ m \times 62 μ m pixel size
- analog and digital readout inside pixel
- double-column architecture

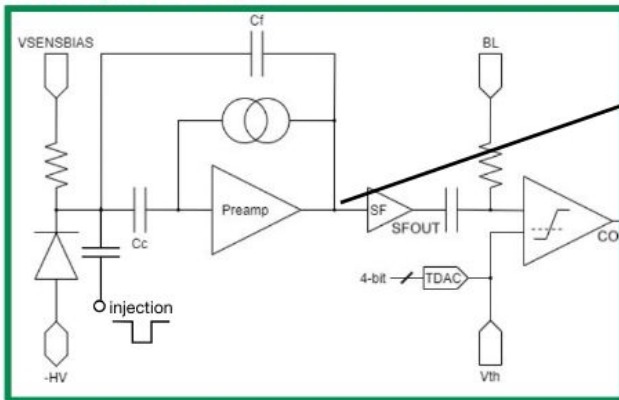


RD50-MPW4 in pixel electronics

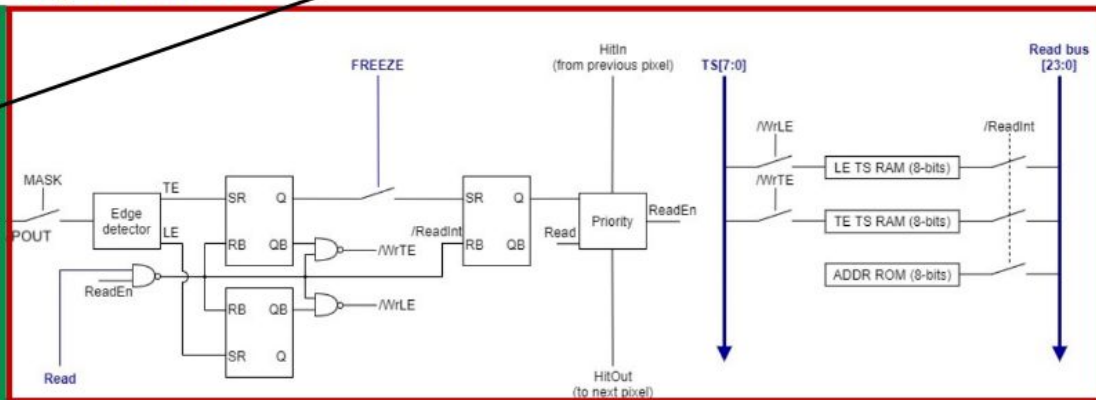
- Charge Sensitive Amplifier with injection circuit
- Comparator with 4-bit trimDAC
- Processing time (\sim ToT) for a 25 ke- signal $<$ 200 ns
- Triggerless column drain readout architecture
- 8 bit pixel address for row (pixel) and column (EoC)
- 8 bit leading and trailing edges give ToT



Analogue readout



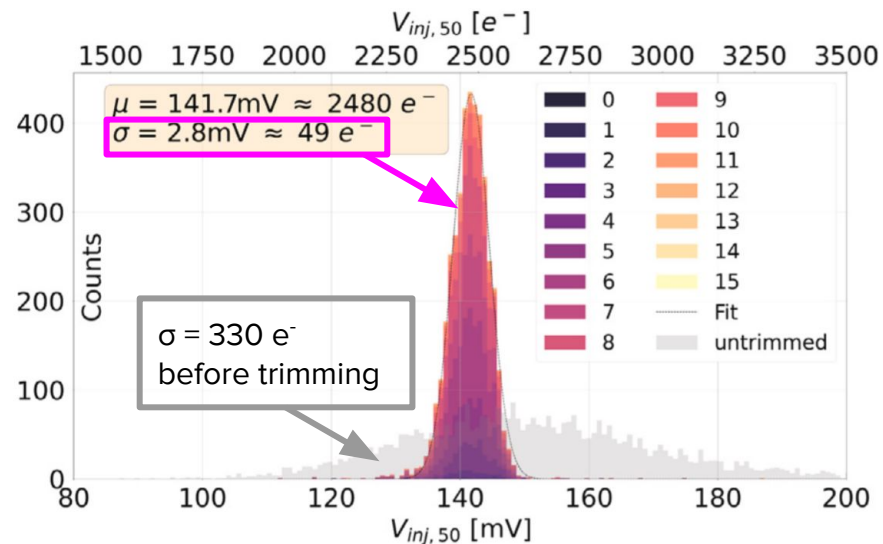
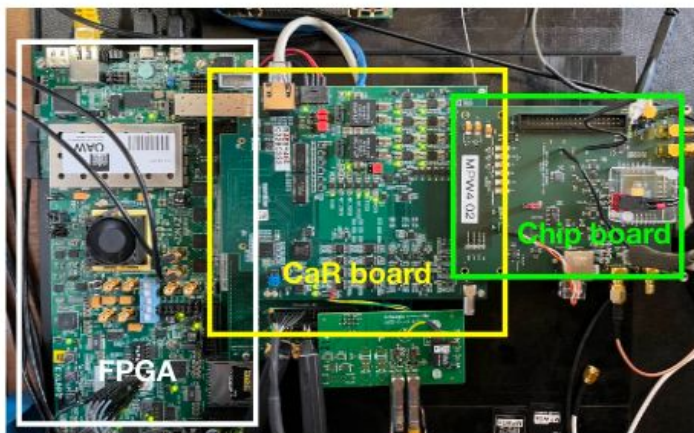
Digital readout



RD50-MPW4 readout and data acquisition

- I2C protocol for slow control configuration
- 32 End of Column (EoC) that serialize data
- Data is sent out through a 640 Mbit/s LVDS link
- DAQ based on Caribou

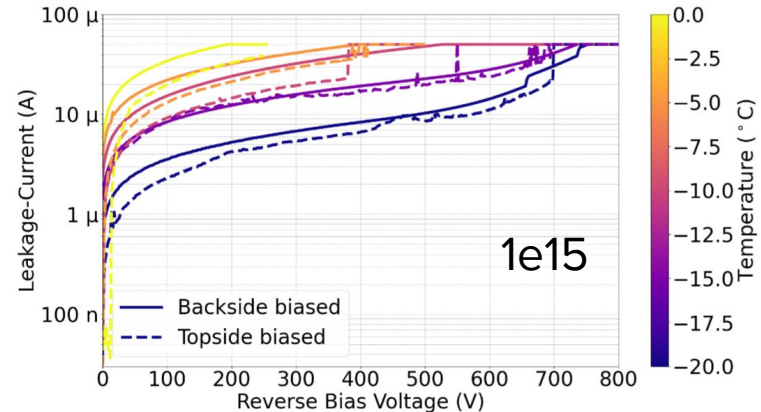
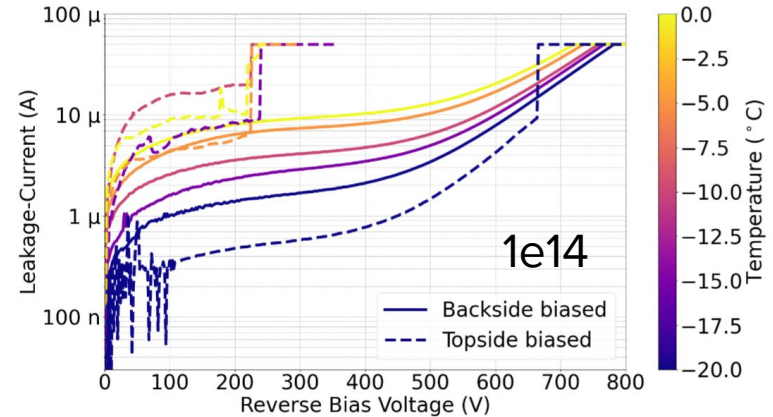
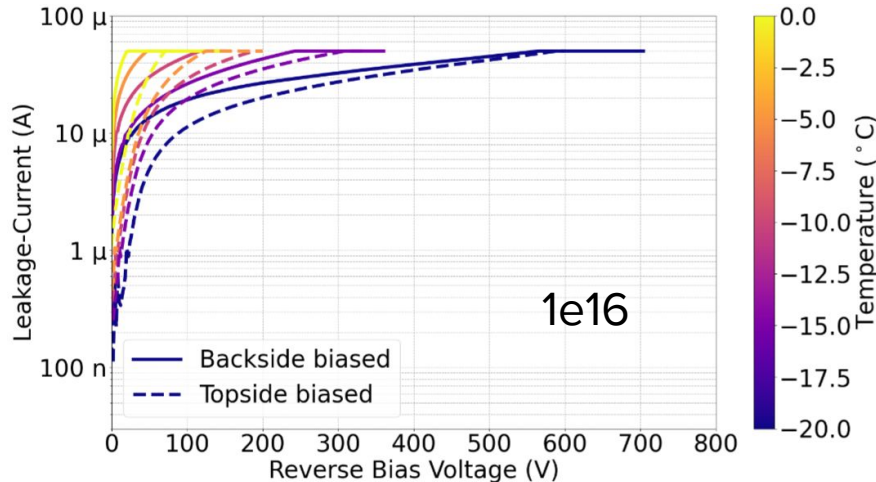
[Y. Otariid et al 2025 JINST 20 C07043](#)



RD50-MPW4 leakage current after irradiation



- Unirradiated samples: Leakage current $O(10 \text{ nA})$ at $V_{\text{depletion}} = -190 \text{ V}$
- Can bias sensors beyond 600 V
- Increased leakage current for increased temperatures as expected

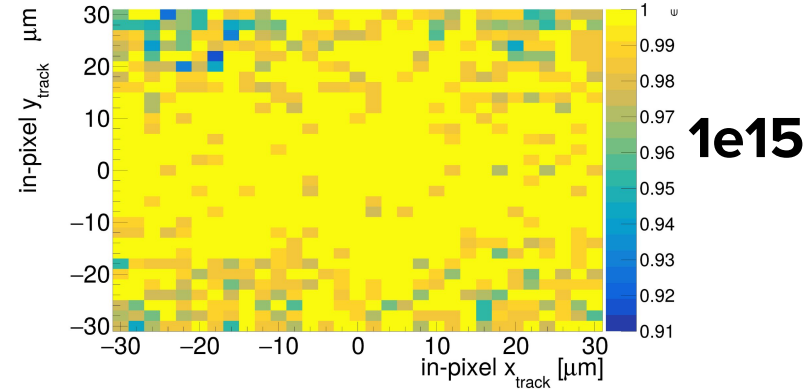


Efficiency of irradiated RD50-MPW4

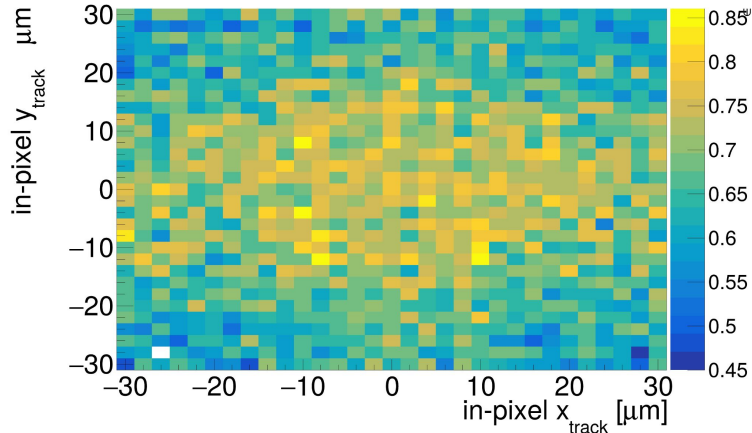


- Test beam at DESY with 4.2 GeV electrons
- 10 sensors were tested
- Sensors were annealed at 60 °C for 80 min.
- Efficiency degrades with higher fluences as expected, especially in pixel corners

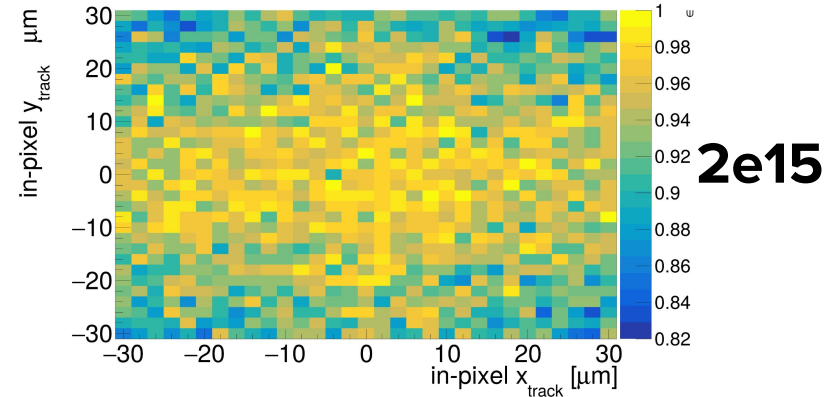
In-pixel efficiency
RD50_MPWx_0 Pixel efficiency map



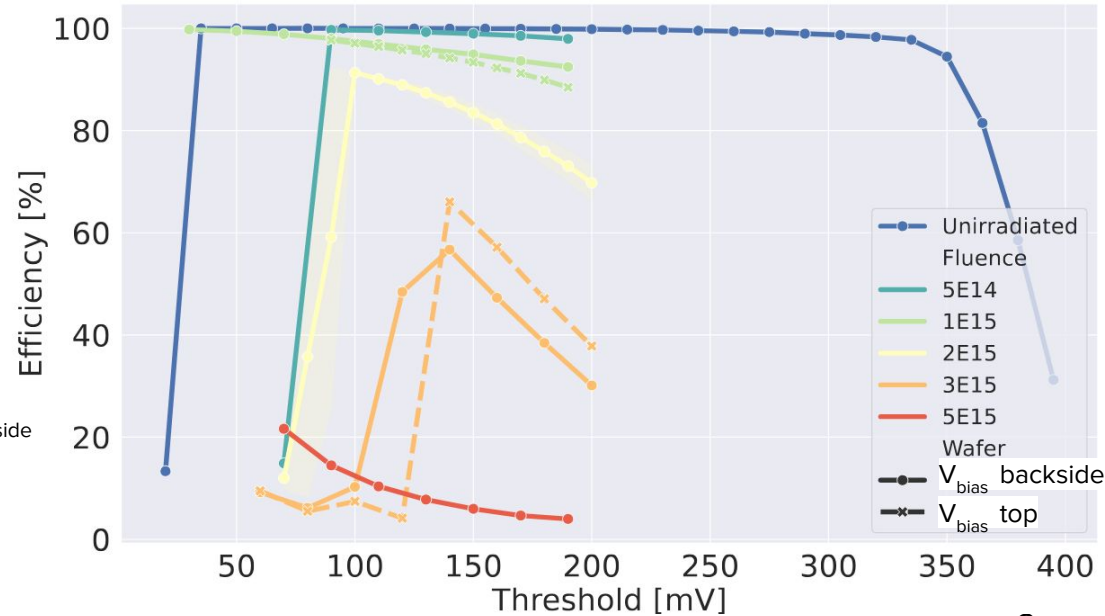
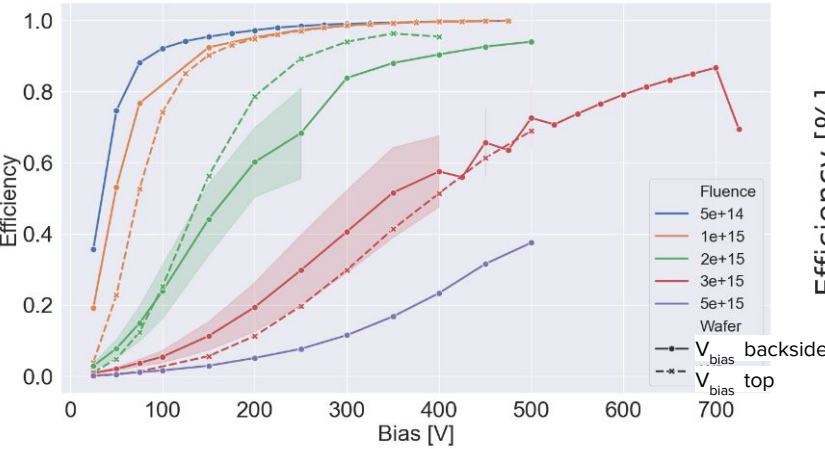
RD50_MPWx_0 Pixel efficiency map



RD50_MPWx_0 Pixel efficiency map



RD50-MPW4 efficiency vs bias and threshold

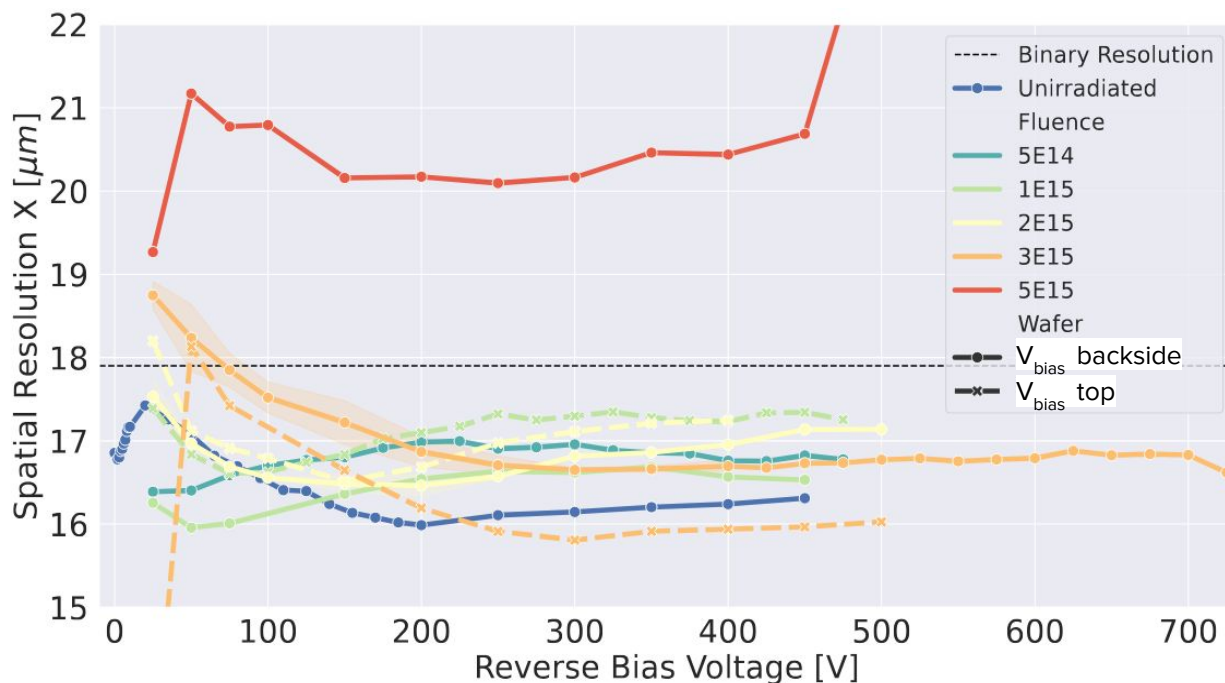


- An **efficiency > 99%** was reached for fluences **between 1e15 and 2e15** n_{eq}/cm^2
- Backside biased sensors perform mostly better than topside biased sensors

Fake hit rate: acceptable up to $\Phi_{eq} = 3 \cdot 10^{15} n_{eq}/cm^2$ and noisy from $\Phi_{eq} = 5 \cdot 10^{15} n_{eq}/cm^2$

RD50-MPW4 spatial resolution

- All samples beside the one irradiated to $5E15 \text{ n}_{\text{eq}}/\text{cm}^2$ have a better than binary spatial resolution
- No clear correlation between fluence and resolution



Using geometric mean of biased and unbiased resolution

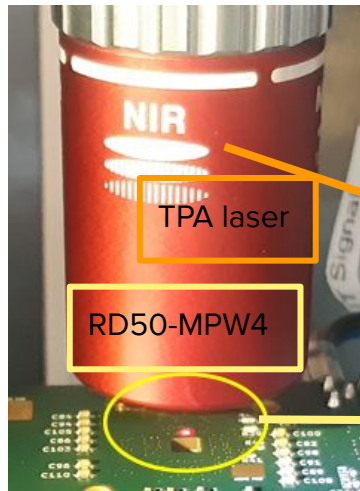
Characterization with two-photon absorption laser

TPA lasers can be used for 3D imaging of semiconductors

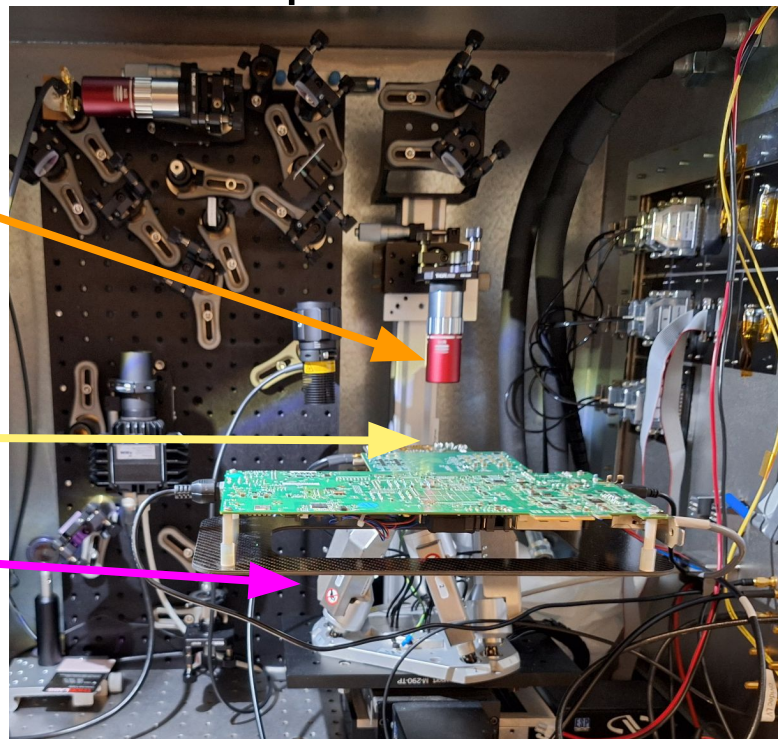
They are available only in a limited number of HEP institutes: CERN (CH), JSI Ljubljana(SI), IFCA (ES), NIKHEF(NL), Lancaster (UK), Oxford (UK), Manchester (UK)...

At the CERN Solid State Detector lab:

- Backside illumination
- 1550 nm 400 fs pulse laser
- Non-backside processed sensor
- Hexapod stage for XY and Z
- Injection 0.25 nJ / pulse
- Shot rate 1 kHz



Hexapod stage



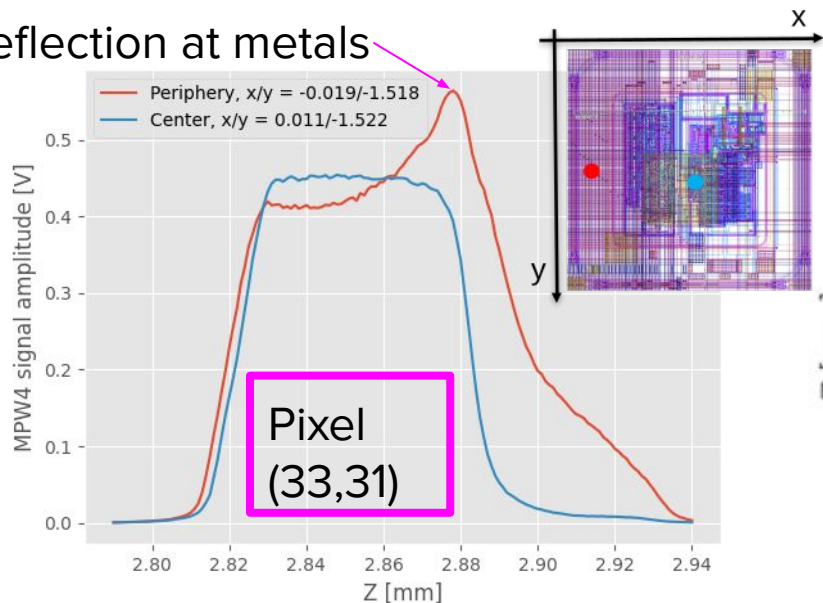
Sensor and front-end settings:

- Threshold 940 mV
- $V_{\text{bias}} = -90 \text{ V}$

Depletion depth of RD50-MPW4



Reflection at metals



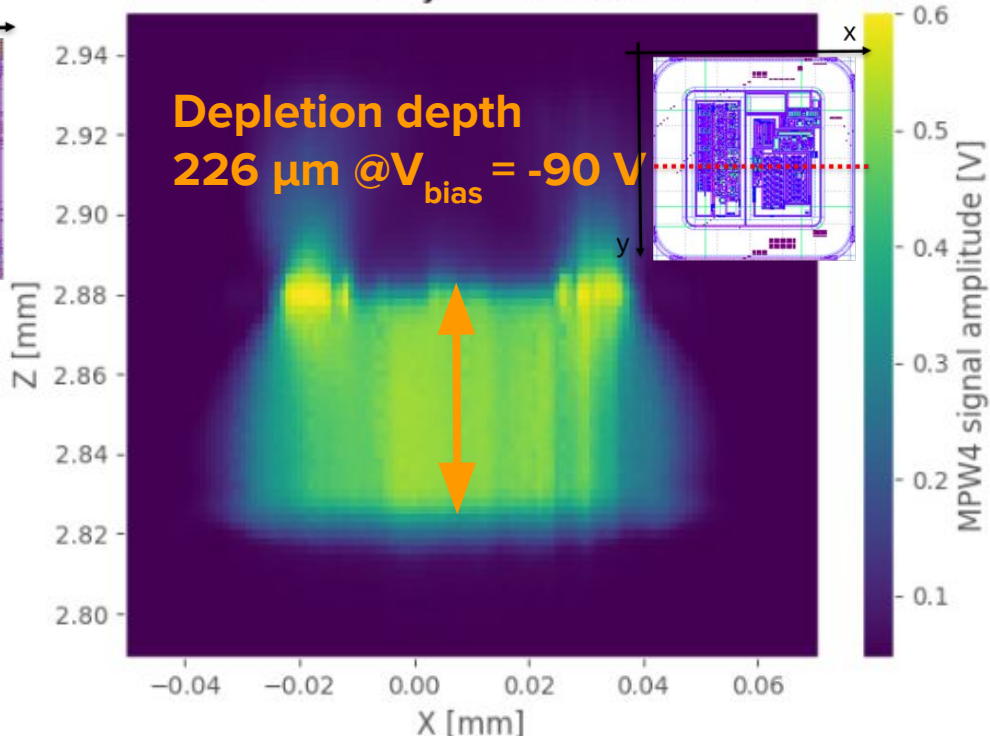
$$z_{Si} = z_{stage} \cdot \sqrt{\frac{z_R \pi n_{Si}^3}{z_R \pi n - \lambda n^2 + \lambda}}$$

[Wiehe et al IEEE Trans. Nucl. Sci. 68 \(2021\) 2](#)

$$w_0 = 1.5 \mu\text{m} \quad z_R = \frac{\pi w_0^2 n_{Si}}{\lambda}$$

z-scale corrected for refraction $n_{Si} = 3.77$

xz-scan, $y = -1.522\text{mm}$ (Hexapod stage)

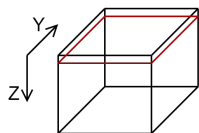
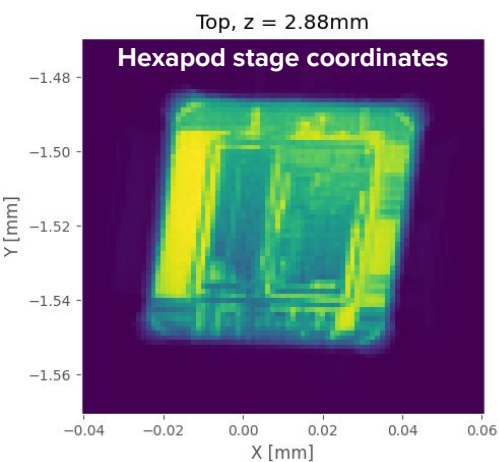
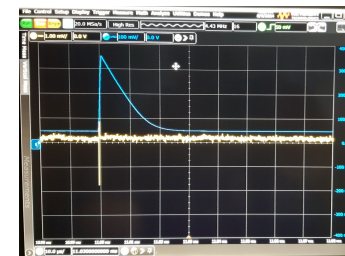


X is scanned from 0 to 62 μm Y=85 μm
Z is scanned from 0 to 264 μm

Signal amplitude at different pixel depths

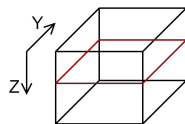
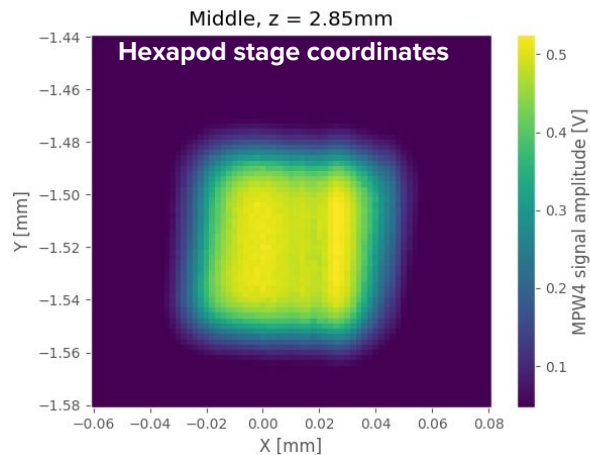
XY scan of 280 μm thick sensor:

- Metal affects signal response. Electronics visible at the top.
- Edge of depletion region reached at $-245 \mu\text{m}$.



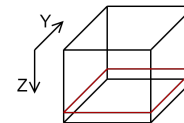
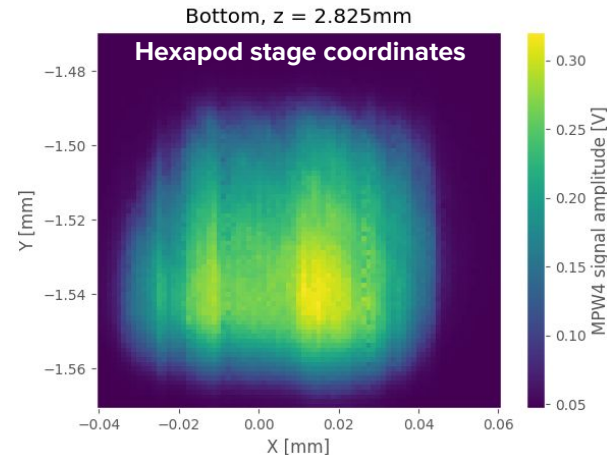
Top of sensor,
 $0 \pm 3 \mu\text{m}$

Jory Sonneveld



Middle of sensor,
 $-113 \pm 3 \mu\text{m}$

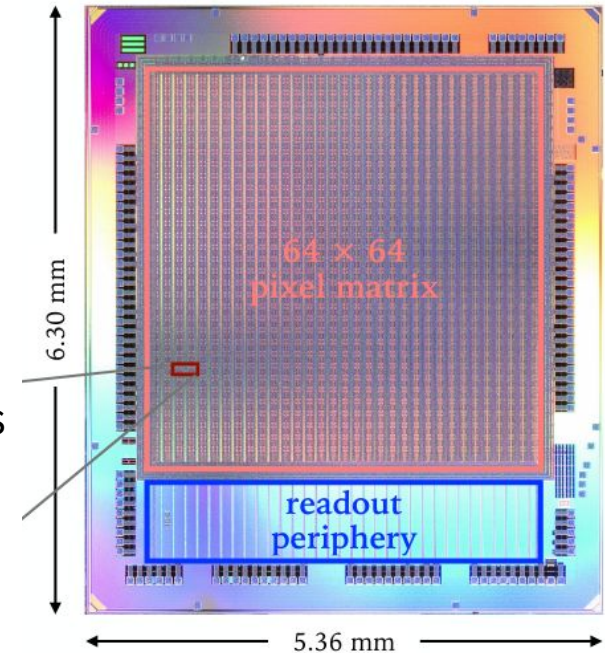
TIPP 2026 – RD50-MPW4 HV CMOS 2026-02-05



Backside of sensor,
 $-245 \pm 3 \mu\text{m}$

Summary and outlook

- The RD50-MPW are a series of monolithic High Voltage CMOS pixel sensors
- With breakdown voltages over 600 V the RD50-MPW4 can be fully depleted
- The RD50-MPW4 has high radiation tolerance with high bias voltage and backside biasing
- The RD50-MPW4 has > 99% efficiency for fluences up to $2 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$
- A 3D image of the sensor was obtained using a TPA laser
- R&D with LFoundry 150 nm continues within DRD3 with RadPix sensor towards LHCb Mighty Tracker



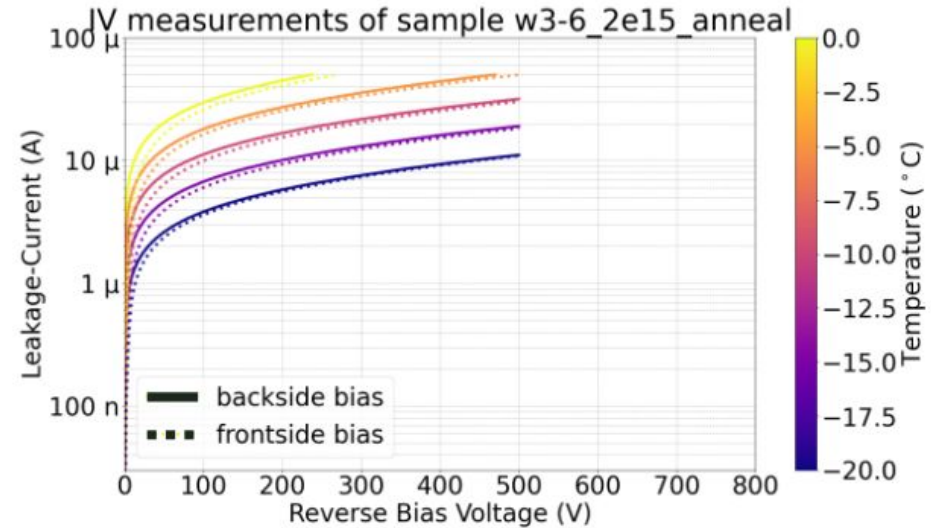
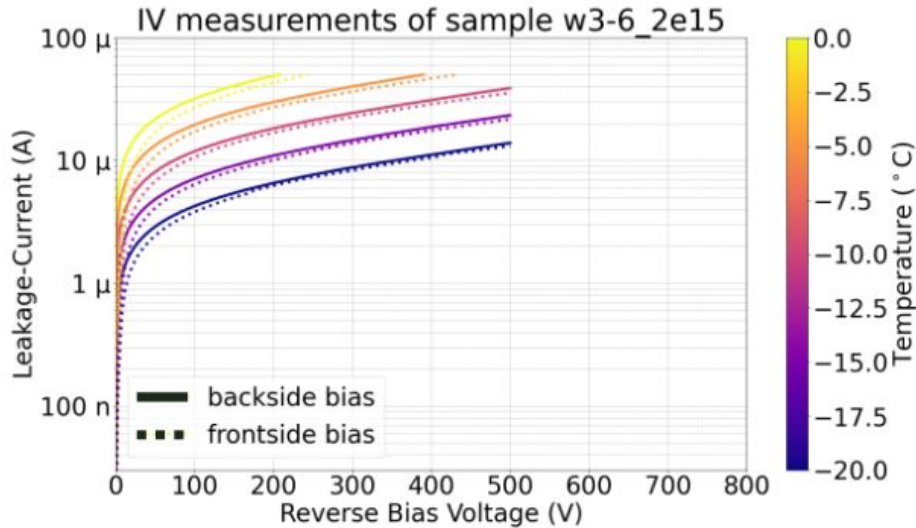
Additional material

RD50 MPW4 behavior after irradiation



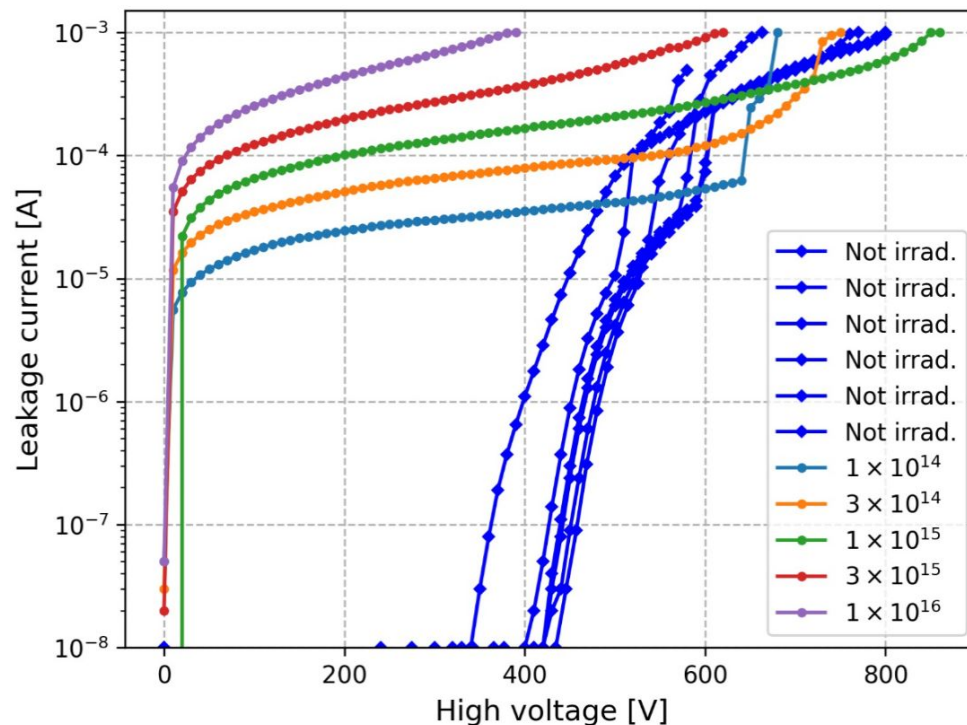
[From Bernhard Pils!](#)

IV curves



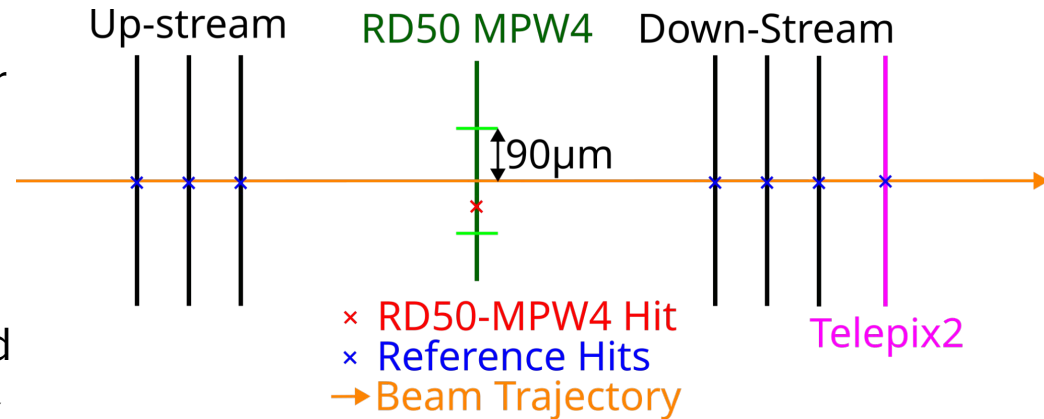
RD50-MPW4 leakage current after irradiation

- Unirradiated samples:
Leakage current $O(10 \text{ nA})$
at $V_{\text{depletion}} = -190 \text{ V}$
- Sudden leakage increase
between 350 V and 450 V
- Irradiated samples can be
biased beyond 600 V



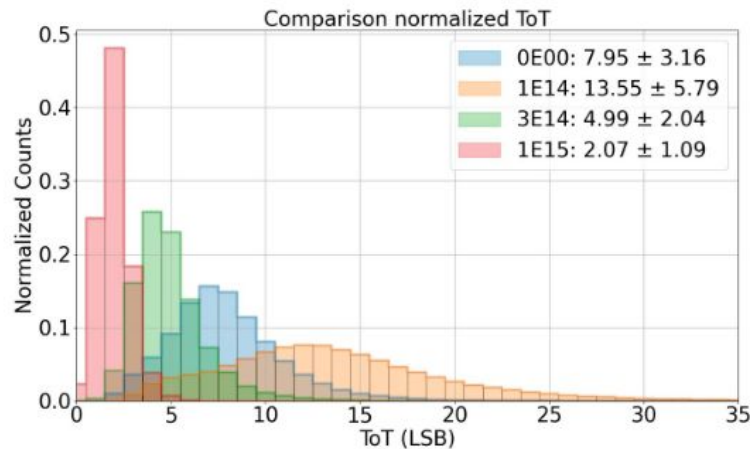
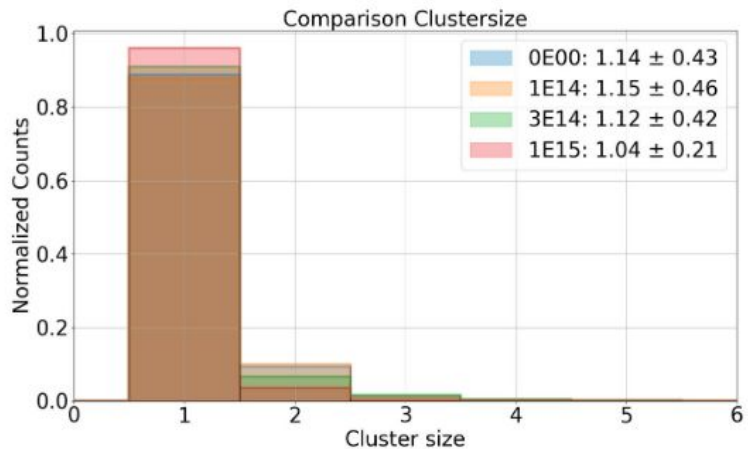
DESY Testbeam

- Adenium telescope with 6 ALPIDE planes
- AIDA-TLU for synchronization
- Peltier based cooling setup down to $\sim 0^{\circ}\text{C}$
- Telepix2 as ROI and timing layer
- Data acquisition EUDAQ2
- Analysis using Corryvreckan
- Allow distance between reconstructed track position and detected cluster at DUT of $\sim 1.5x$ pitch



RD50-MPW4 ToT and cluster size

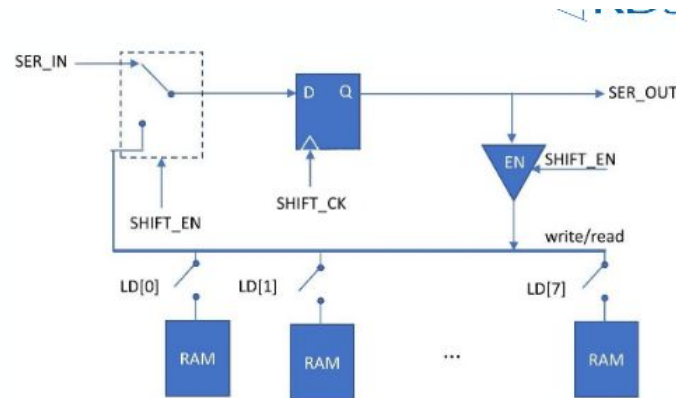
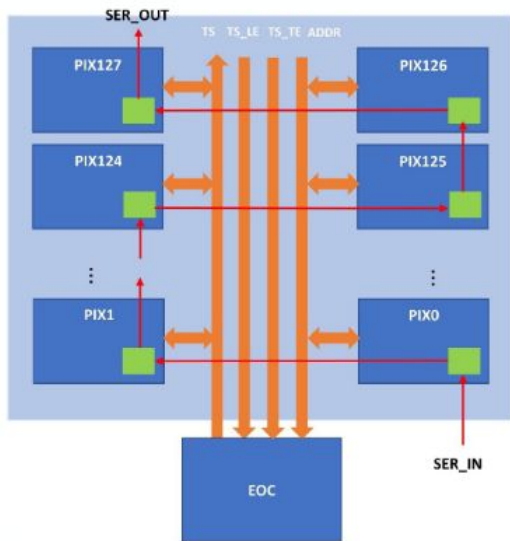
From DESY test beam:



[From C. Zhang](#)

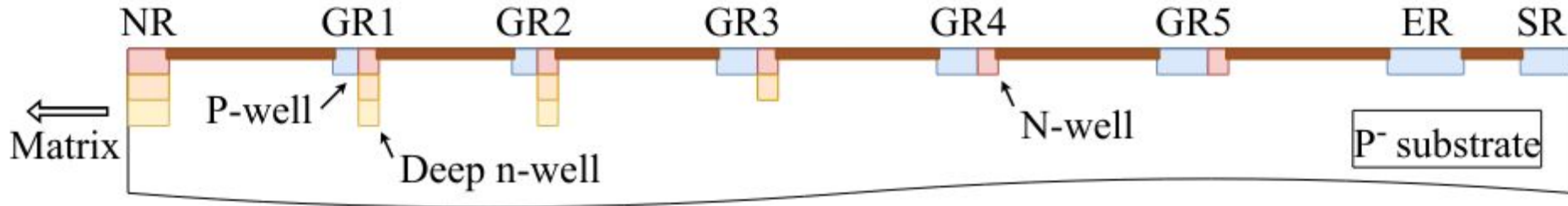
RD50-MPW4 in pixel electronics

- Configuration registers:
 - Each pixel has a serial-in 8-bit configuration register;
 - Data sent in from the bottom.



bit	Name	Description
0	INJ_EN	enables the injection circuit
1	SFOUT_EN	Enables SFOUT
2	TDAC[0]	trim-DAC configuration bit[0]
3	TDAC[1]	trim-DAC configuration bit[1]
4	TDAC[2]	trim-DAC configuration bit[2]
5	TDAC[3]	trim-DAC configuration bit[3]
6	MASK	Masks discriminator output
7	HB_EN	Enables Hitbus

Multi-ring guard ring structure



- N-Ring (NR) formed with deep n-well implant
 - three n-type implants with different depths in different colors
- n+p type ring structure for floating Guard Rings (GR1 to GR5)
 - different depths of the n-well
- Edge Ring (ER) to use the p-well implant
- ER electrically connected with the Seal Ring (SR)
- Total multi-ring structure width: 278 μm