The Precision Endcap Timing Layer of the CMS MIP Timing Detector at the HL-LHC

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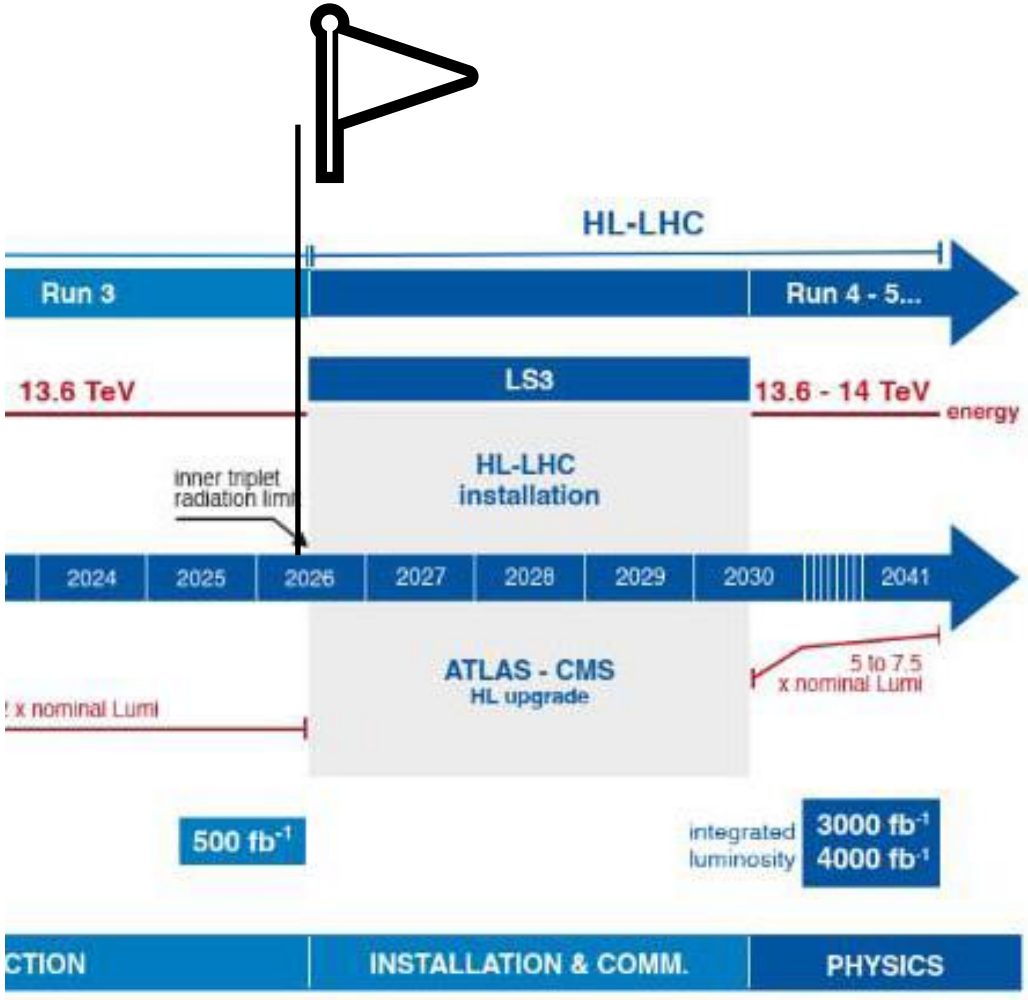
On behalf of the CMS Collaboration

The HL-LHC upgrade

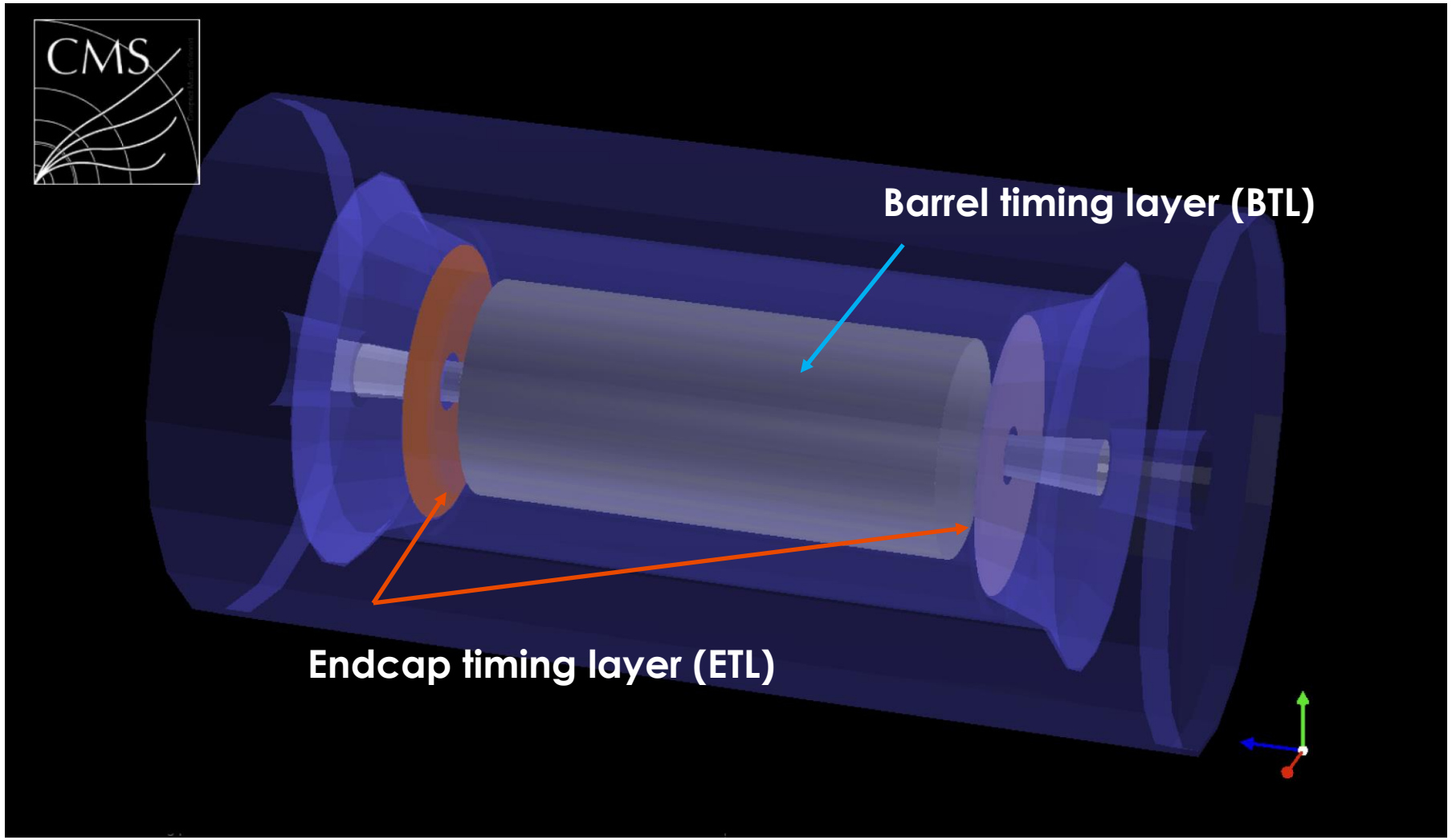
HL-LHC will start in 2030, with a factor 5–7 increase in instantaneous luminosity



- Pile-up will increase from ~50 to ~200 events per bunch crossing
- Radiation levels will significantly increase
- Physics performance would degrade without detector upgrades

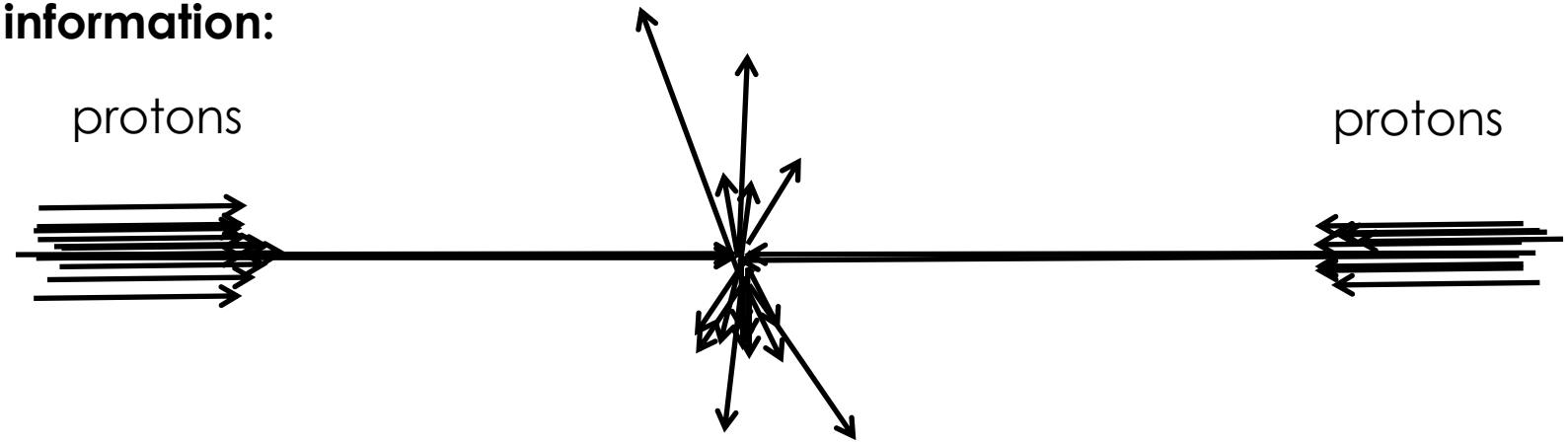
A CMS upgrade: the MIP timing detector

CMS has decided to add a timing layer covering the whole rapitidy range in order to maintain excellent physics performance in the challenging environment of HL-LCH,



Why is timing needed at HL-LHC?

No temporal information:



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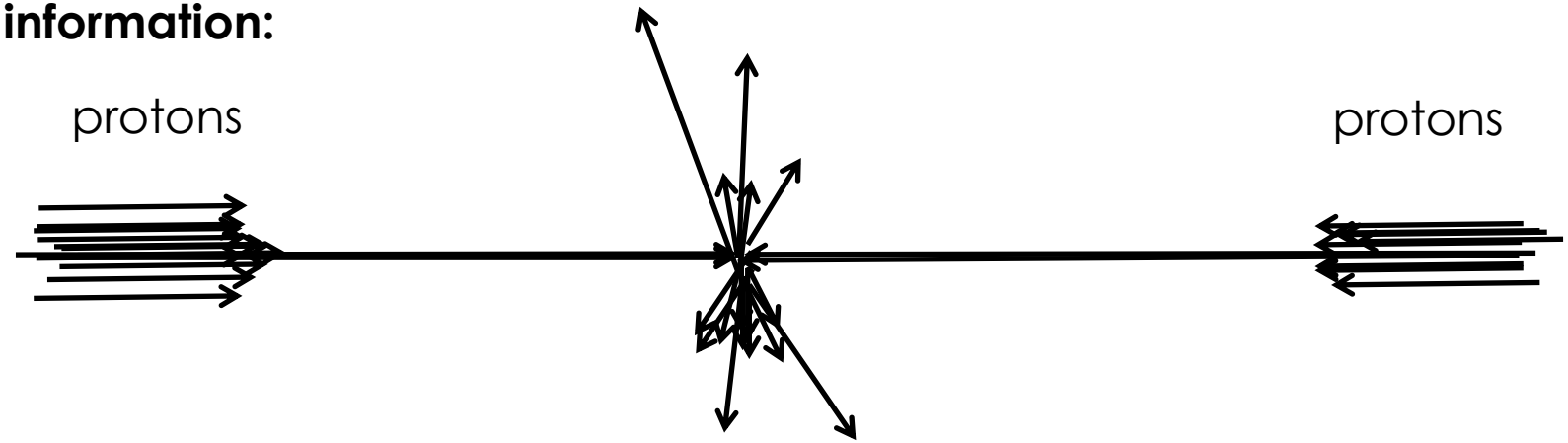
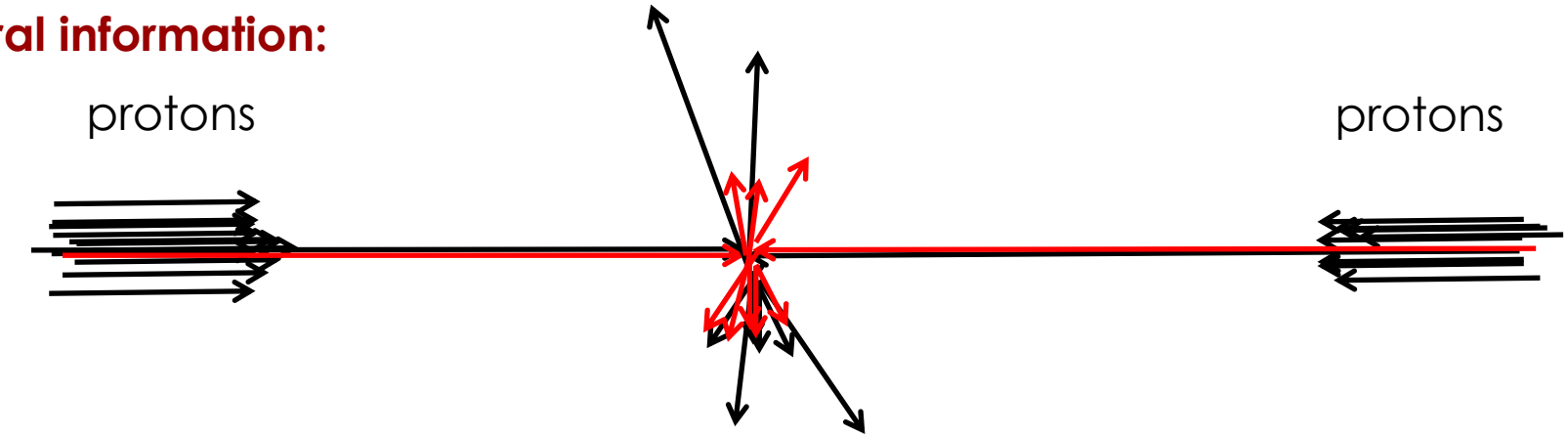


With temporal information:



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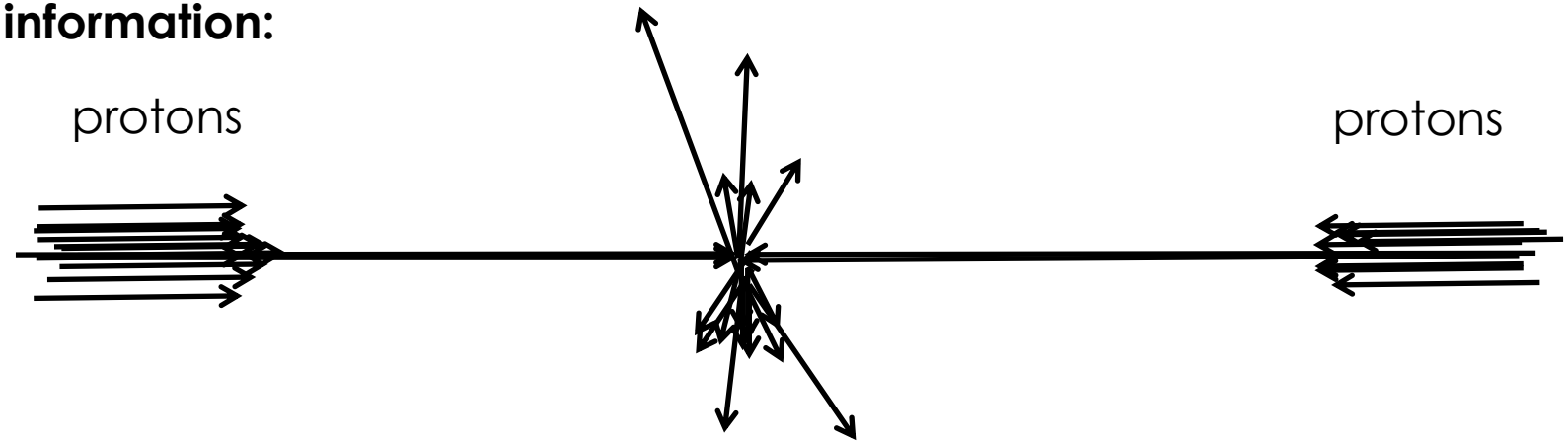

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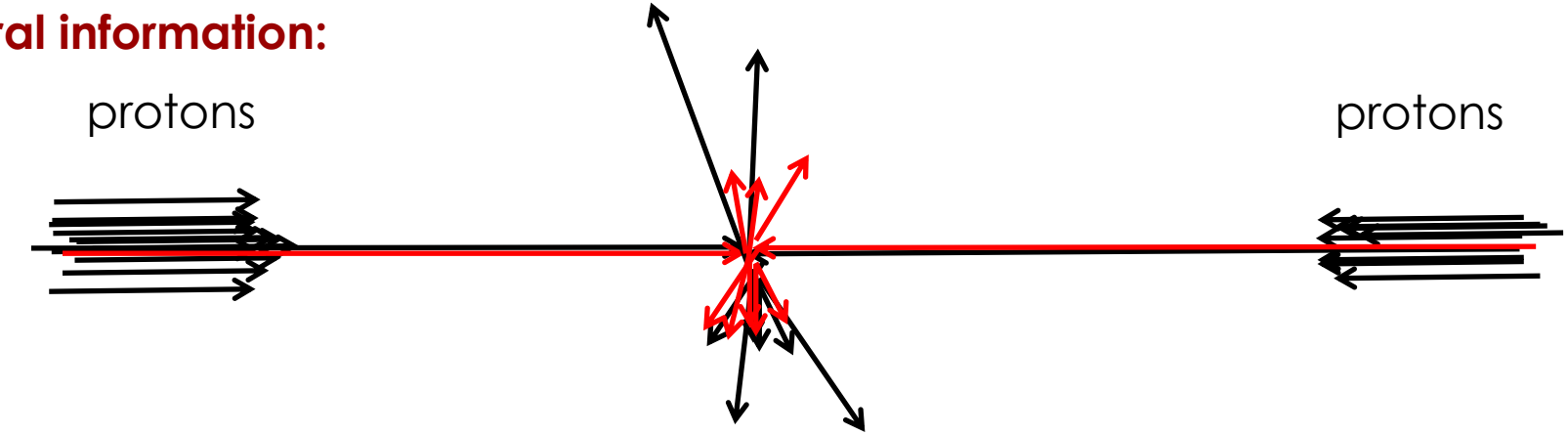


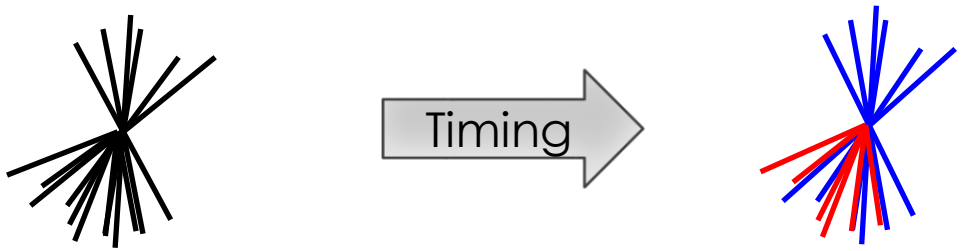
HL-LHC situation:

the collisions are so dense that vertices overlap in space

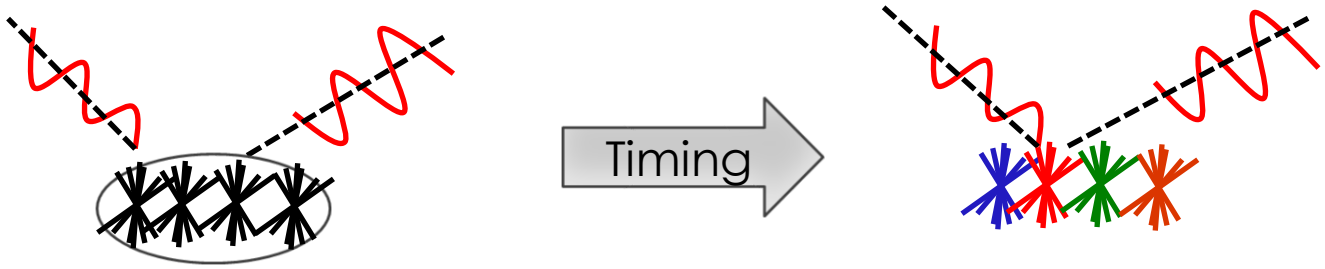
Timing allows to separate them

The timing layer: a pile-up reduction tool

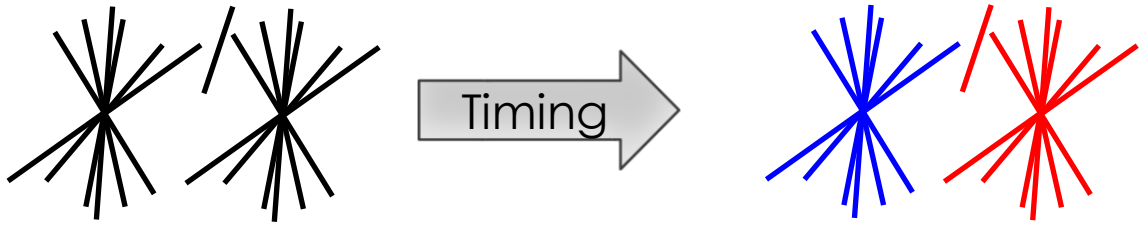
Missing Et:



H ➔ γ γ :

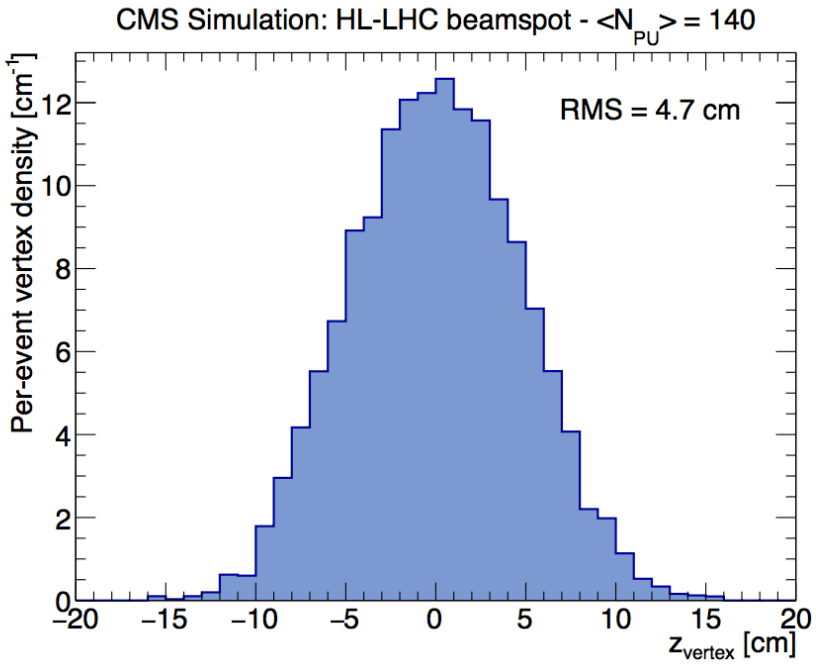


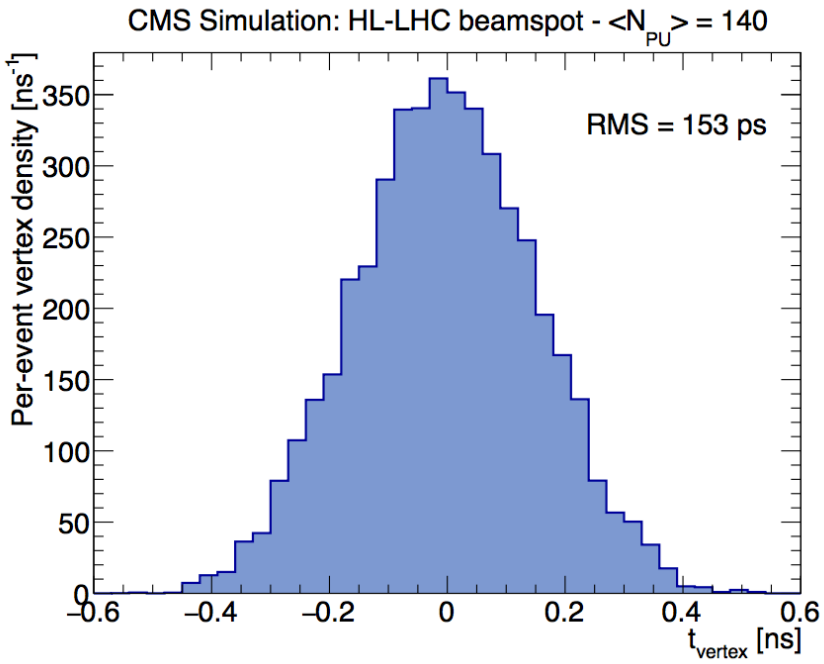
Displaced vertexes:



Timing complements tracking in the correct reconstruction of the events

What resolution do we need?

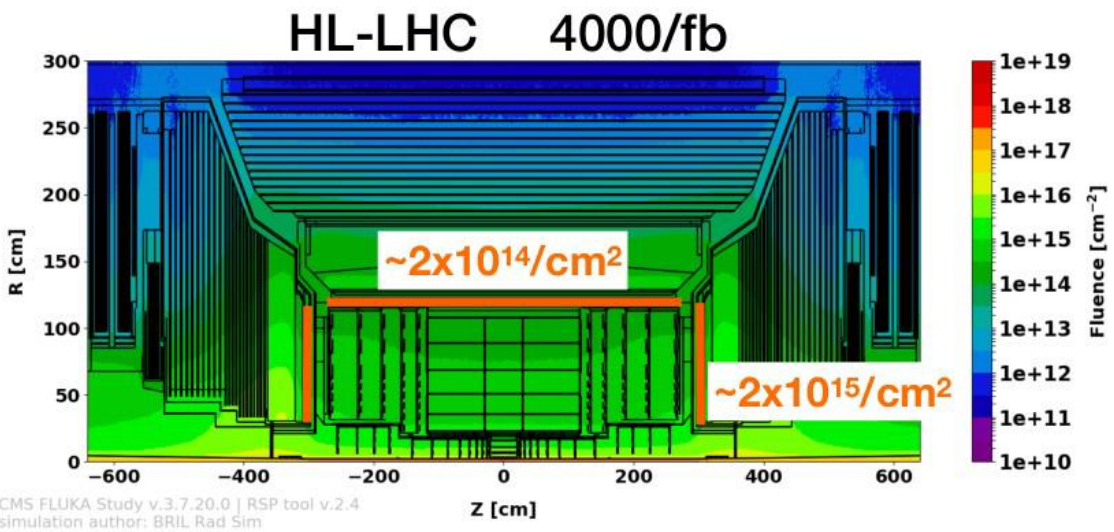


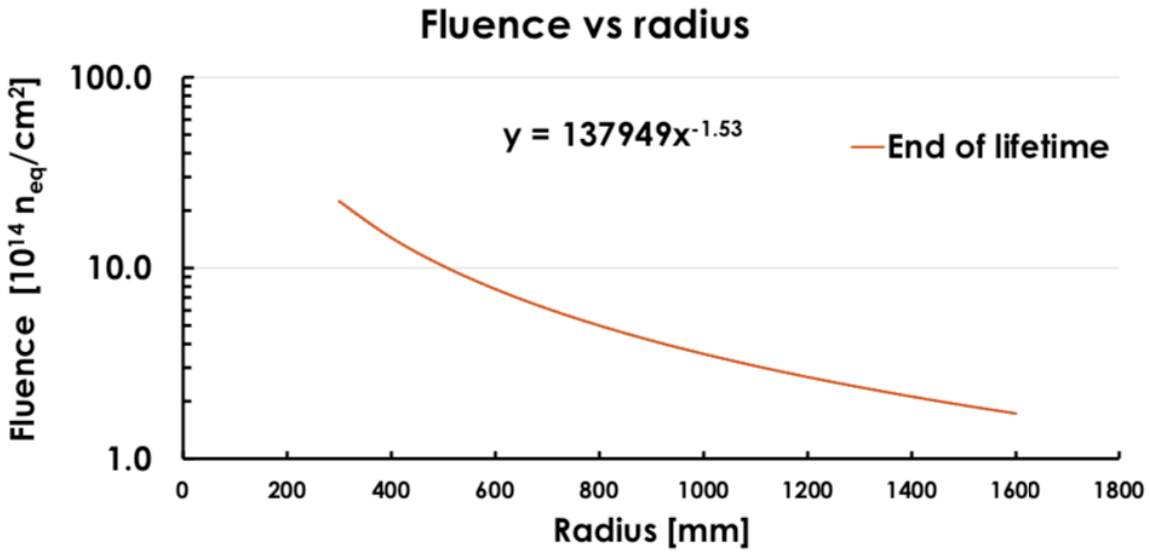


The beam spot extends over 4-5 cm, corresponding to a spread of the interaction time of about 150 ps

A resolution ~ 40-50 ps per track decreases effective pile-up by a factor of about 3

CMS radiation environment





After $\mathcal{L}_{int}$ = 4000 fb^{-1}:

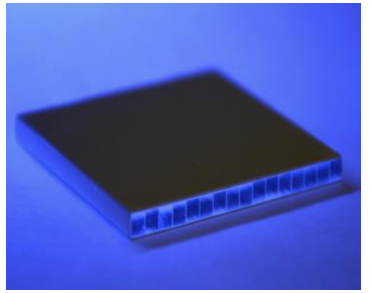
- Fluence in BTL: up to **2·10^{14} n$_{eq}$/cm^2**
- Fluence in ETL: from **1.5·10^{14} n$_{eq}$/cm^2** to **2.3·10^{15} n$_{eq}$/cm^2** at high $|\eta|$
  - About **12%** of ETL will be exposed to fluence above **1·10^{15} n$_{eq}$/cm^2**

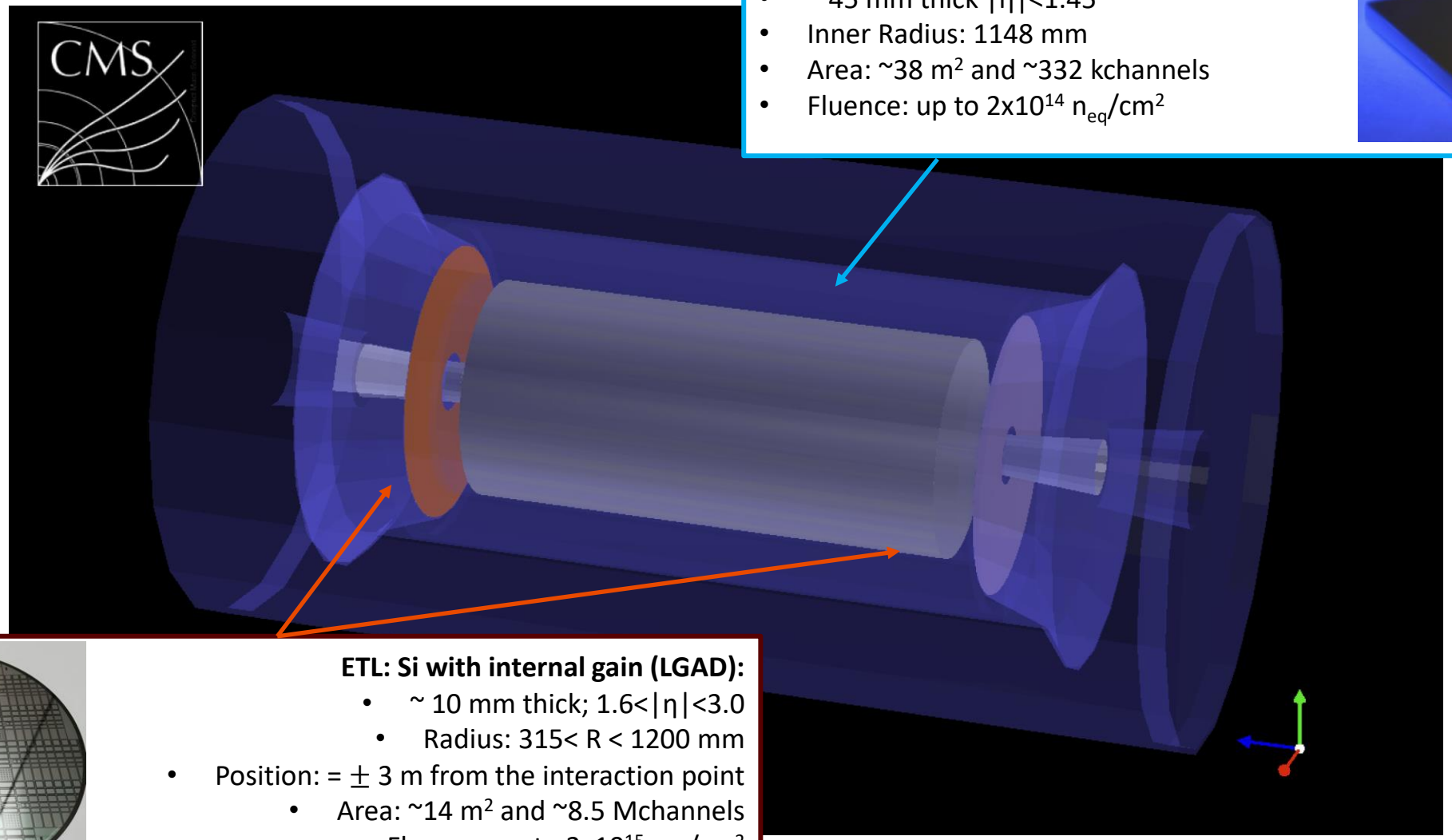
The radiation levels were key factors in the choice of technology for BTL and ETL

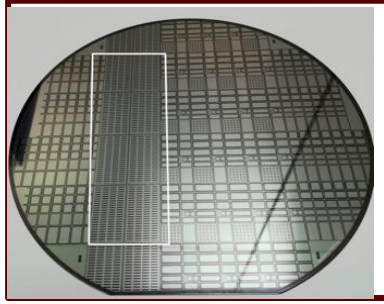
Technological choices: crystal and silicon

BTL: L(Y)SO bars + SiPM readout:

- ~ 45 mm thick $|\eta|<1.45$
- Inner Radius: 1148 mm
- Area: ~38 m^2 and ~332 kchannels
- Fluence: up to $2x10^{14}$ n_{eq}/cm^2







ETL: Si with internal gain (LGAD):

- ~ 10 mm thick; $1.6<|\eta|<3.0$
- Radius: $315< R < 1200$ mm
- Position: = $\pm$ 3 m from the interaction point
- Area: ~14 m^2 and ~8.5 Mchannels
- Fluence: up to $2x10^{15}$ n_{eq}/cm^2

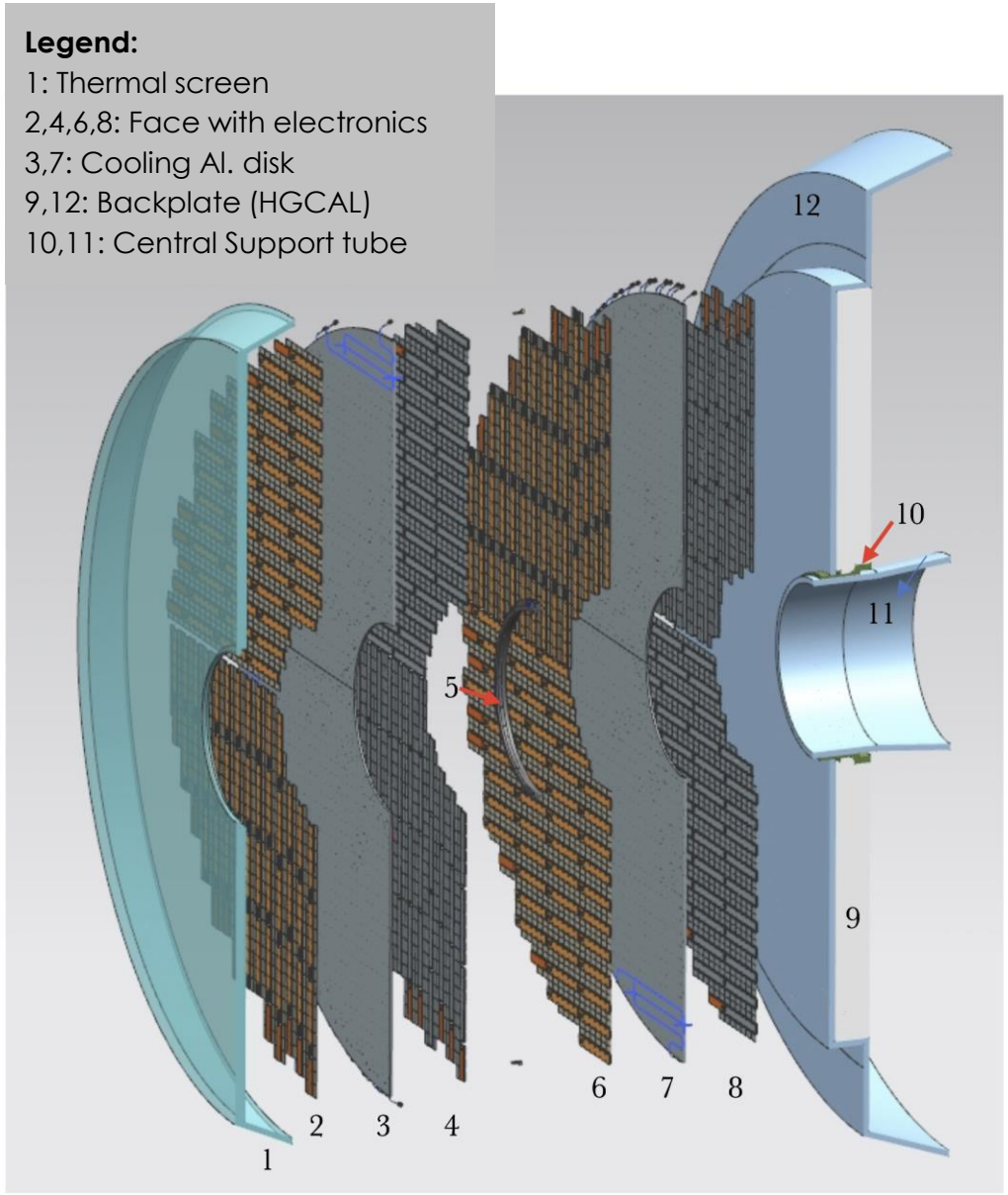
The CMS endcap timing layer (ETL)

ETL is a technological wonder…

Each of the two side:

- Very thin, ~**99 mm thick**
- Quite large, ~ **2.5 m diameter**
- Radiation resistant up to fluence ~ **$2x10^{15}$ n_{eq}/cm^2**
- Two active layers, each with **< 50 ps resolution**
- **Custom developed silicon sensors** (1.3x1.3 mm^2 pixel)
- **Custom developed read-out ASIC** (ETROC, 65 nm)
- **8.5M** channels, organized in 16x16 array
- Operating power **~ 35 kW**
- Operating temperature **-30° C (**evaporated CO_2)
- Aluminium cooling structure with stainless steel piping

Installation in CMS during 2029…



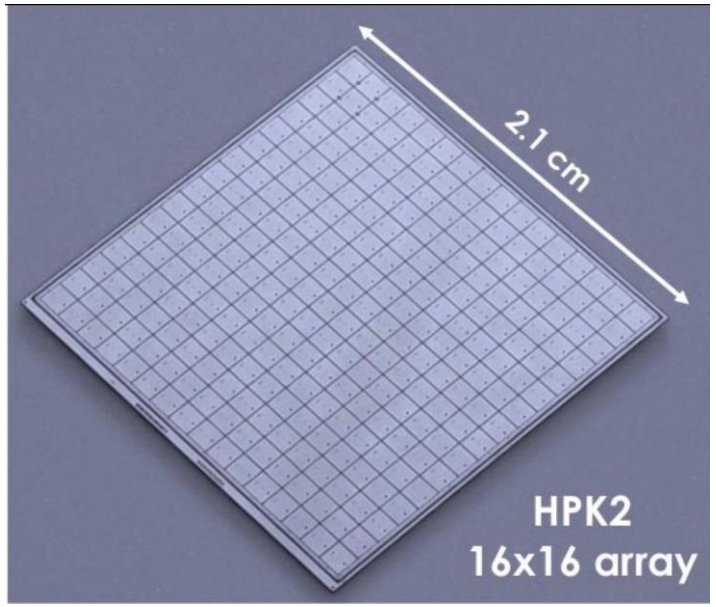
The ETL UFSD silicon sensors

Sensor Requirements

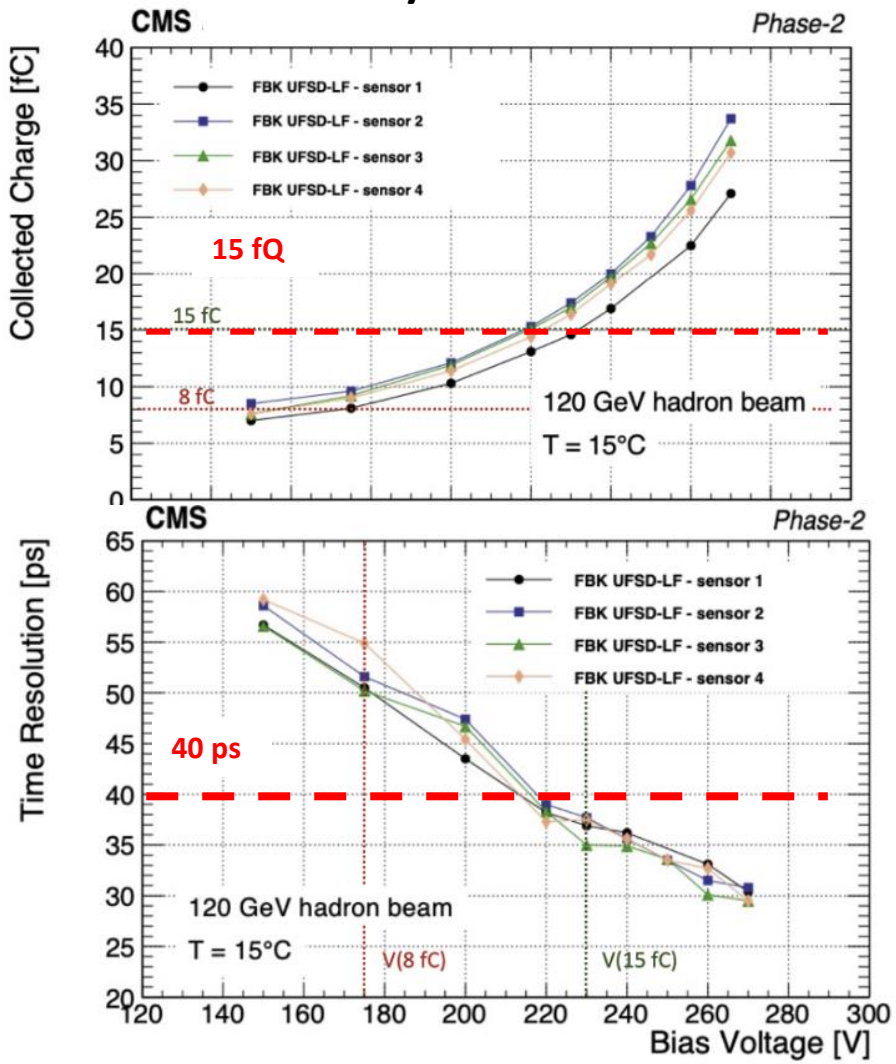
- **16x16 pixel matrix** with pixel **pitch** of **1.3 mm**
- Delivered **charge**
  - **> 15 fQ** in unirradiated device
  - **> 8 fQ** up to the end of operation ($1.5 \cdot 10^{15}$ n_{eq}/cm^2)
- Timing Resolution **< 40 ps/hit**
- **Fill factor ~ 90%**

Foundries:

- HPK
- FBK-LFoundry



LFoundry sensors

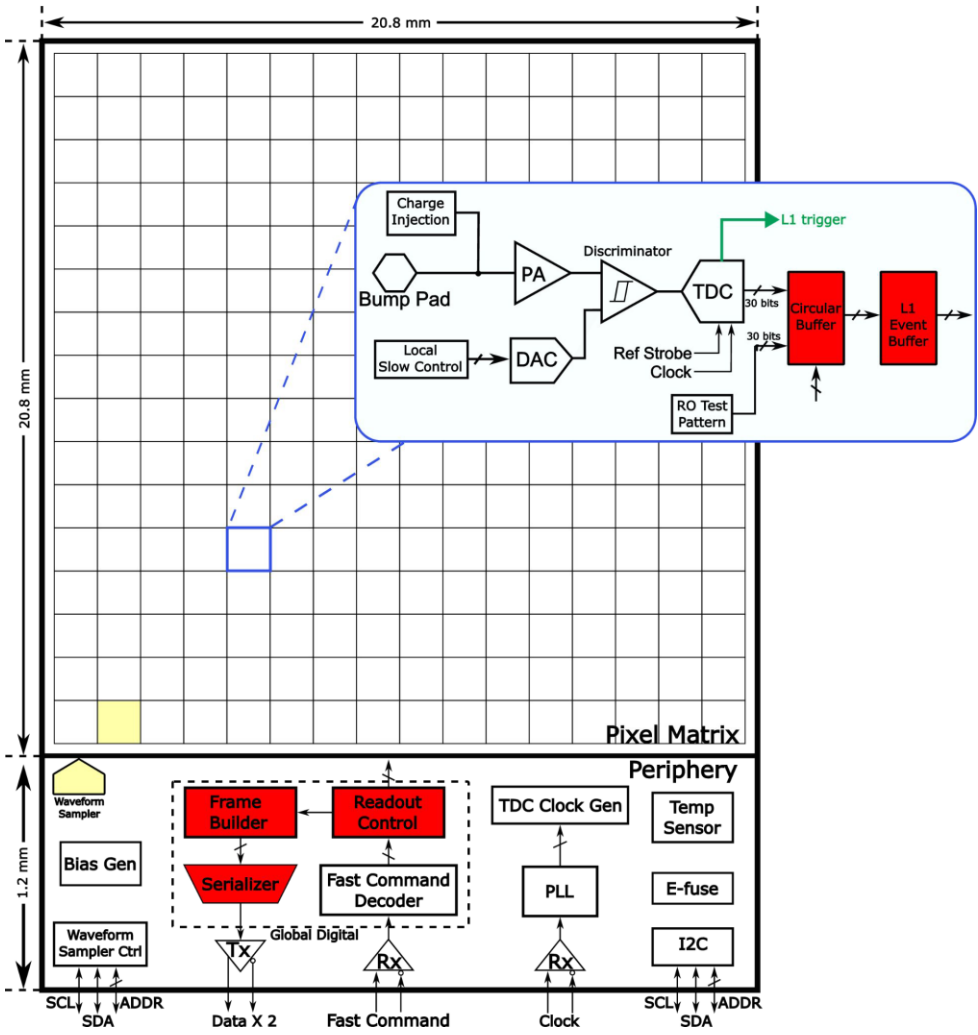


The ETL read-out ASIC

ETROC design architecture and constraints:

- **Front-end: Pre-Amplifier + Discriminator + TDC**
- **Self-Calibration TDC**
  - Time of Arrival (ToA)
  - Time over Threshold (ToT)
- 16x16 array with 1.3 mm pitch in **TSMC CMOS 65 nm** technology
- 40 MHz Reference clock
- **Low Power: 1W/chip** (240mW/cm^2) at 1.2V, **< 4mW/Ch**
- **Radiation hardness** at **100MRad** over 3 ab^{-1} at HL-LHC

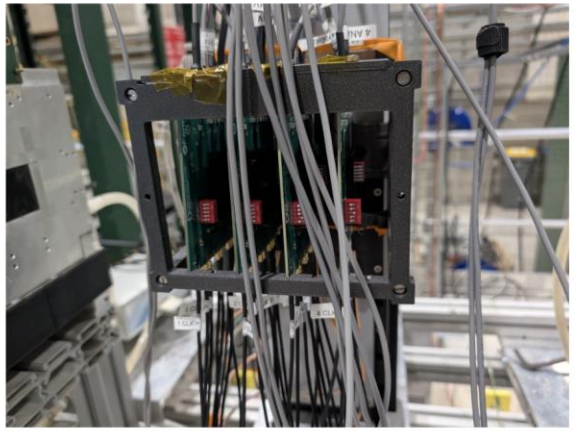
Goal: achieve ASIC contribution to the temporal resolution < 40 ps

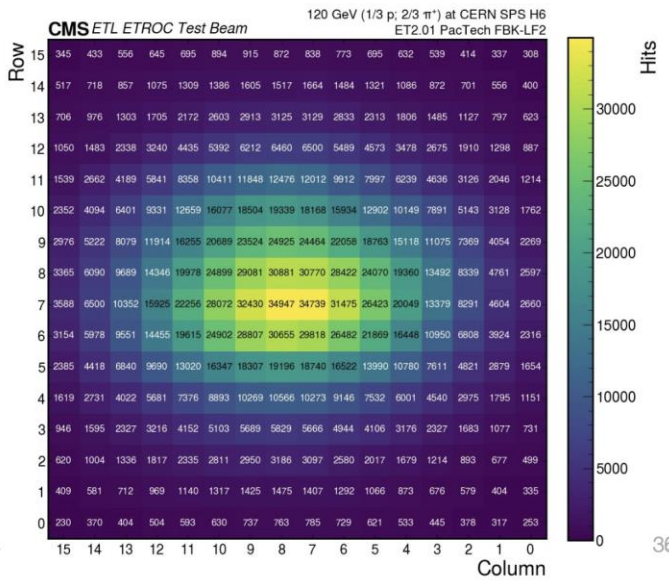


Sensor-ETROC @ testbeam

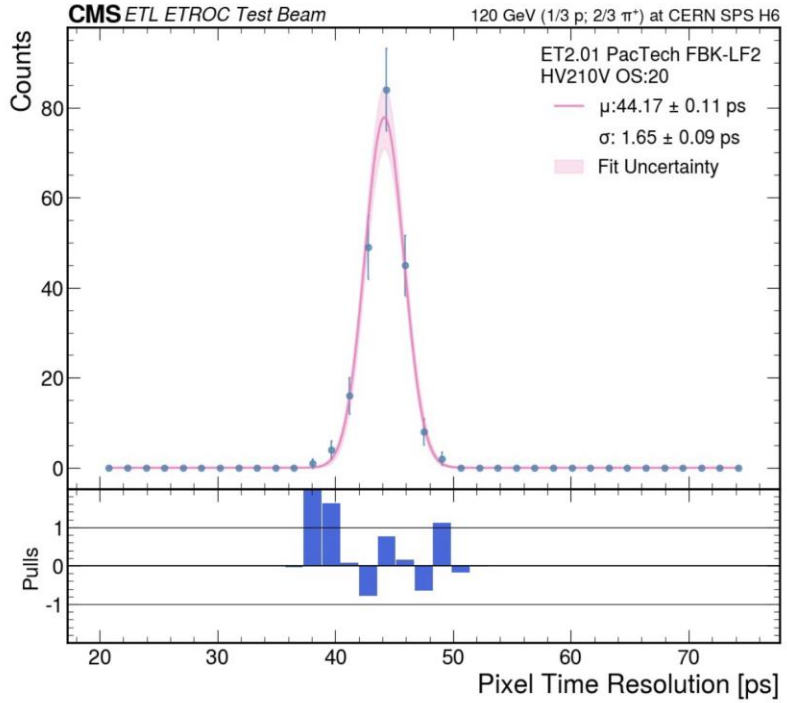
Highlights:

- 100% pixels working
- Very uniform noise and baseline
- **Resolution of 256 pixels: 44 ps**
- **Sigma of 256 pixels: 1.85 ps**





Observed ~ 44ps with FBK-LF sensor at room temperature

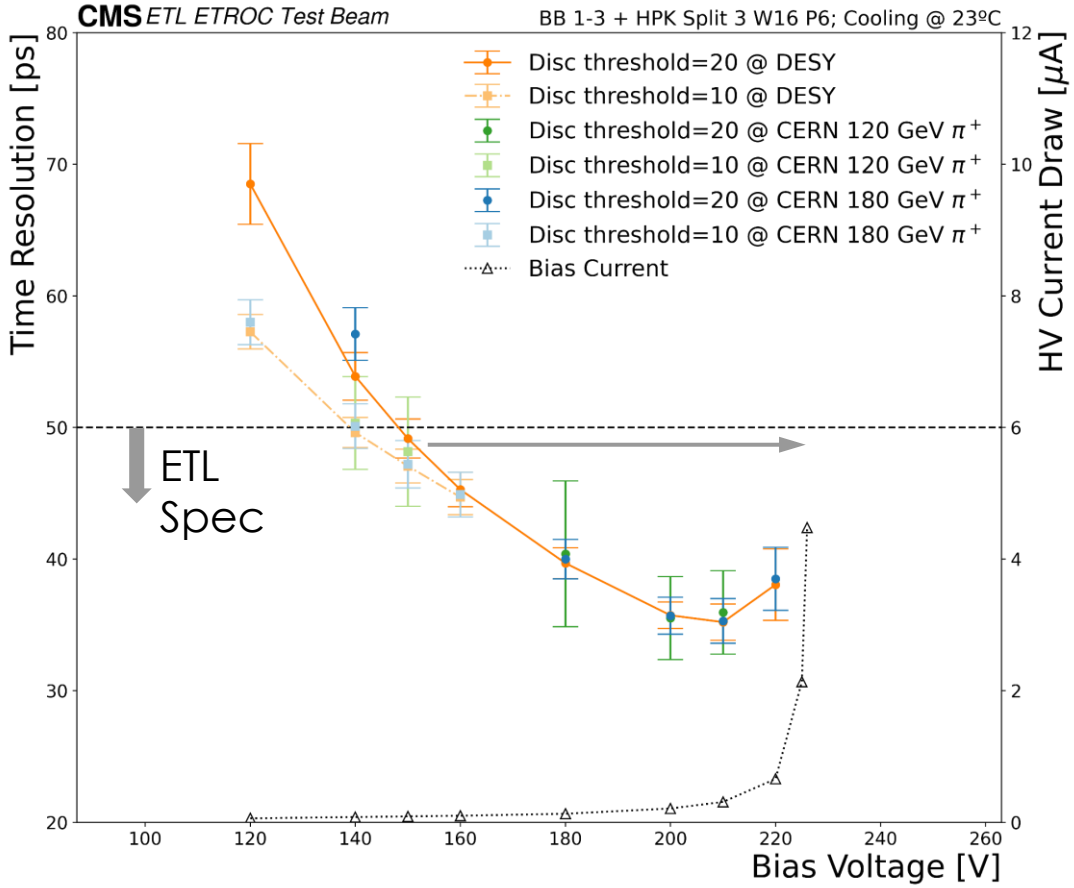


The results demonstrate uniform, production-quality performance across the full pixel matrix

Sensor-ASIC test beam results

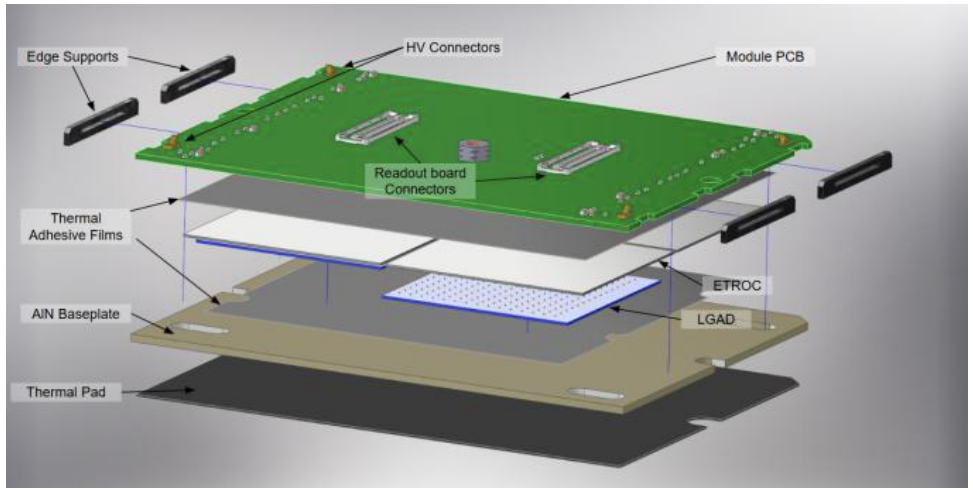
Sensor-ETROC2 combination achieves the required resolution, with more than **70V operating range**

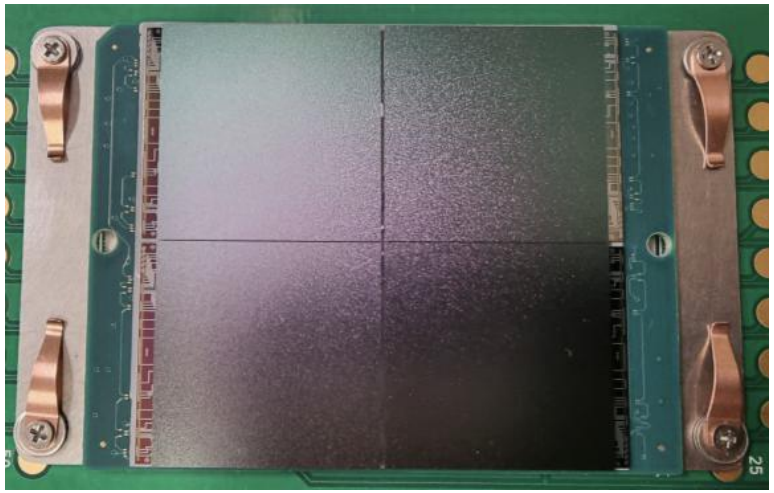
Sensors and ASIC have passed the final reviews and are now entering the pre-production phase



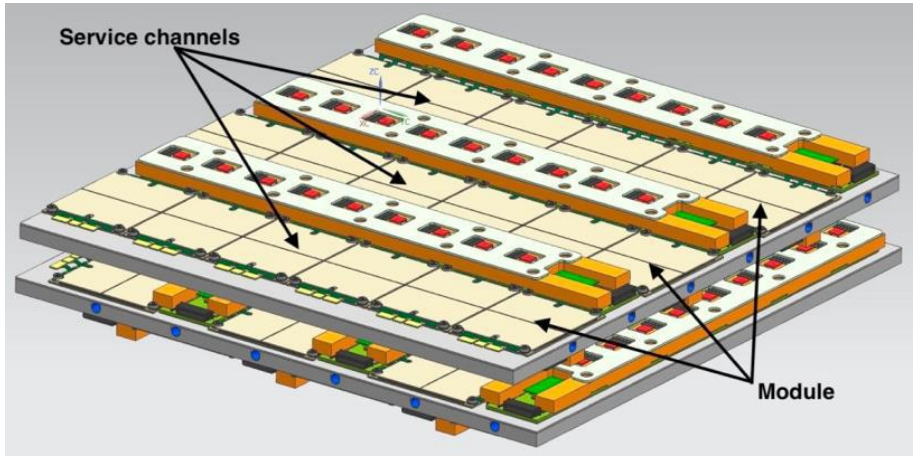
Putting things together

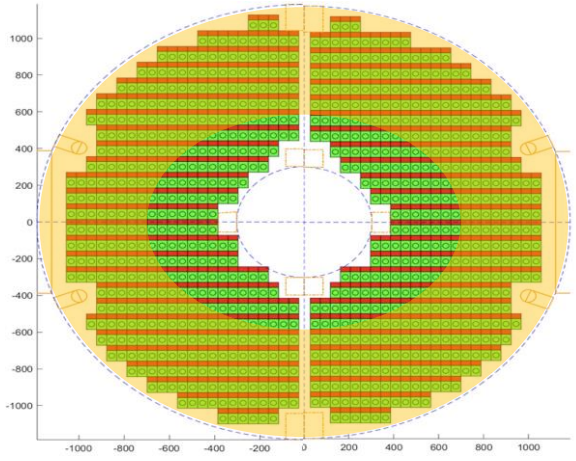
4 hybrids are placed together to form a module





Modules are place on service hybrids to cover the whole ETL disk





Summary and outlook

- **The CMS experiment** has decided to install an innovative new detector, the MIP timing layer, **to mitigate the effects of increased pile-up at HL-LHC**
- The endcap timing layer, ETL, is instrumented with pixelated LGAD silicon sensors, readout by a dedicated ASIC.
- The sensor-ASIC combination achieves the TDR temporal resolution, **< 50 ps/ track**
- **ETL is now entering the construction phase, leading to installation by 2029**