



A FPGA-based L1 trigger system design for Super Tau Charm Facility

Yuhe Huang

On behalf of STCF Trigger Working Group

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Outline

1. STCF overview and requirement for trigger system
2. STCF trigger system preliminary design
3. FPGA-based L1-level hardware platform R&D
 - Hardware platform and prototype design
 - MDC sub-trigger hardware design
 - ECAL sub-trigger hardware design
 - Global trigger hardware design
4. Beam test
5. Summary

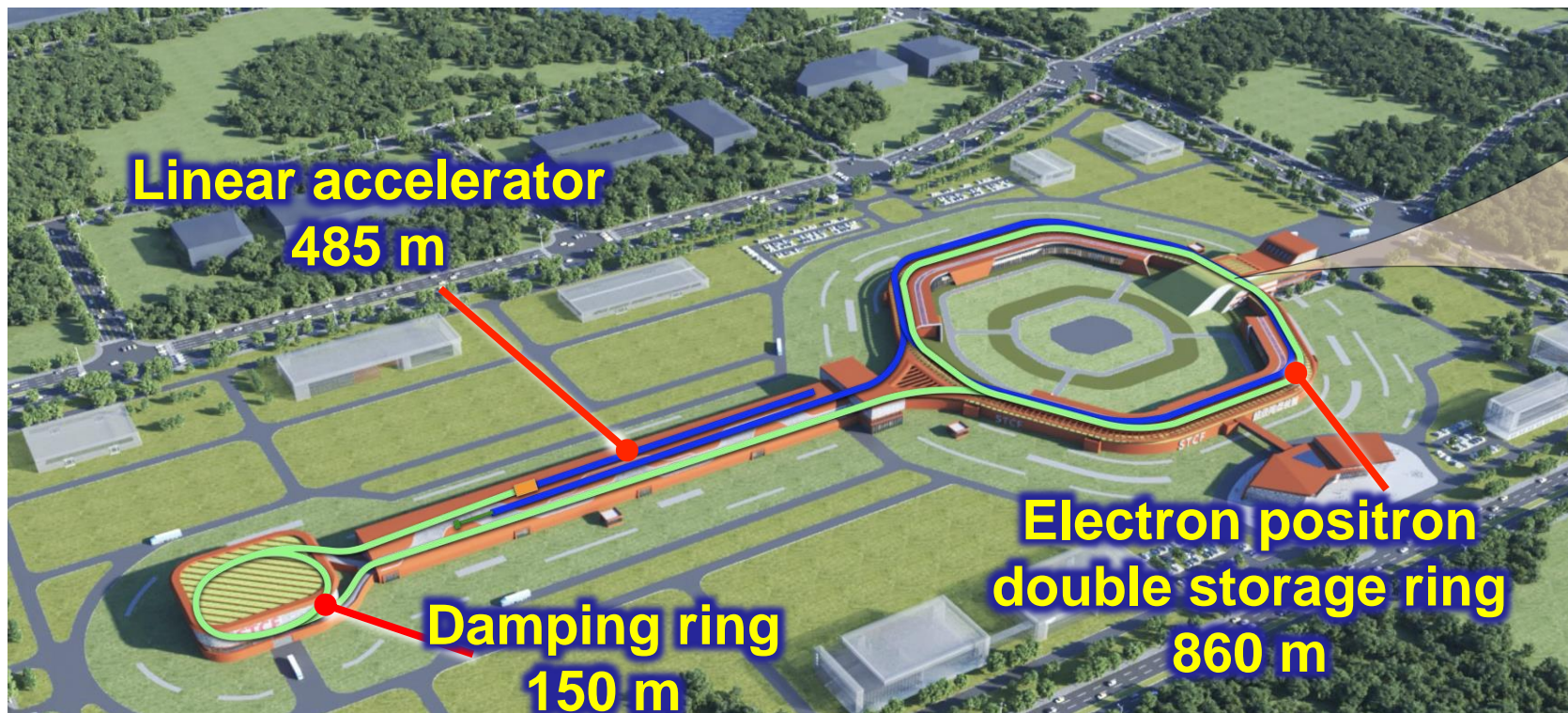


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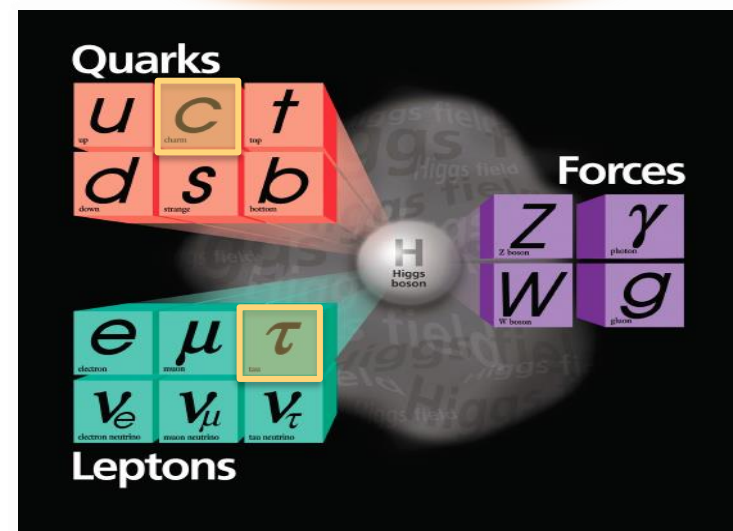
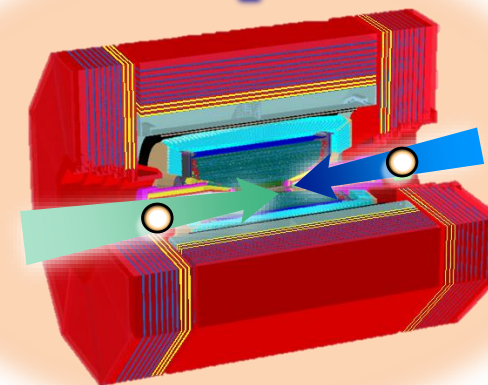
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The Overview of Super Tau Charm Facility (STCF)



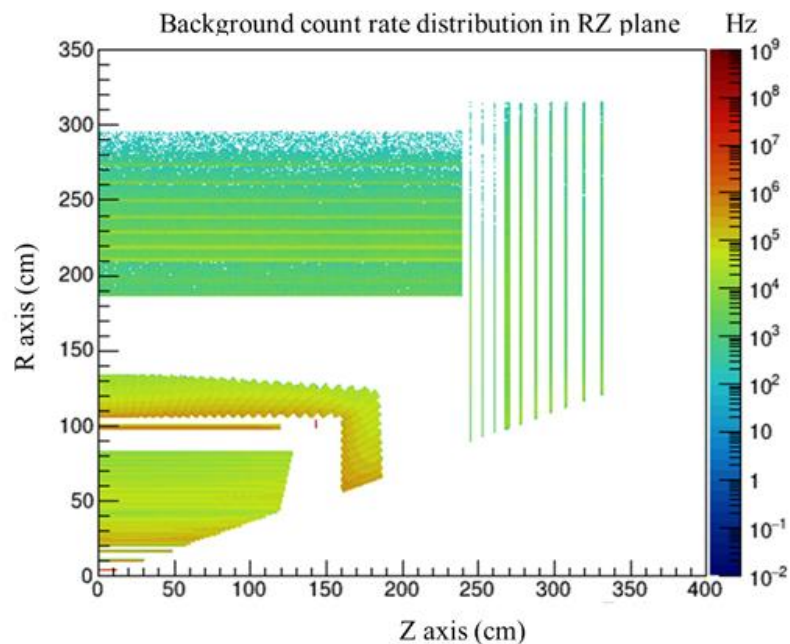
Detector spectrometer



- $E_{CM} = 2-7\text{GeV}$, luminosity over $0.5 \times 10^{35} \text{cm}^{-2} \text{s}^{-1}$
- Event rate within 2 days \approx 1 year of current facility



Requirements of STCF trigger system



□ Main challenges of STCF

- High background
 - MDC: 180 kHz/wire
 - ECAL: 580 kHz/crystal
- High physics rate (400 kHz)
- High count rate

| Component | Readout time window | Event size(B) | Total(B/s) |
|---------------------|---------------------|---------------|------------|
| ITK(Silicon) | 1000 ns | 14300 | 5.72G |
| ITK(μ RWELL) | 600 ns | 17232 | 6.89G |
| MDC | 800 ns | 20400 | 8.16G |
| PID(RICH) | 200 ns | 15600 | 6.24G |
| PID(DTOF) | 100 ns | 7380 | 2.95G |
| ECAL | 400 ns | 15000 | 6.00G |
| MUON | 600 ns | 262 | 105M |
| Total(Silicon) | - | 72.9k | 29.2G |
| Total(μ RWELL) | - | 75.9k | 30.4G |

□ Demand of STCF L1-trigger System

- High trigger efficiency ($\sim 99\%$)
- Low background trigger rate ($< 50\text{kHz}$)
- High throughput, low latency
- Good adjacent event distinguishing ability



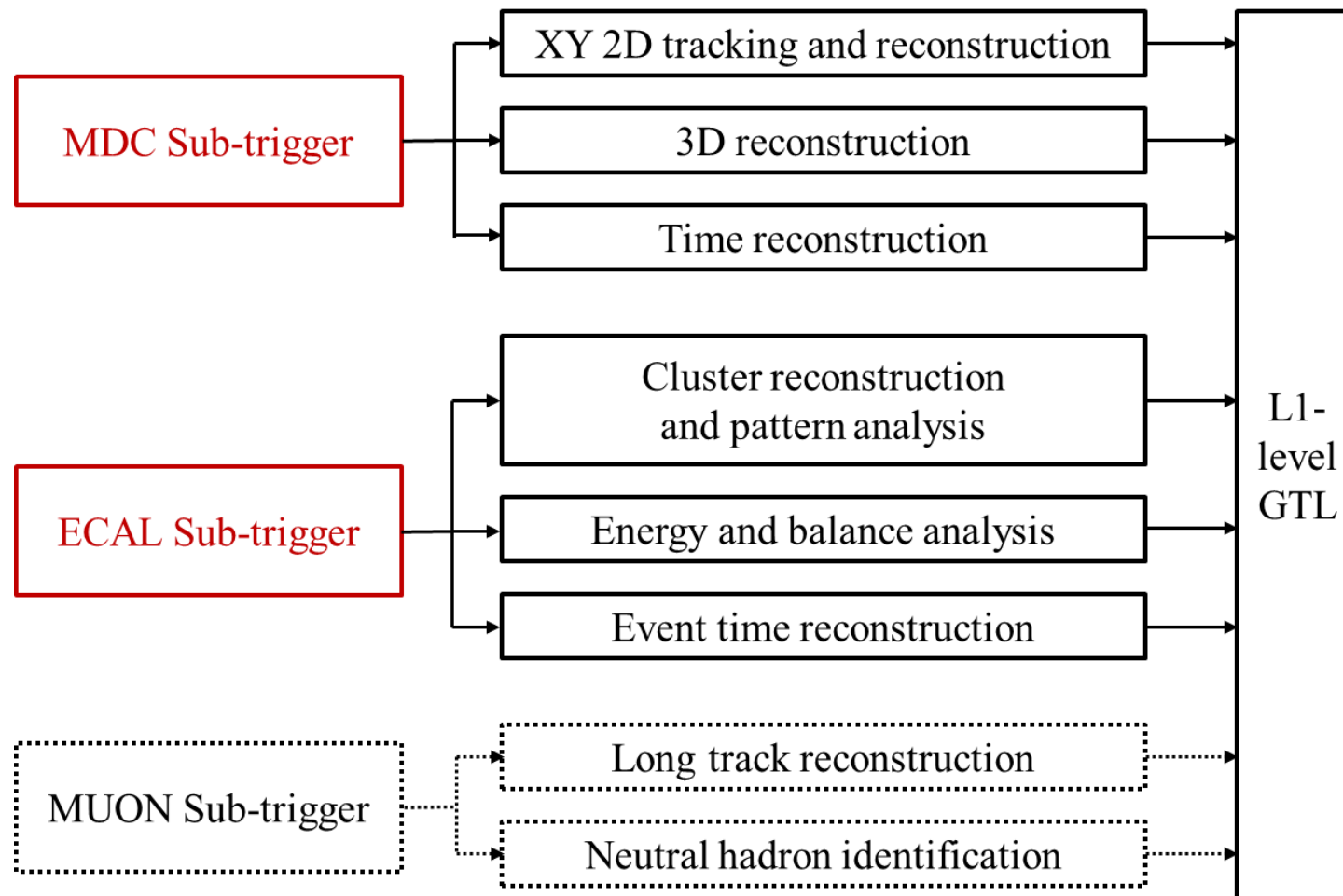
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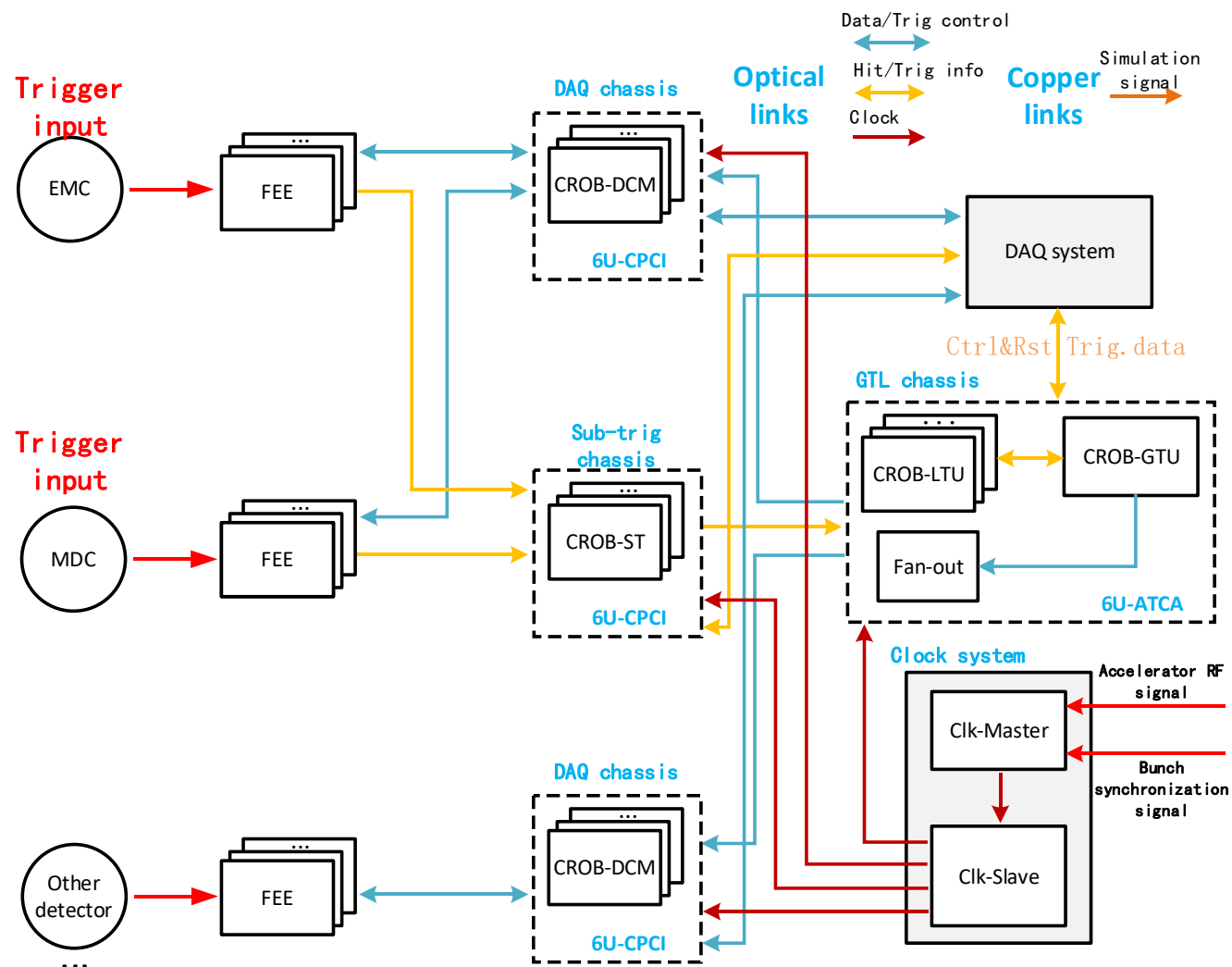
STCF L1-trigger system preliminary design

- **ITK**: high background
- ✓ **MDC**: key tracking detector
- **BTOF**: complex reconstruction
- **DTOF**: complex reconstruction
- ✓ **ECAL**: key calorimeter, fast response
- **MUON**: identification of $\mu/\pi/n/K_L$





STCF L1 trigger hardware design



- **CROB**: Common ReadOut Board
- **CROB-DCM** for data collection for DAQ system
- **CROB-ST** for data collection for L1 sub-trigger
- **CROB-LTU** for data processing of sub-trigger logic
- **CROB-GTU** for trigger decision of global trigger logic
- Global clock: 40 MHz



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Hardware platform key board test

□ The 3rd version of CROB-LTU

CROB-LTU



FMC+ sub-board



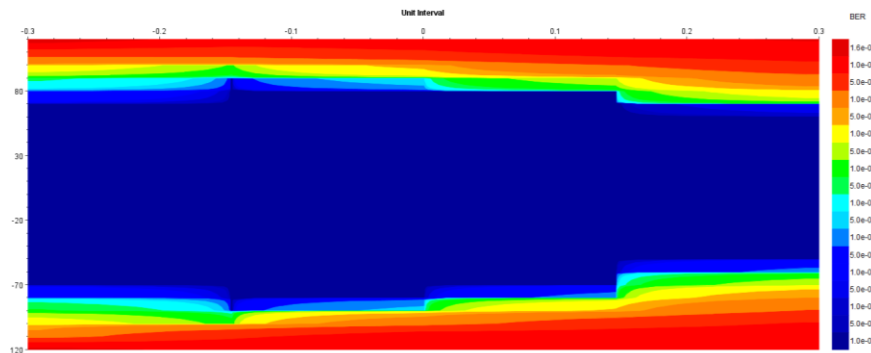
Data simulation board



CTM board



□ 10 Gbps eye map of FMC+



□ Chassis testing



➤ CROB-LTU

- 3rd version of key boards have been manufactured and tested
- 8 DDR4 modules all usable

➤ FMC+

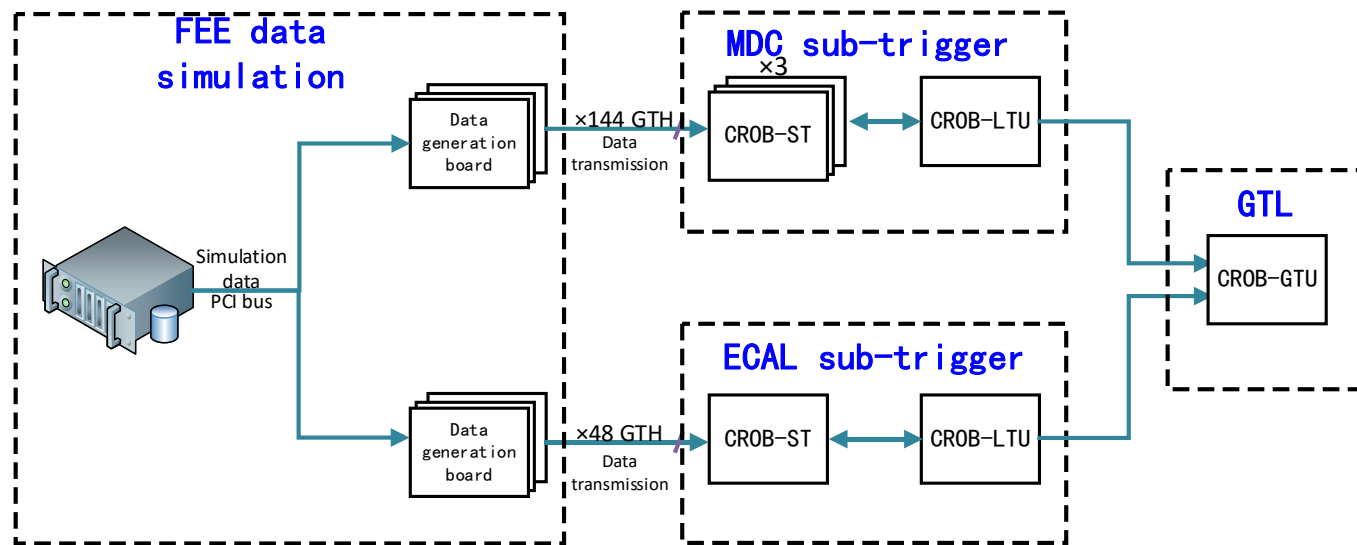
- high-frequency optimizing

➤ Data simulation board and CTM board

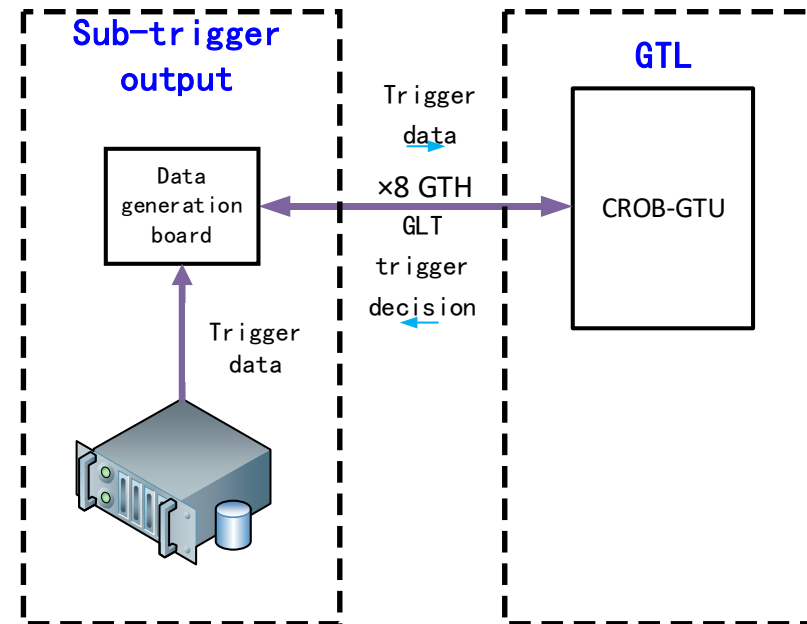
- Testing completed

L1 trigger prototype

□ Prototype for frame test and sub-trigger logic



□ Prototype for global trigger logic



- Prototype: 1/8 MDC (cover 1/3 of MDC)、1/4 ECAL
- Frame verification: data transmission, latency
- Sub-trigger algorithm performance evaluation
- GTL performance evaluation



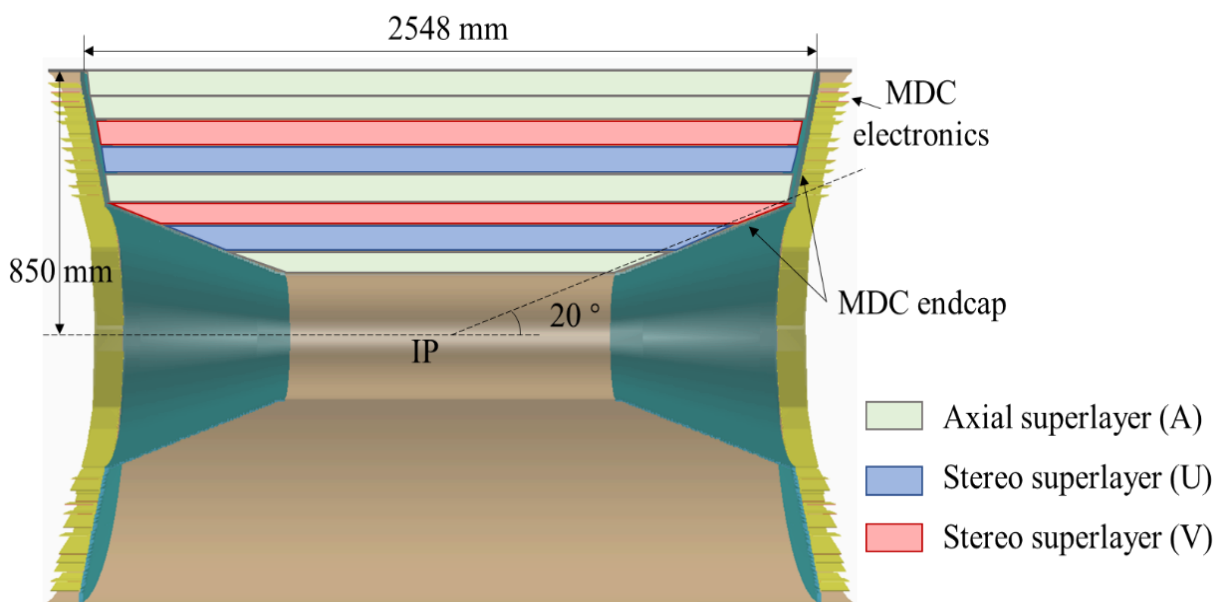
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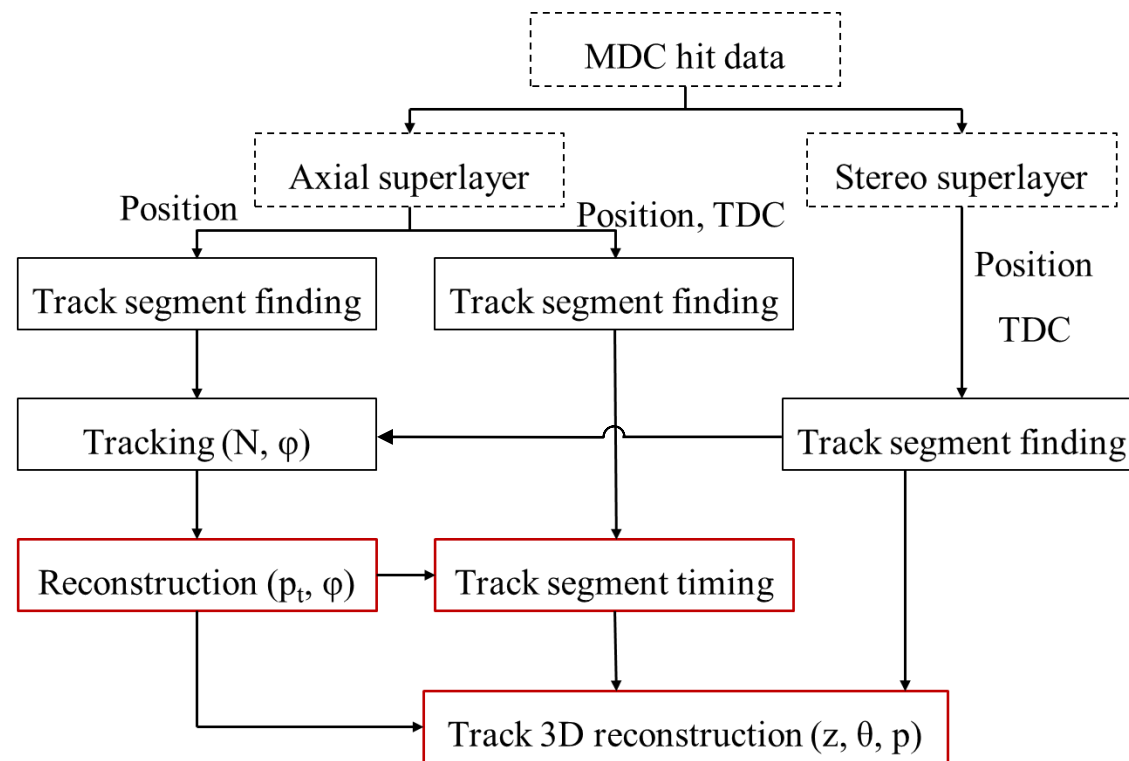
MDC sub-trigger

□ MDC structure

- 4 × axial superlayer
- 4 × stereo superlayer

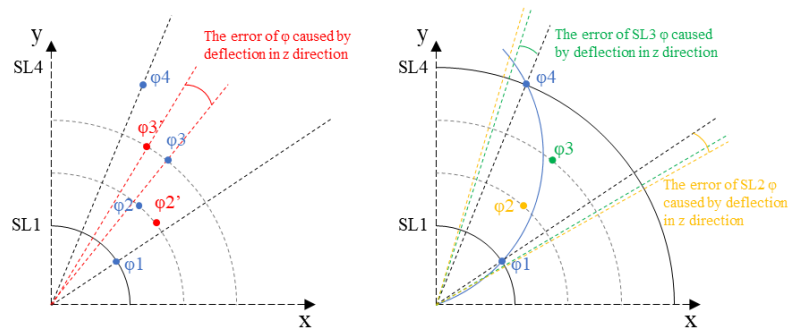


□ MDC sub-trigger logic



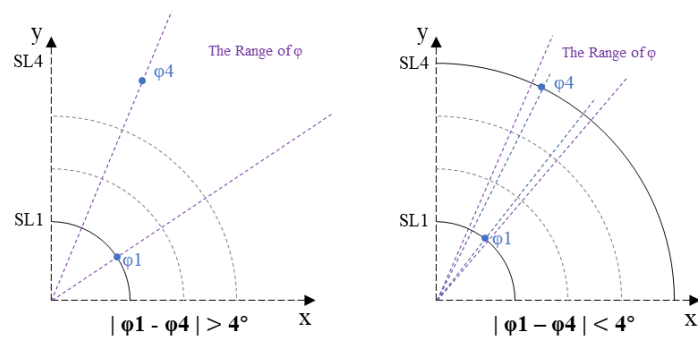
MDC sub-trigger

Introducing stereo superlayers in 2D tracking



Criterion 1: if $\phi_1 < \phi_4$ then $\phi_2' < \phi_3'$

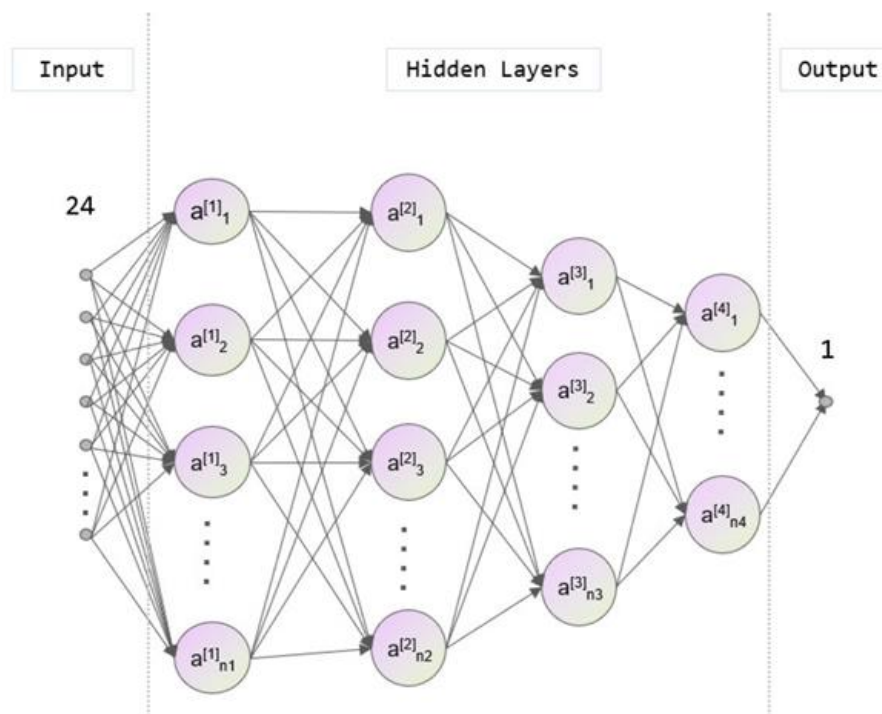
Criterion 2: The candidate ϕ_2 and ϕ_3 are in their corresponding color range



Criterion 3: The range of candidate ϕ expands if $|\phi_1 - \phi_4| < 4^\circ$

- Single track efficiency exceeds 99%
- Reduces background false tracking rate in charged trigger channel by 45%

3D reconstruction



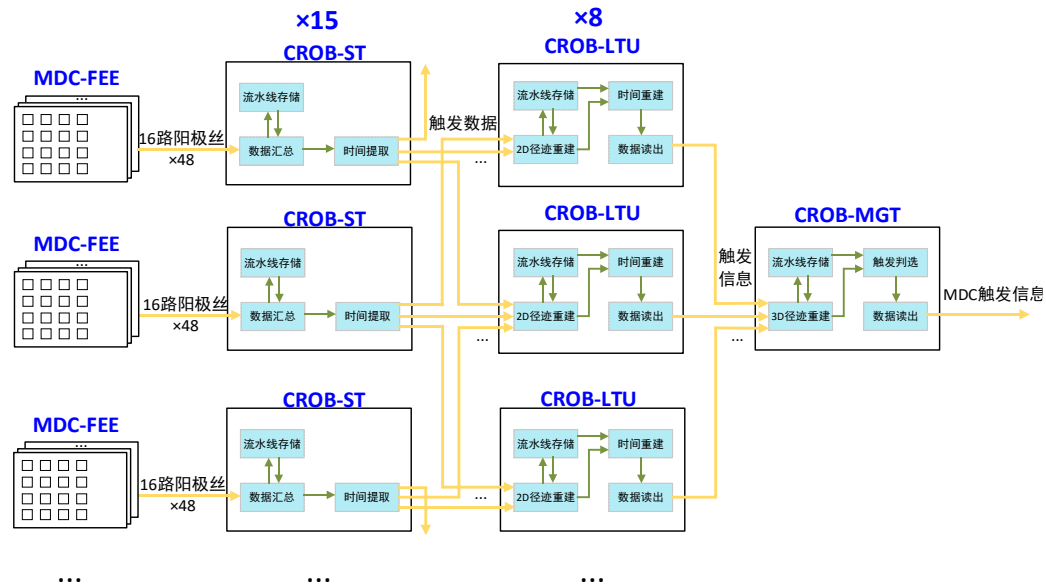
➤ Multi-layer fully connected neural network (MLP)

- Input: TS numbers and TDC for 8 superlayers
- Output: z-vertex in various pt regions



MDC sub-trigger hardware design

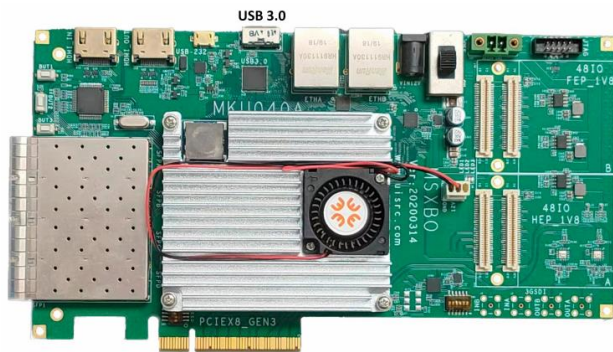
The MDC sub-trigger hardware design



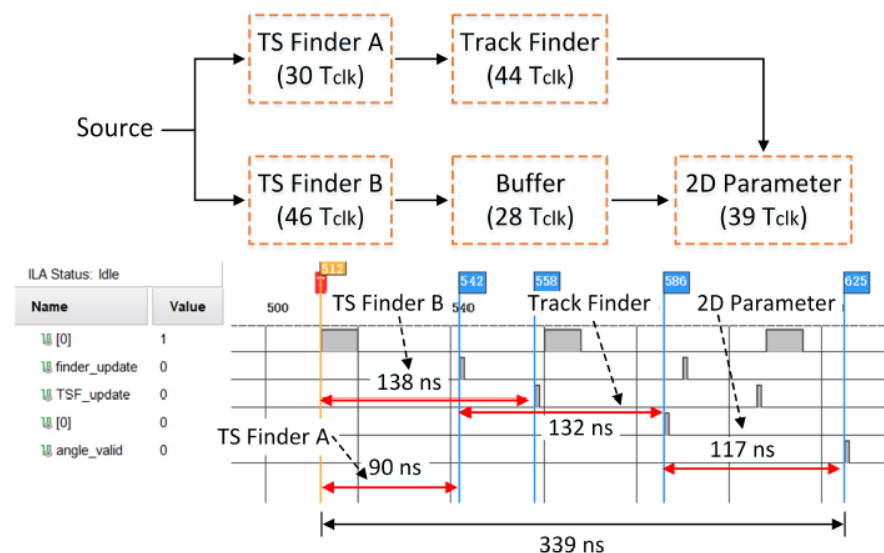
Track segment trigger efficiency in evaluation board

| Event Types | 4/4 Threshold | 3/4 Threshold | 2/4 Threshold |
|-------------------------------|---------------|---------------|---------------|
| $J/\Psi \rightarrow k^+k^-$ | 97.6% | 98.2% | 99.6% |
| $J/\Psi \rightarrow p^+p^-$ | 91.9% | 93.8% | 99.2% |
| $J/\Psi \rightarrow Anything$ | 96.1% | 97.1% | 99.3% |
| False trigger rate | 0 | 0.6 KHz | 8.8 KHz |

FPGA evaluation board



Latency measured in FPGA evaluation board

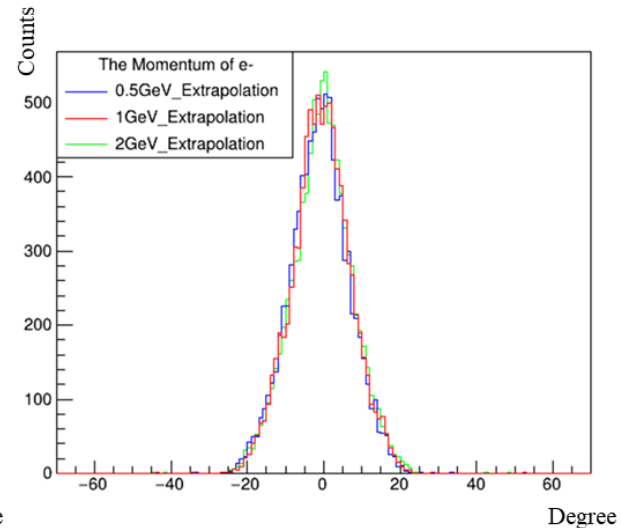
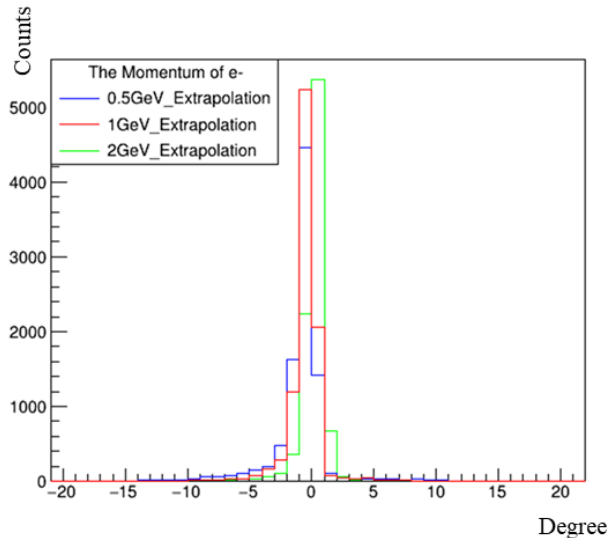
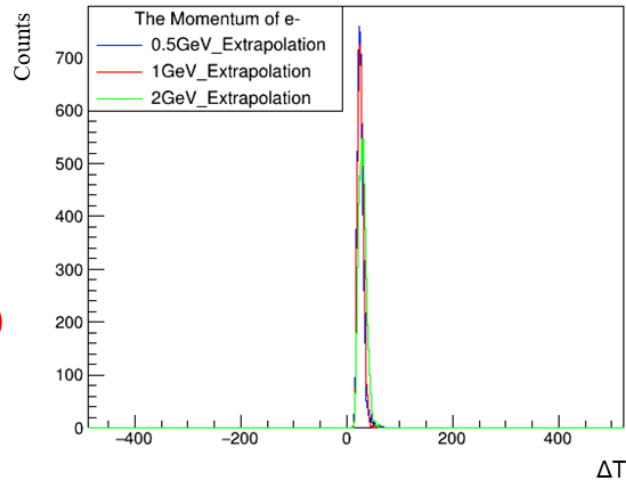




MDC sub-trigger performance

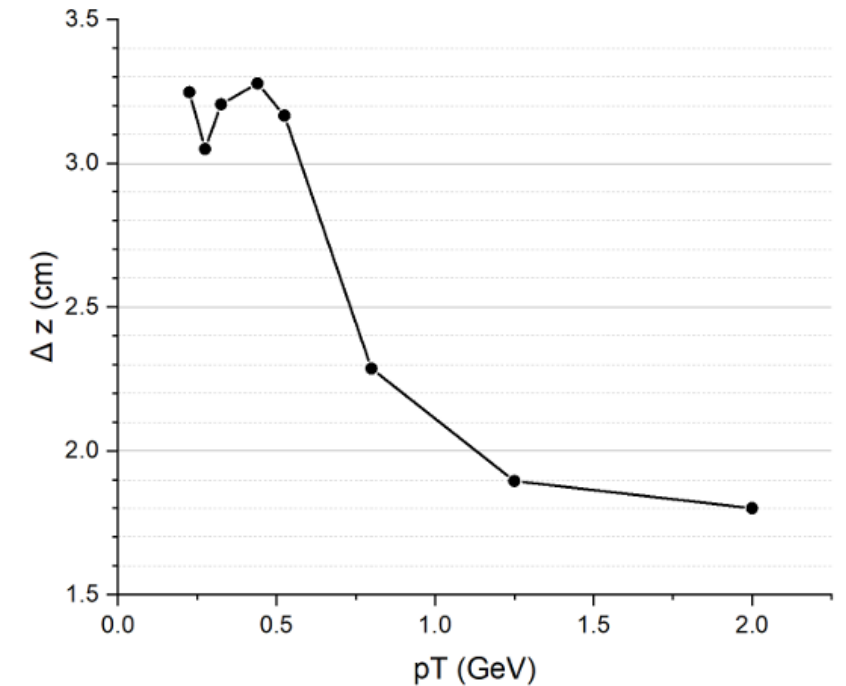
2D and time reconstruction

- σ_T : ~ 6.6 ns
- σ_θ : $\sim 7.9^\circ$
- σ_φ : $\sim 2.5^\circ$
- Latency: 340 ns (2D) + 210 ns (timing)



Z-vertex resolution of different pT

- DSP: 71% \rightarrow 4%
- FF: 29 % \rightarrow 4%
- LUT: 19% \rightarrow 17%
- Latency: 125 ns





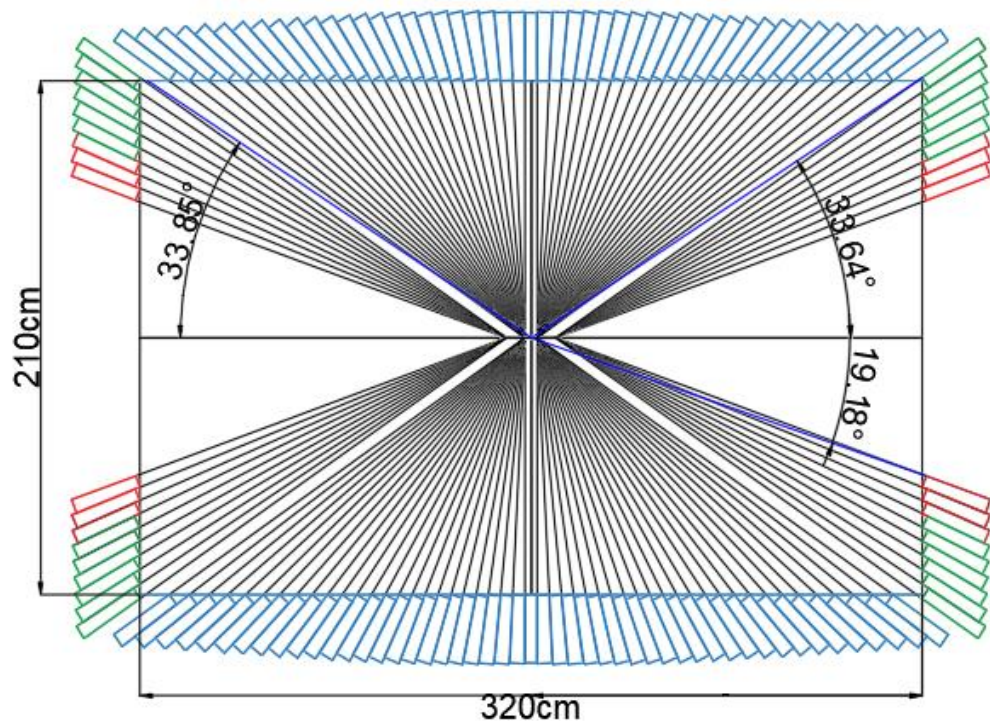
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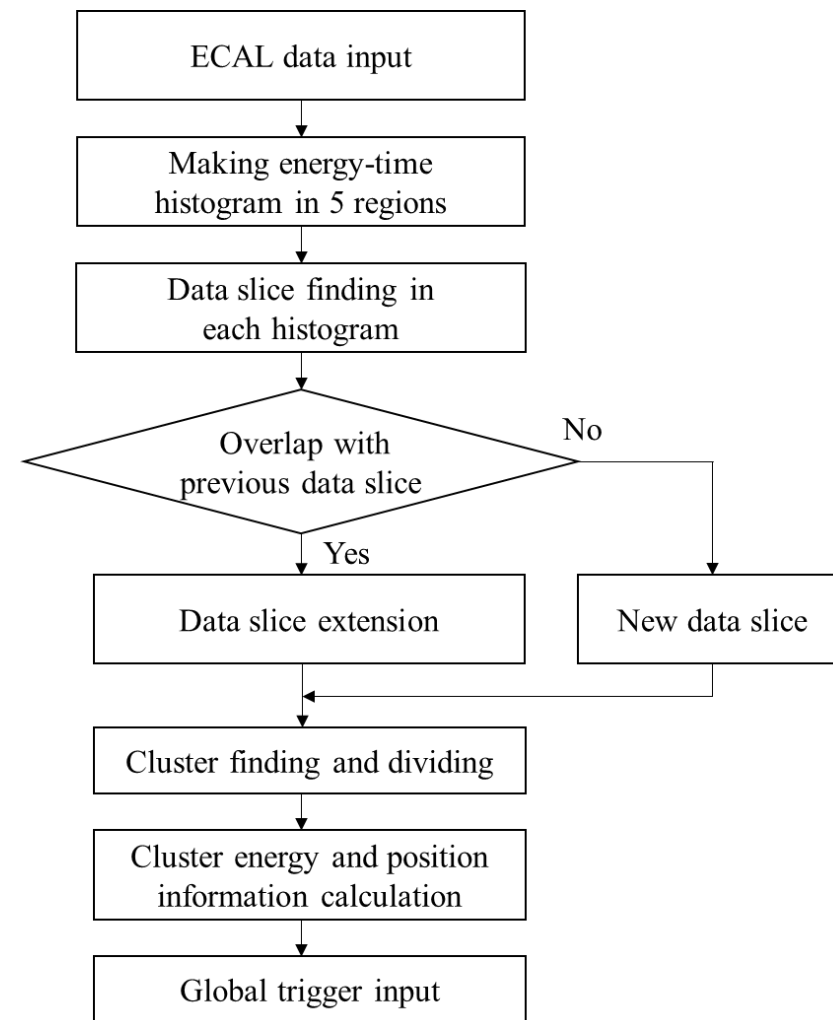
ECAL sub-trigger

ECAL structure

- Trigger cell:
 - Barrel: 4×4 or 3×4
 - Endcap: 3×5 or 4×5
- Region division:
 - Barrel
 - Inner Endcap $\times 2$
 - Outer Endcap $\times 2$

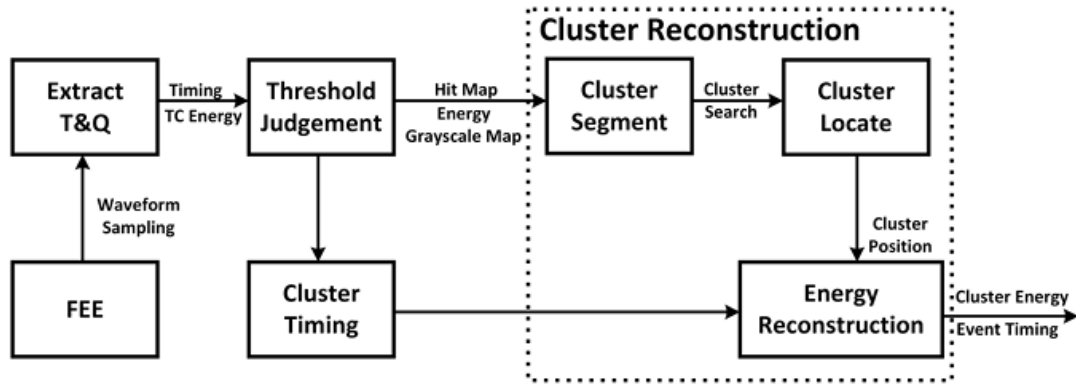


ECAL sub-trigger logic

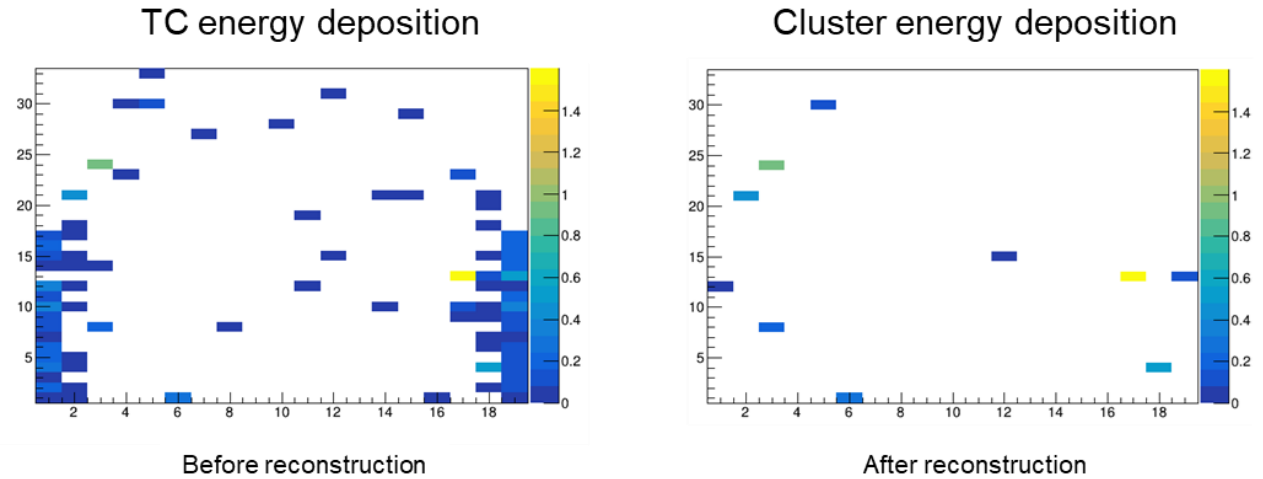


ECAL sub-trigger hardware design

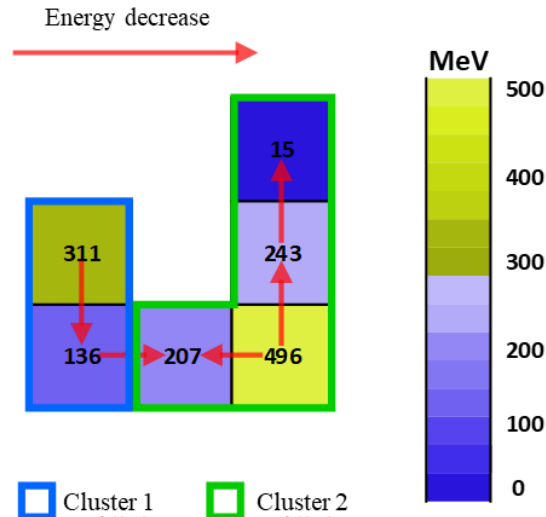
The cluster reconstruction method in ECAL sub-trigger



The result of cluster reconstruction



Cluster finding based on gradient descent method



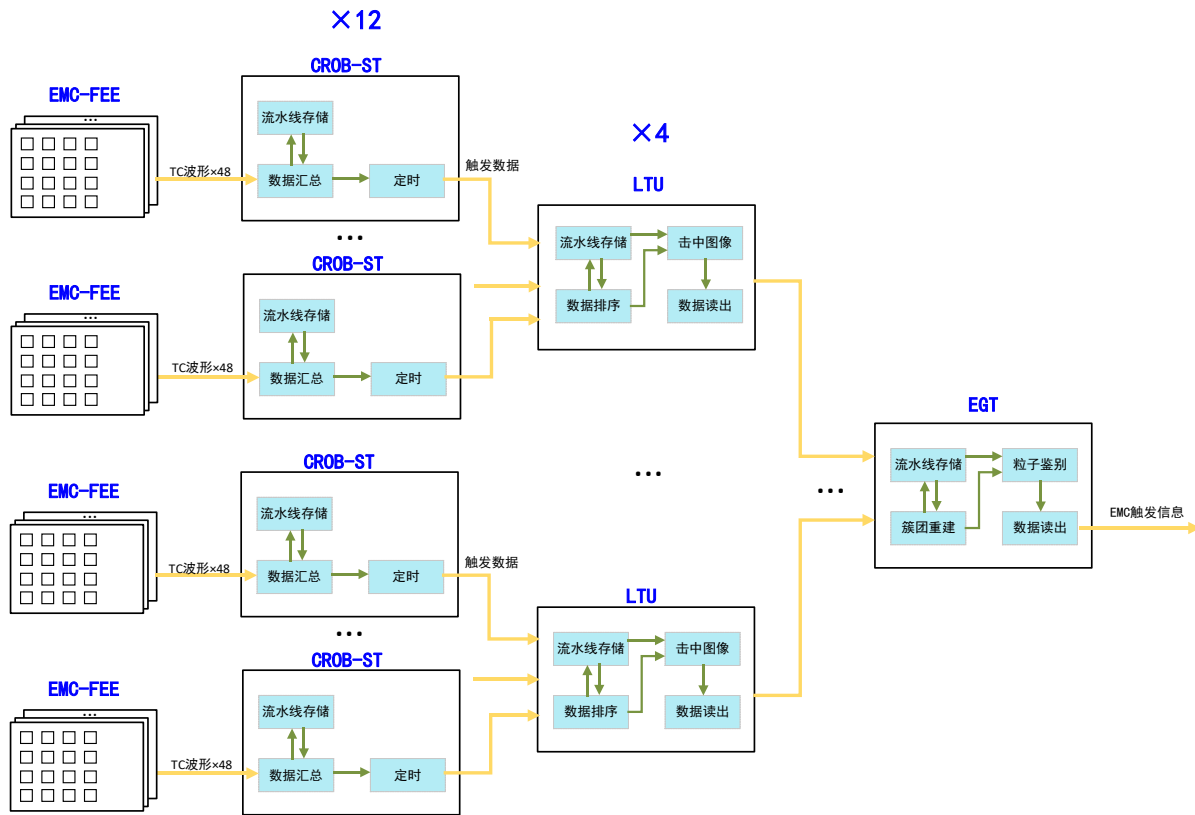
The resource evaluation (left: barrel; right: endcap)

| Resource | Utilization | Available | Utilization % |
|----------|-------------|-----------|---------------|
| LUT | 229814 | 663360 | 34.64 |
| LUTRAM | 829 | 293760 | 0.28 |
| FF | 508745 | 1326720 | 38.35 |
| BRAM | 599.50 | 2160 | 27.75 |
| IO | 45 | 728 | 6.18 |
| BUFG | 6 | 1248 | 0.48 |
| MMCM | 1 | 24 | 4.17 |

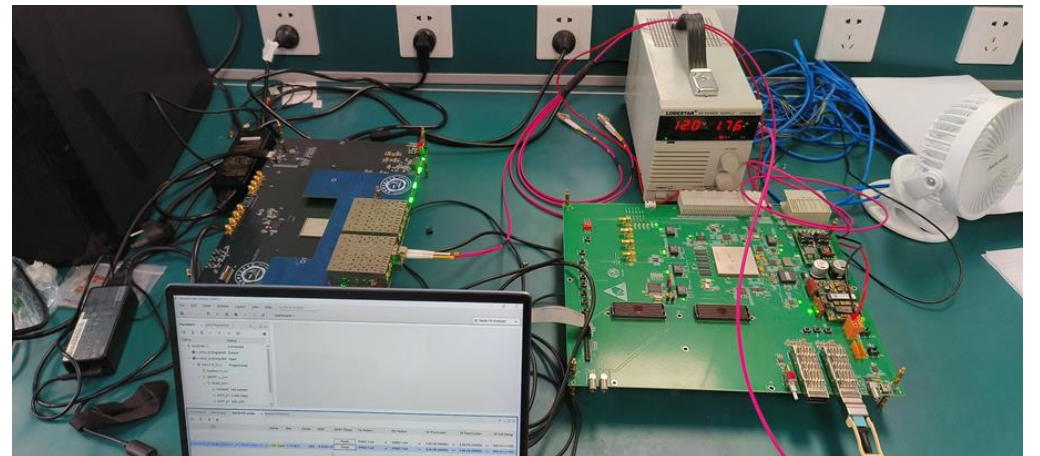
| Resource | Utilization | Available | Utilization % |
|----------|-------------|-----------|---------------|
| LUT | 83341 | 663360 | 12.56 |
| LUTRAM | 1309 | 293760 | 0.45 |
| FF | 130684 | 1326720 | 9.85 |
| BRAM | 132.50 | 2160 | 6.13 |
| IO | 45 | 728 | 6.18 |
| BUFG | 6 | 1248 | 0.48 |
| MMCM | 1 | 24 | 4.17 |

ECAL sub-trigger hardware design

□ The hardware design of ECAL sub-trigger

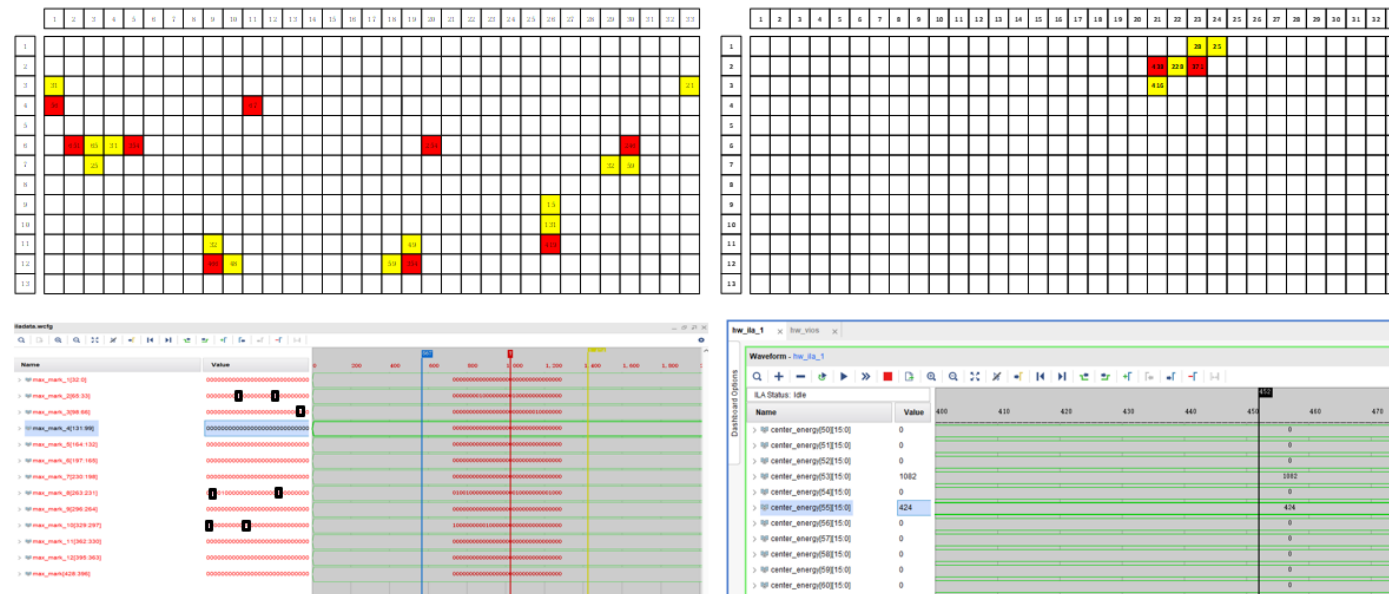
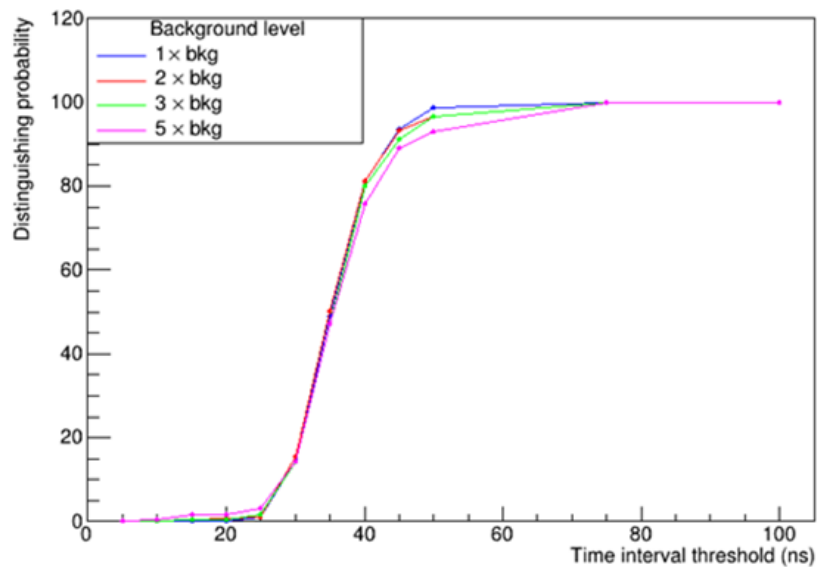
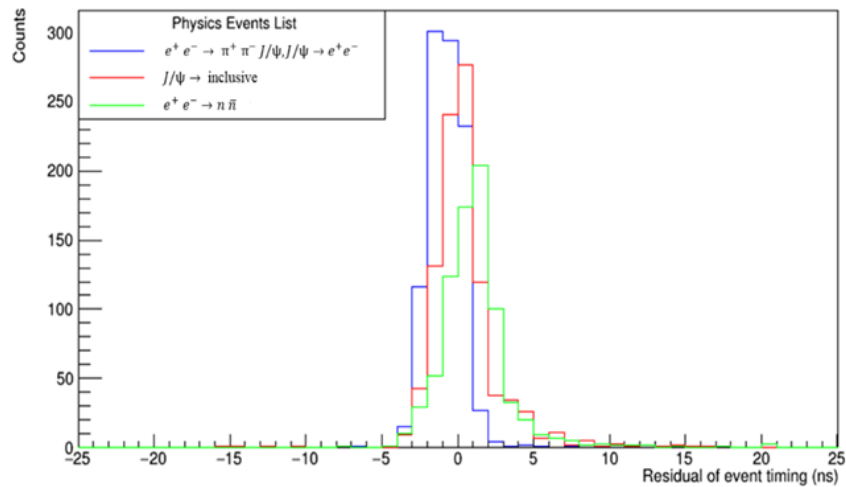


□ The board testing setup





ECAL sub-trigger performance



ECAL sub-trigger performance

- Event timing residual < 5 ns
- Distinguishing efficiency around 100% for adjacent events with 50 ns interval
- Hardware latency < 150 ns

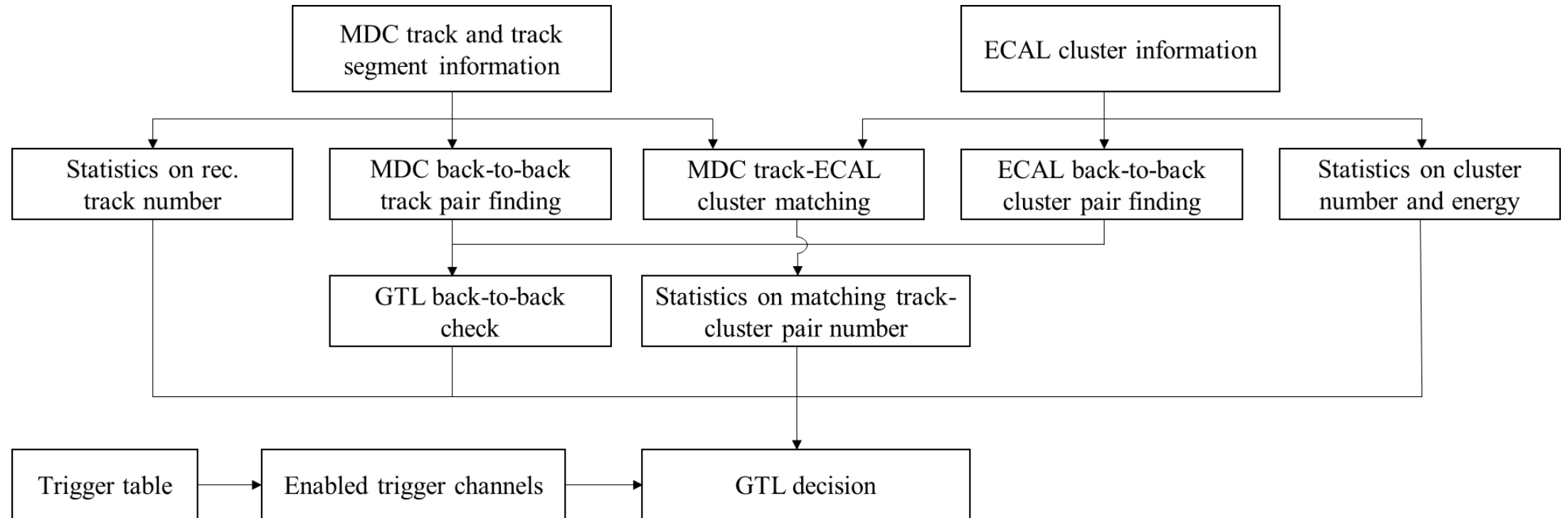


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Global trigger logic design



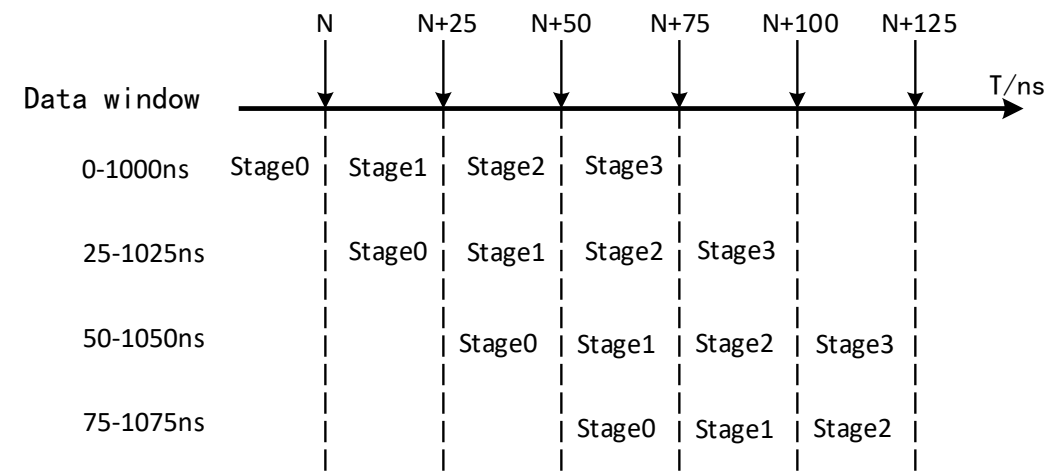
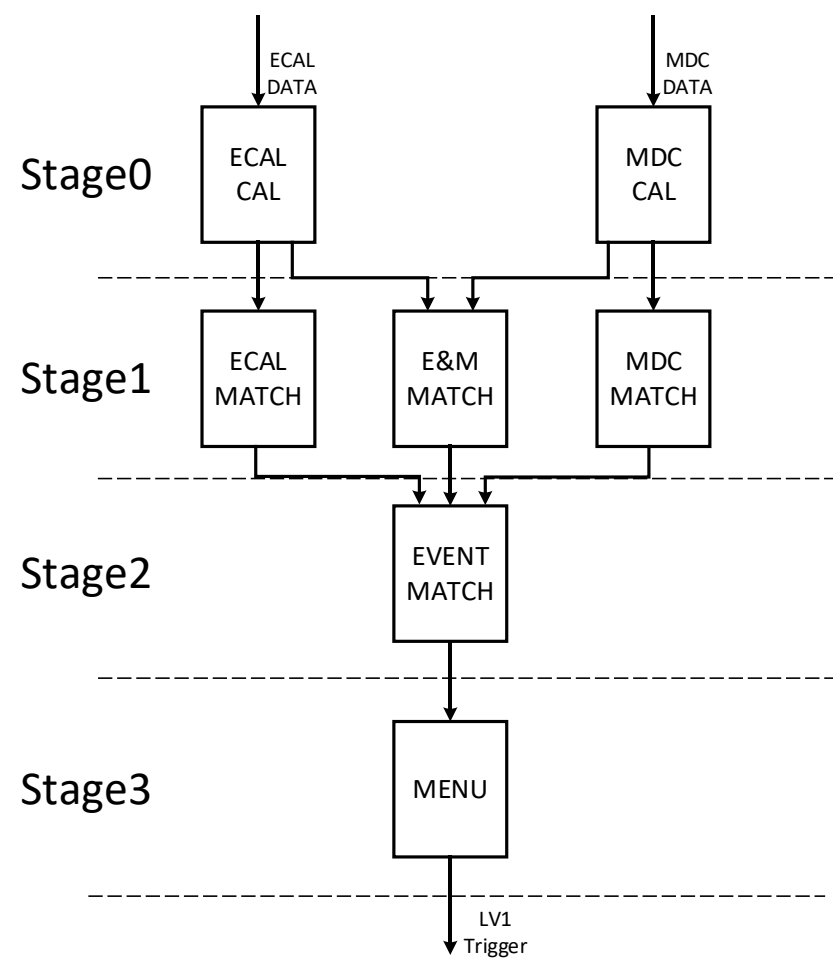
□ Function of GTL

- Match the information of the two sub-detectors
- Extract trigger criteria with the information of the two sub-detectors
- Design a trigger table considering all physics process with the input information



Global trigger logic hardware design

□ The hardware design of global trigger



| Resource | Utilization | Available | Utilization % |
|----------|-------------|-----------|---------------|
| LUT | 147979 | 663360 | 22.3 |
| FF | 366092 | 1326720 | 27.6 |
| CARRY8 | 18085 | 82920 | 21.8 |
| MUXES | 5400 | 331680 | 1.6 |

- The latency of each stage is constrained within 25 ns
- The dead time of GTL is 50 ns to 75 ns
- The resource evaluation has been completed



Global trigger logic performance

| Trigger channel | Physics Signal | Energy Point | Single particle matching ratio in the signal data slice | Signal trigger efficiency | Background trigger rate(kHz) | Signal trigger rate (kHz) |
|--|--|--------------|---|---------------------------|------------------------------|---------------------------|
| Charged channel | J/ ψ -> inclusive | 3.097GeV | 99.4% | 98.6% | 28.1 | 165.4 |
| | e ⁺ e ⁻ -> $\pi^+\pi^-$ J/ ψ J/ ψ -> e ⁺ e ⁻ | 4.26GeV | 95.0% | 99.8% | | 2.97×10 ⁻⁴ |
| | e ⁺ e ⁻ -> $\pi^+\pi^-$ J/ ψ J/ ψ -> $\mu^+\mu^-$ | 4.26GeV | 94.6% | 99.8% | | 2.98×10 ⁻⁴ |
| | e ⁺ e ⁻ -> $\tau^+\tau^-$ | 4.26GeV | 99.3% | 98.4% | | 1.72×10 ⁻¹ |
| | J/ ψ -> $\Lambda\bar{\Lambda}$ | 3.097GeV | 90.8% | 98.6% | | 3.13×10 ⁻¹ |
| | J/ ψ -> $\Xi\bar{\Xi}$ | 3.097GeV | 92.4% | 97.8% | | 1.59×10 ⁻¹ |
| | e ⁺ e ⁻ -> K ⁺ K ⁻ J/ ψ J/ ψ -> l ⁺ l ⁻ | 4.682GeV | 98.0% | 99.5% | | 1.78×10 ⁻⁵ |
| | e ⁺ e ⁻ -> D ₀ \bar{D}_0 | 3.773GeV | 97.3% | 99.9% | | 2.08×10 ⁻¹ |
| | e ⁺ e ⁻ -> D ⁺ D ⁻ | 3.773GeV | 100% | 99.8% | | 1.64×10 ⁻¹ |
| e ⁺ e ⁻ -> D _s ⁺ D _s ⁻ | 4.04GeV | 99.8% | 99.9% | 3.37×10 ⁻⁴ | | |
| Neutral channel | J/ ψ -> γ invisible | 3.097GeV | - | 98.8% | 1.16×10 ⁻⁴ | |
| | e ⁺ e ⁻ -> n \bar{n} | 3.097GeV | - | 97.2% | 3.41×10 ⁻¹ | |
| | e ⁺ e ⁻ -> γ n \bar{n} | 3.097GeV | - | 98.9% | 1.28×10 ⁻² | |
| | e ⁺ e ⁻ -> γ n \bar{n} (ISR) | 3.713GeV | - | 98.4% | 2.47×10 ⁻² | |
| Luminosity monitor channel | Digamma | 4.26GeV | - | 98.7% | 1.78 | |
| | Bhabha scattering | 4.26GeV | 97.5% | 99.8% | 36.6 | |



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Summary

□ The demand and tested performance of L1 trigger system

- High trigger efficiency ($\sim 99\%$)
 - Most typical charged trigger channel $> 99\%$
 - Most typical neutral trigger channel $> 97\%$
- Low background trigger rate (< 50 kHz)
 - The average background trigger rate is under 30 kHz
- Low latency (< 5 μs)
 - ECAL hardware latency $< 150\text{ns}$
 - MDC hardware latency is 340 ns (2D) + 210 ns (timing) + 125 ns (3D) = 675 ns
 - GTL hardware latency is around $600\sim 1000$ ns
- Good adjacent event distinguishing ability ($\Delta T < 100$ ns)
 - ECAL timing can distinguish data slice with time interval more than 50 ns

Thanks~