Design and performance of MAPS prototypes for the STCF inner tracker

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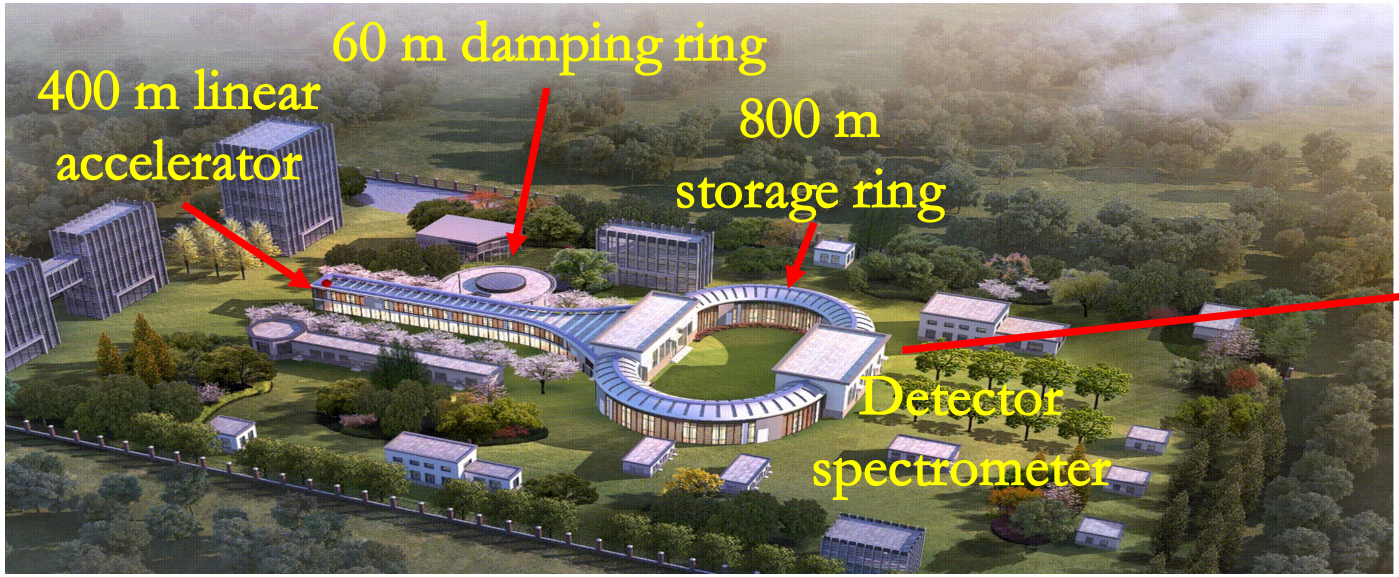
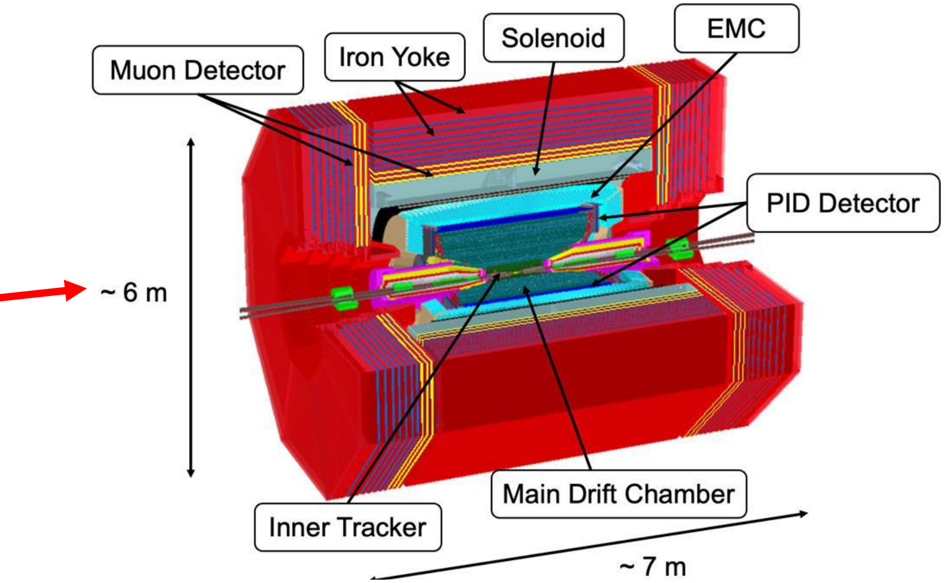
Super Tau-Charm Facility

❖ **STCF: next generation e^+e^- collider in China**

- Center-of-mass energy: **2-7 GeV**
- Peak luminosity: **> 0.5×10^{35} $cm^{-2}s^{-1}$ at 4 GeV**
- Collision data: more than **1 ab^{-1}/y**
- With potential to further **increase luminosity** and **beam polarization**





Detector Considerations for ITK

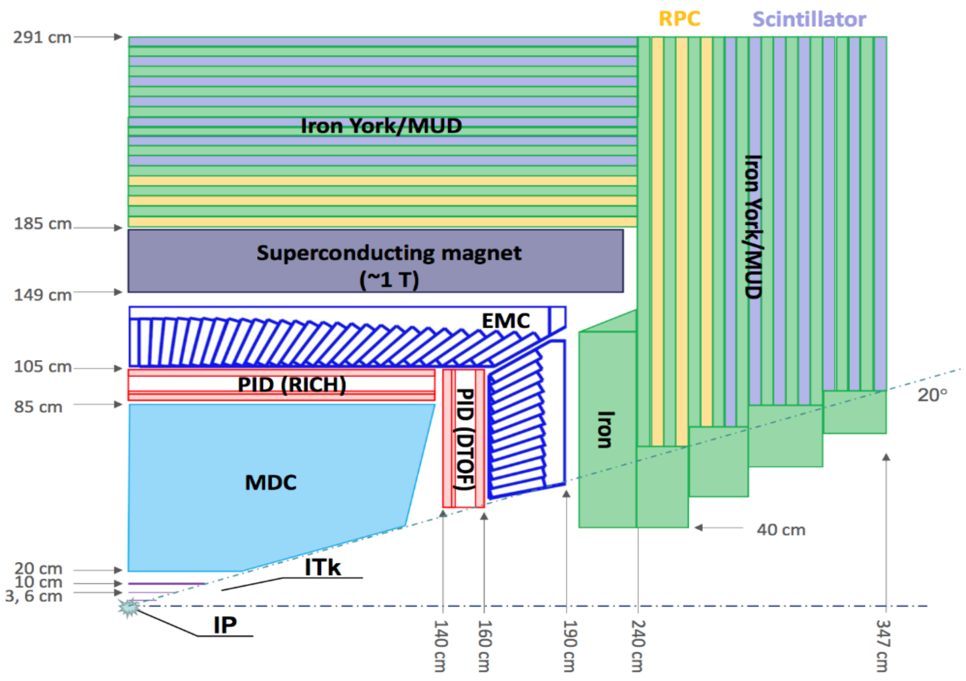
❖ Physics requirements

Solid angle coverage: 93%·4π

(polar angle: 20°~160°)

Inner tracker(ITK)
- ~ 0.3%X_0/layer
- σ_{xy}<100 μm

Main drift chamber(MDC)
- σ_{xy} < 130 μm
- σ_p/p~ 0.5% @ 1GeV
- dE/dx ~ 6%



Front. Phys. 19, 14701 (2024)

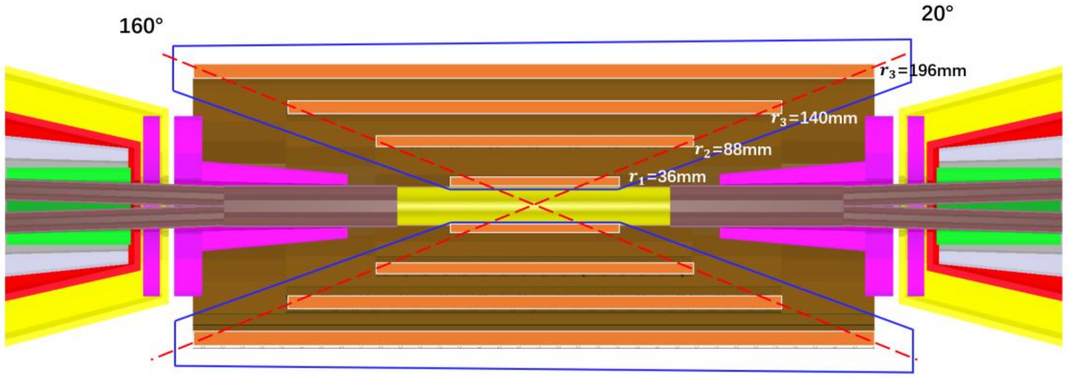
Process	Physics Interest	Optimized Sub-detector	Requirements
$\tau \to K_s \pi \nu_\tau$, $J/\psi \to \Lambda\bar{\Lambda}$, $D_{(s)}$ tag	CPV in τ sector, CPV in hyperon sector, Charm physics	Tracker	acceptance: 93% of 4π; trk. effi.: $> 99\%$ at $p_T > 0.3$ GeV/c; $> 90\%$ at $p_T = 0.1$ GeV/c; $\sigma_p/p = 0.5\%$, $\sigma_{\gamma\phi} = 130\ \mu$m at 1 GeV/c

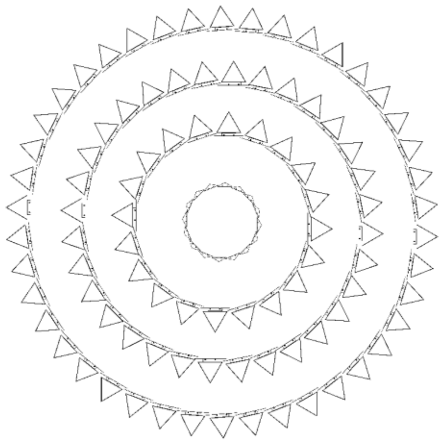
❖ Tracking challenges at low p_T
- Momentum resolution: Multiple Coulomb scattering
- Track reconstruction efficiency

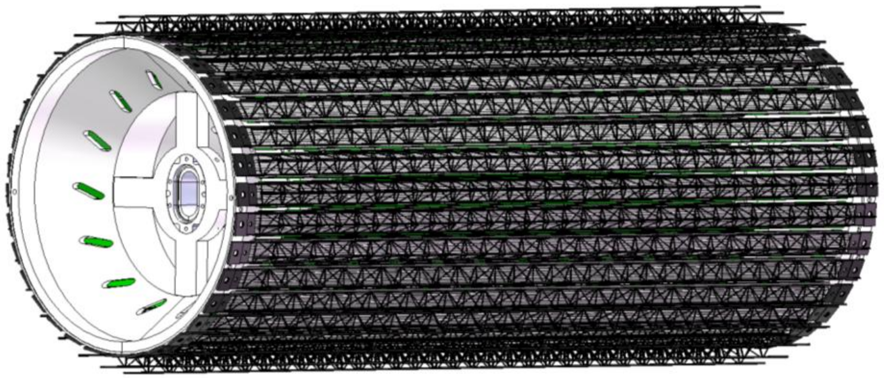
❖ Low material budget is essential to satisfy the physics requirements

Conceptual Design

- ❖ MAPS is one of the options for the Inner Tracker (ITKM)
  - Another option is the MPGD based Inner Tracker (ITKW)
- ❖ Four layers of silicon pixel detectors, with radii of 36 mm, 88 mm, 140 mm, and 196 mm
  - Beam pipe radium: 30 mm
- ❖ Total area: 2.5 m^2
- ❖ 6222 chips with single chip size of ~ 2 cm × 2 cm



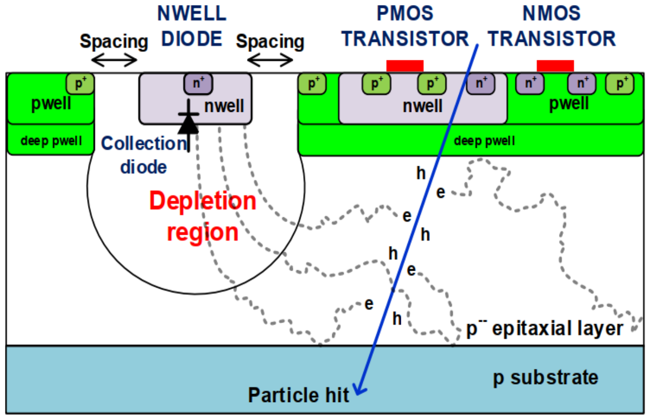




Design Targets

❖ Requirements on the MAPS based Inner Tracker

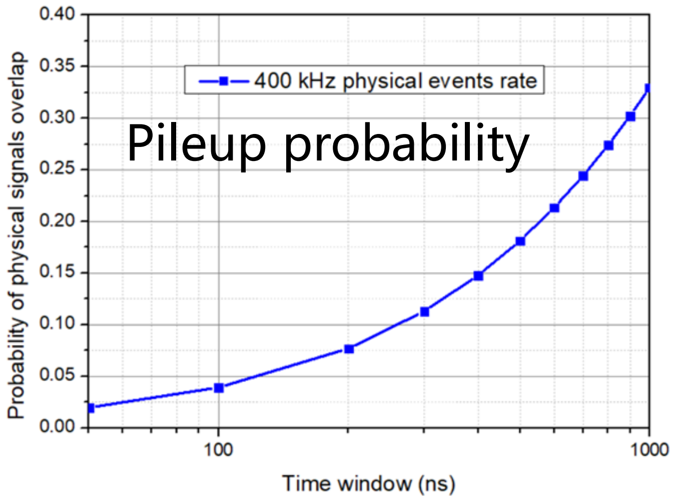
	Requirements
Hit position resolution	$<100\,\mu m$
Hit time resolution	$\sim 20\,ns$
Power consumption	$\sim 50\,mW/cm^2$
Material budget	$\sim 0.3\%\ X_0$ per layer
Hit rate	$>1\,MHz/cm^2$
TID	$>1.0\,Mrad/year$
NIEL	$> 1.0 \times 10^{11}\ 1\,MeV\,n_{eq}/cm^2/year$



MAPS with small fill-factor is preferred

High event rate at STCF

Physics Process	Cross-section (nb)	Rate (Hz)
$\sqrt{s} = 3.097$ GeV, $\mathcal{L} = 0.75 \times 10^{35}$ cm^{-2}s^{-1}, $\Delta E = 0.848$ MeV		
J/ψ	4500	337500
$\to e^+e^-$	270	20000
$\to \mu^+\mu^-$	270	20000
Bhabha ($\theta \in (20°, 160°)$)	734	55000
$\gamma\gamma$ ($\theta \in (20°, 160°)$)	36	2700
$\mu^+\mu^-$	11.4	900
Hadronic from continuum	25.6	2000
2γ process ($\theta \in (20°, 160°)$, $E > 0.1$ GeV	~23.3	1740
Total	~5300	~400000

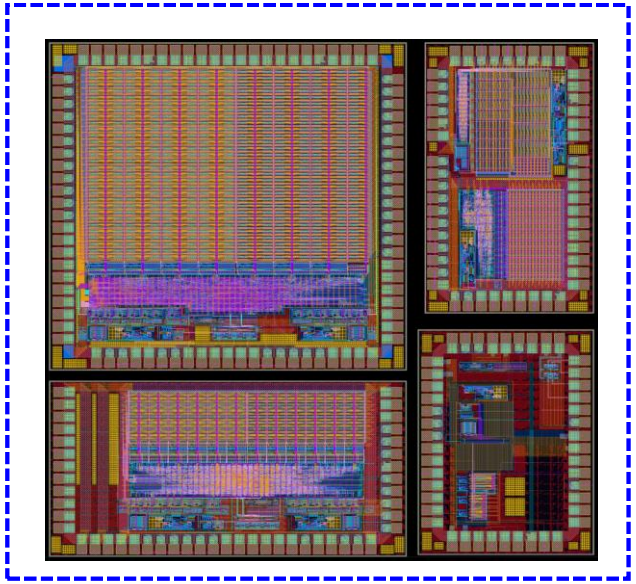


MAPS Prototypes

180 nm process

- Low-resistivity substrate + high-resistivity EPI
- Mature process in HEP

CharTPix_180

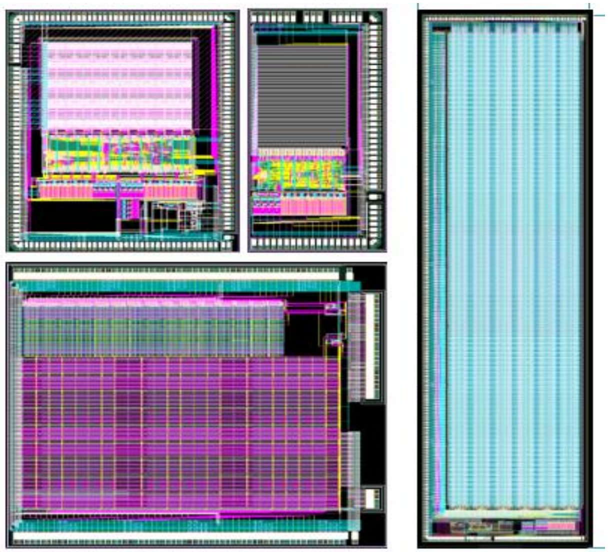


Design started in 2021, finished in 2023
Submitted in Mar. 2024
Chips returned in Dec. 2024

130 nm process

- High-resistivity substrate, no EPI
- Domestic process

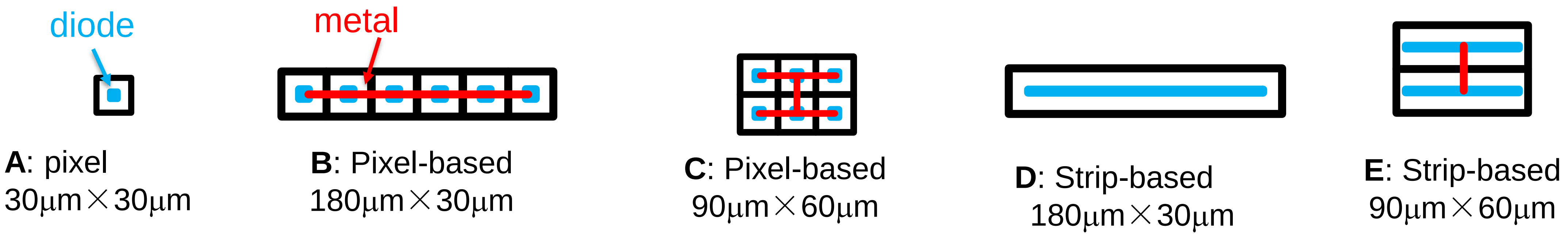
CharTPix_130



Design started in 2023
Submitted in Sep. 2024
Chips returned in Mar. 2025

Sensor Design

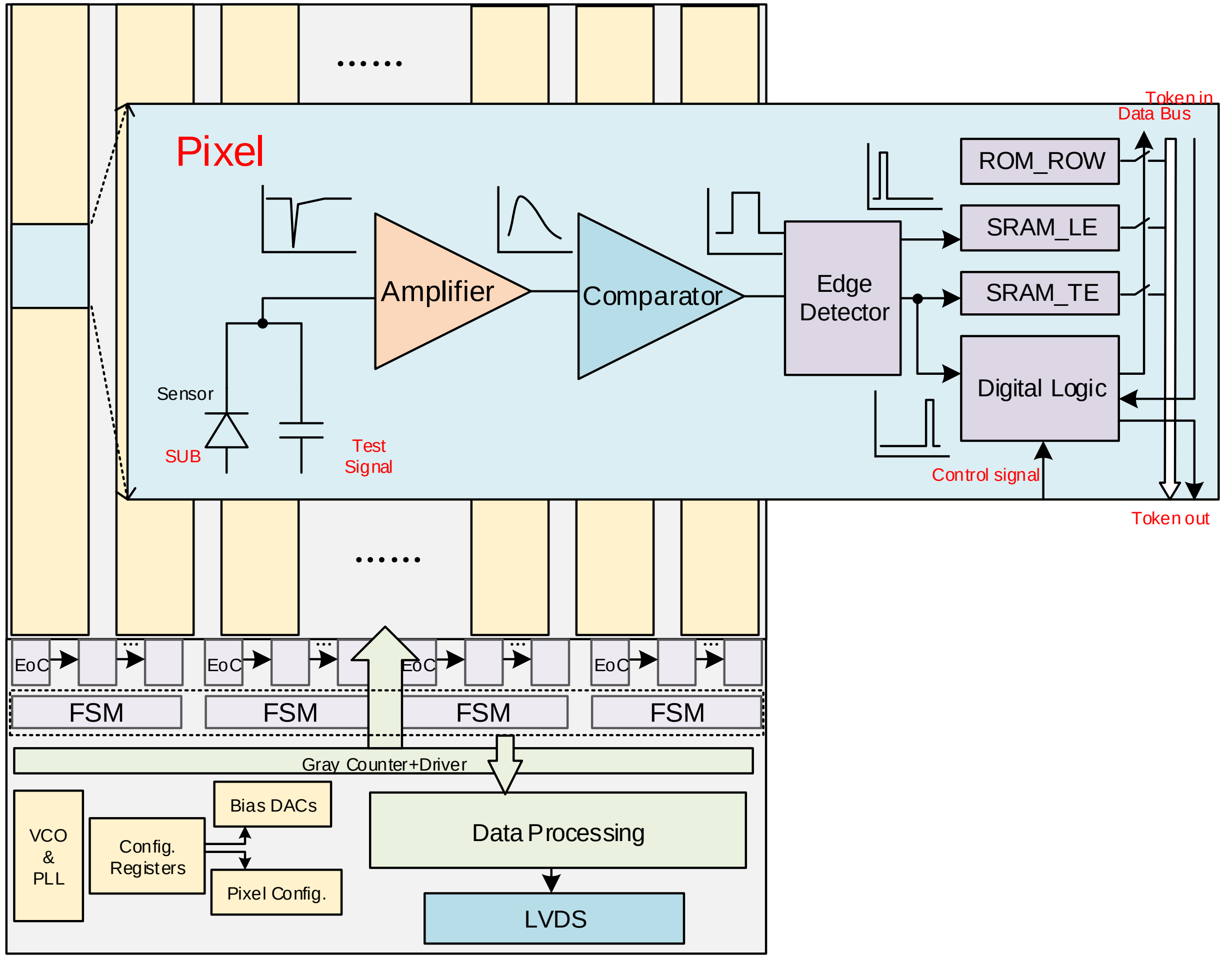
- Pixel size considerations
  - Higher priority on the power consumption than the spatial resolution → larger pixel size to reduce the power consumption density
  - The ALPIDE sensor is already optimized and proven experimentally → keep the sensor geometry as close to ALPIDE as possible
    - Pixel-based: analog connected small pixels ($1 \times 6 \rightarrow 1, 2 \times 3 \rightarrow 1$) using metal lines
    - Strip-based: extended diode size in one direction
    - 3rd option: digital connected small pixels



Metal line connected
✓ small input capacitance

Nwell (active) connected
✓ faster charge collection

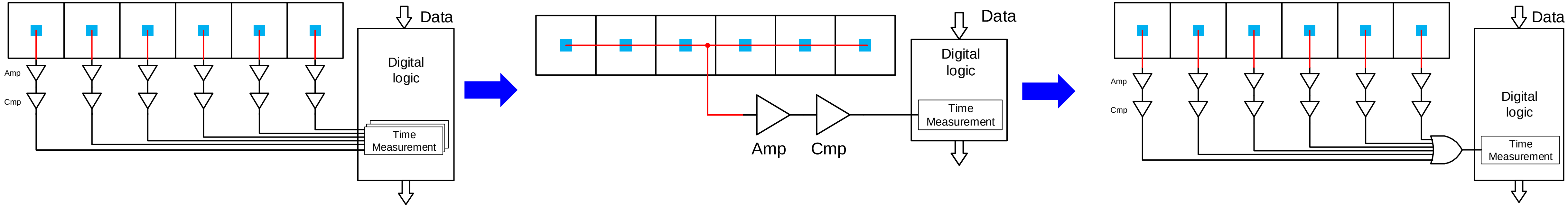
Readout Architecture



- ❖ In-pixel circuit
  - Analog amplifier, comparator
  - Coarse time latches
- ❖ Digital readout
  - Column level priority logic
    - Token ring priority coding
    - 8-bit ToA, 8-bit ToT@20 MHz
  - Data processing module
- ❖ Power consumption estimation for 2cm×2cm chip
  - Strip-based：55.7 mW/cm^2
  - Pixel-based：46.2 mW/cm^2

Timing Improving Consideration

- ❖ Precise timing provides more potential
- ❖ Promising readout architecture： digital “OR” for multiple small pixel



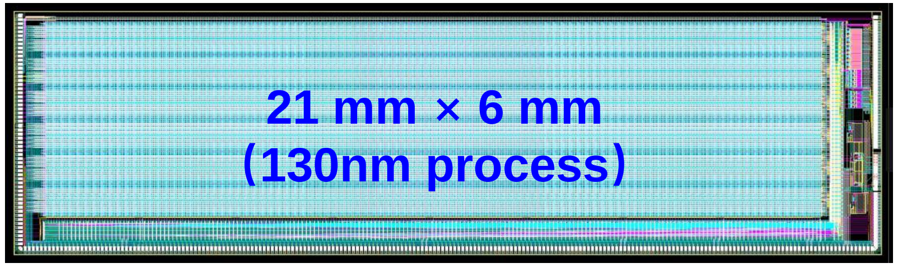
✓ Small collection diode
→ Good time performance
→ Good spatial resolution
✓ Multiple readout channels
→ High digital power

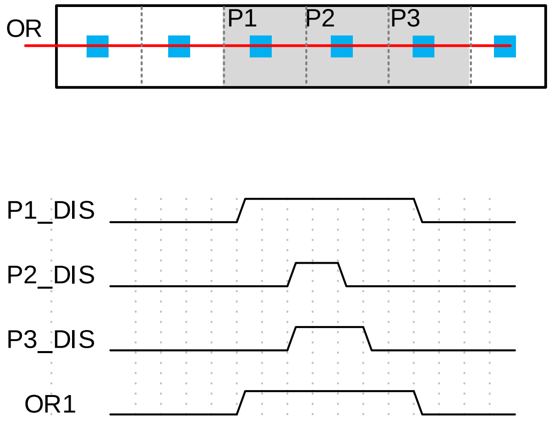
✓ Large collection diode
→ Low time performance
→ Low spatial resolution
✓ Fewer readout channels
→ Low digital power

✓ Small collection diode
→ Good time performance
→ Good spatial resolution
✓ Fewer readout channels
→ Low digital power

Super Pixel Design

- ❖ Combining non-adjacent pixels: avoid ToT loss
- ❖ Super pixel with 6×12 pixel array
  - – 6 sets of digital readout logic
  - – When cluster size < 3X4, no ToT loss occurs

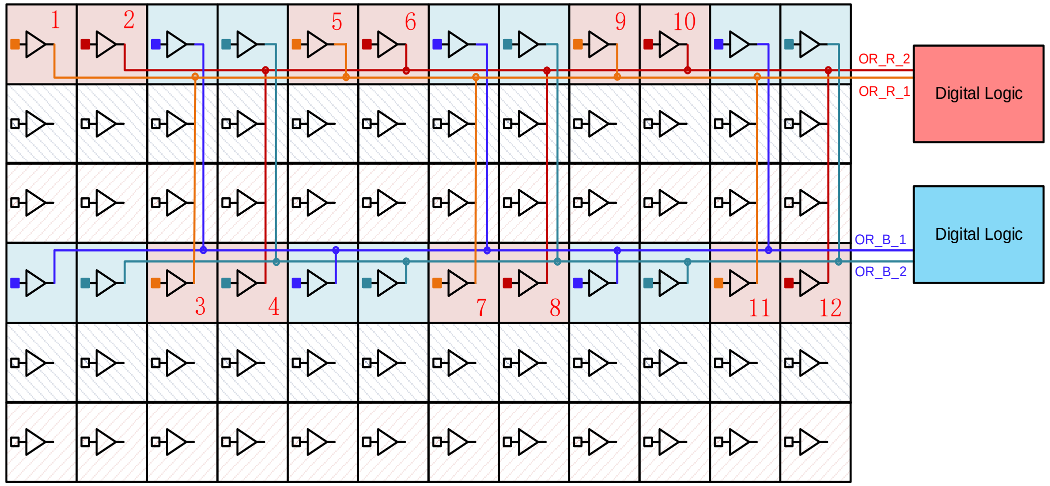




Combining adjacent pixels

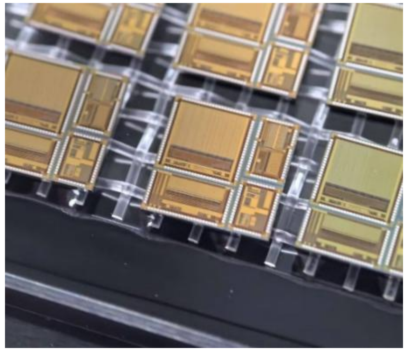
→ ToT loss

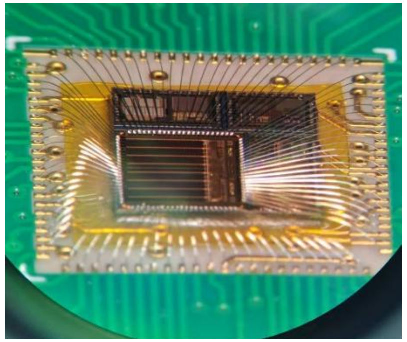
Additional 3-bit for group address

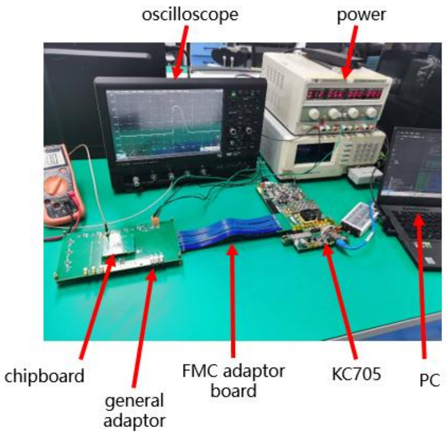


- Pixel Pitch: 33 μm×33 μm
- Pixel Array: 576 rows × 144 columns
- Simulated Threshold: ~ 150 e^-
- TOA+TOT measurement
  - ◇ 2 ns bin size: 500 MHz VCO
- Simulated Power Consumption: < 50 mW/cm^2

CharTPix_180 – Sensor Characterization

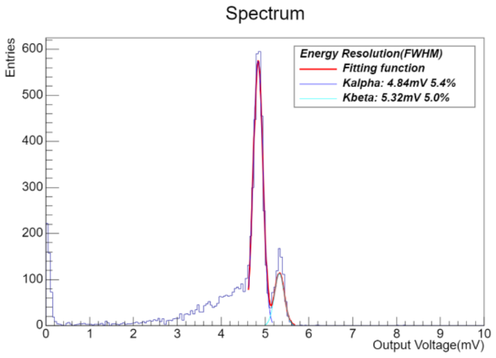


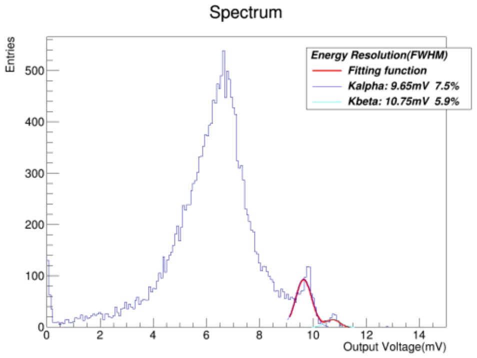


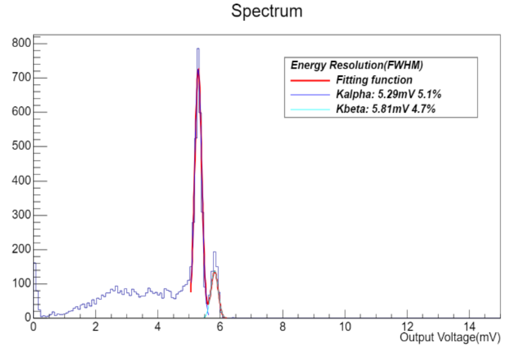


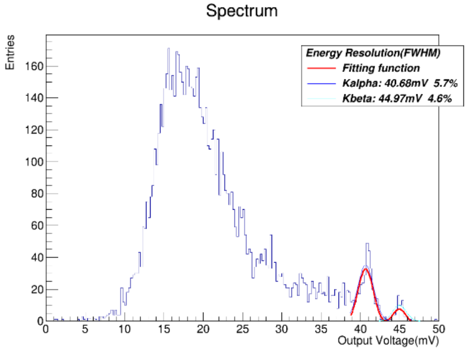
- 3T sensors ^{55}Fe test

Energy spectrum

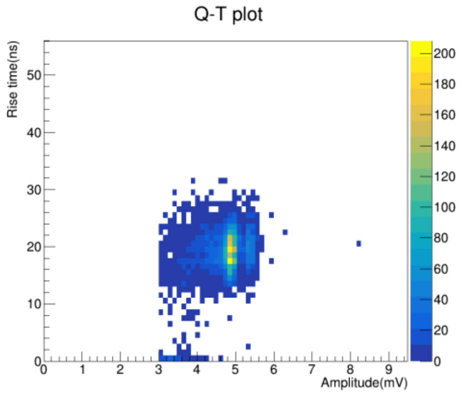


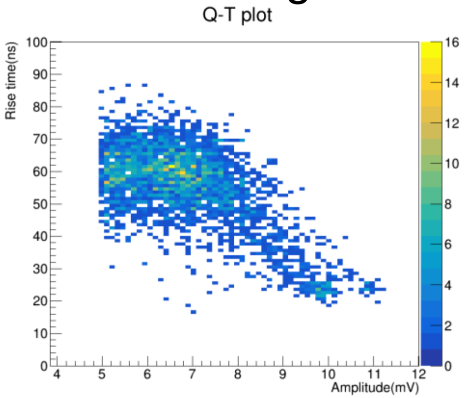


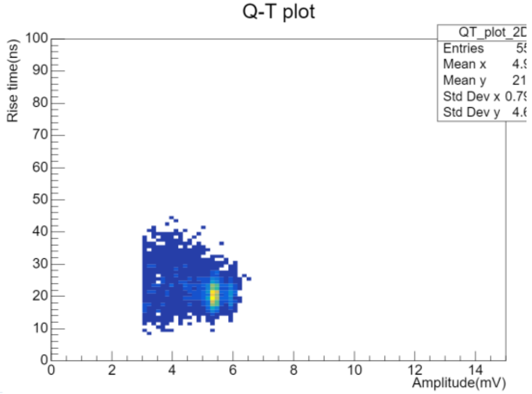


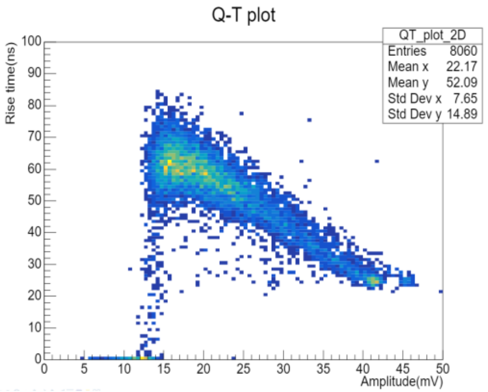


Signal rise time



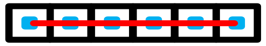




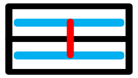


1×6 strip-based

1×6 pixel-based



2×3 strip-based

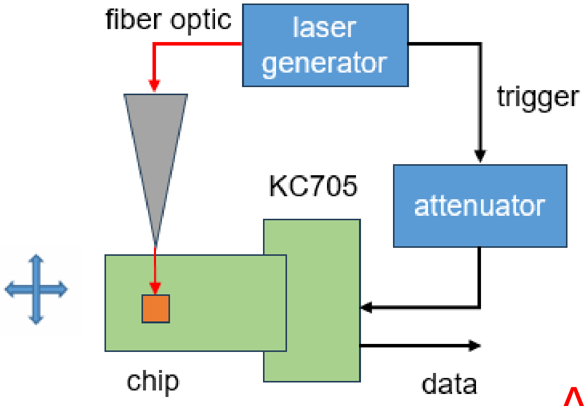


1×1 ALPIDE-like

Strip-based has much better charge collection efficiency

CharTPix_180 – Laser Test

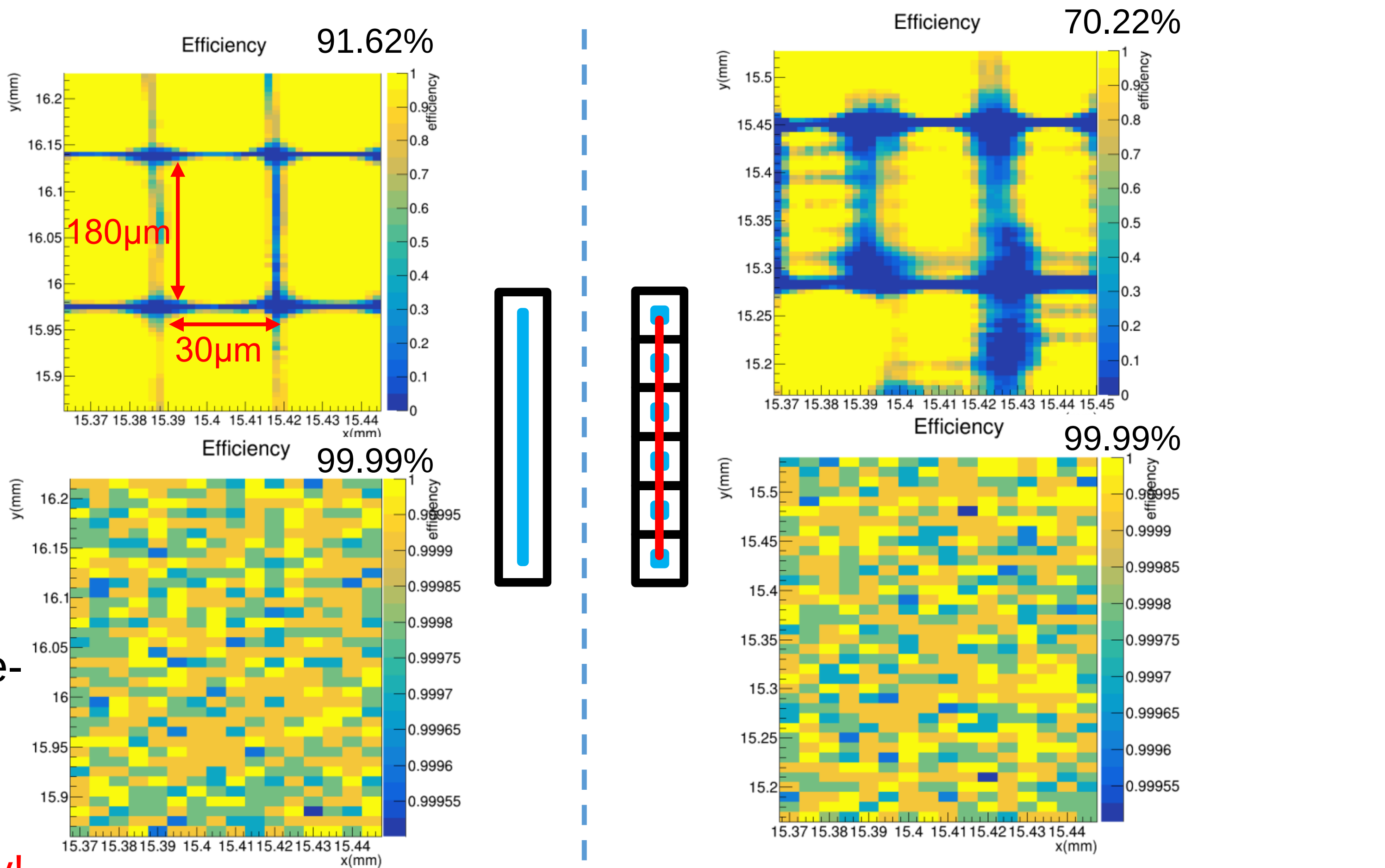
- Laser test to characterize the charge collection profile



With laser intensity equivalent to 600e- (~0.375 MIP)

With laser intensity equivalent to 1600e- (~1 MIP)

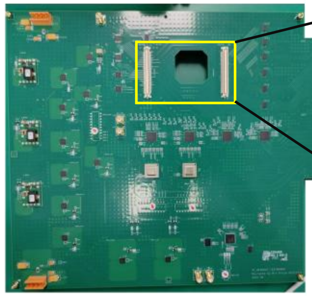
Almost 100% efficiency!



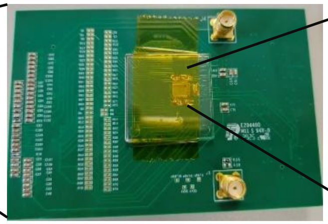
CharTPix_130 – Sensor Characterization

3T sensors: 6×6 pixel test structure with parallel analog readout of all pixels

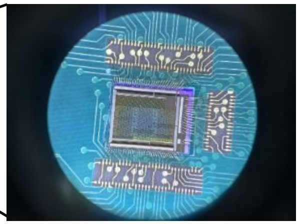
Using a 16ch-ADC readout system



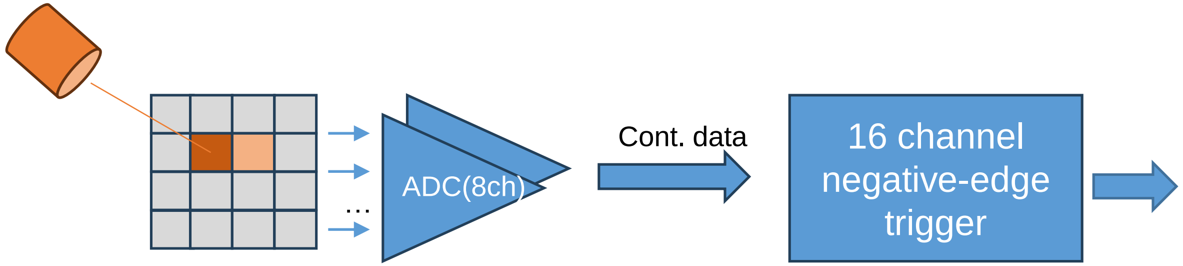
1st Ver. Mother board

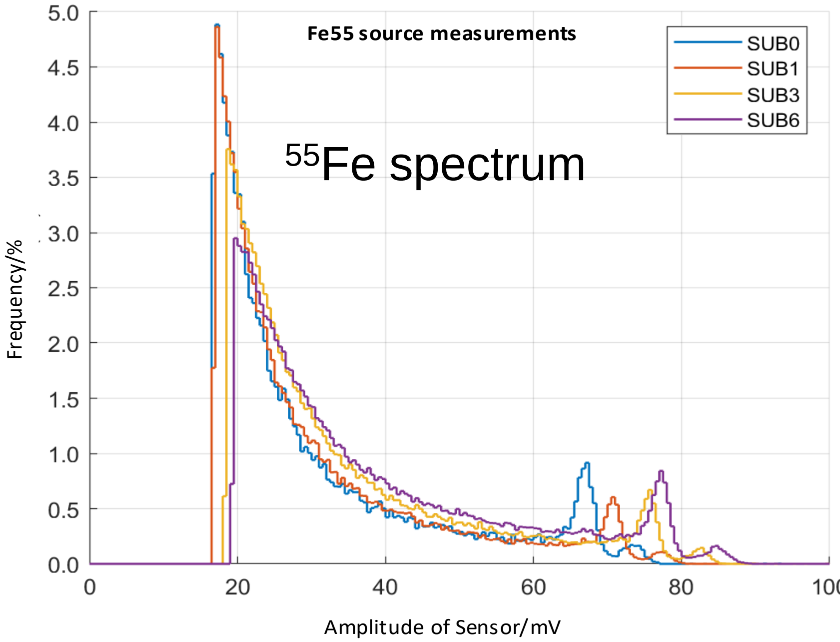


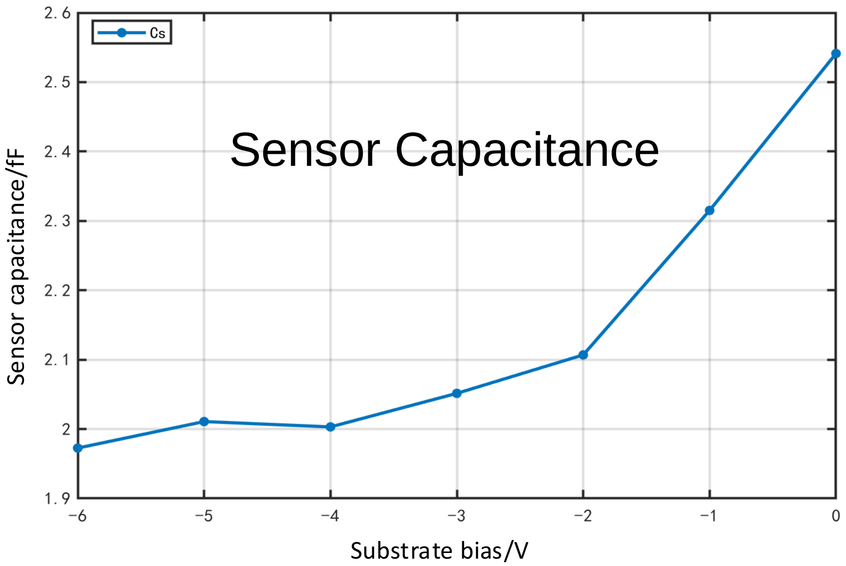
Chip carrier board



Wire bonding



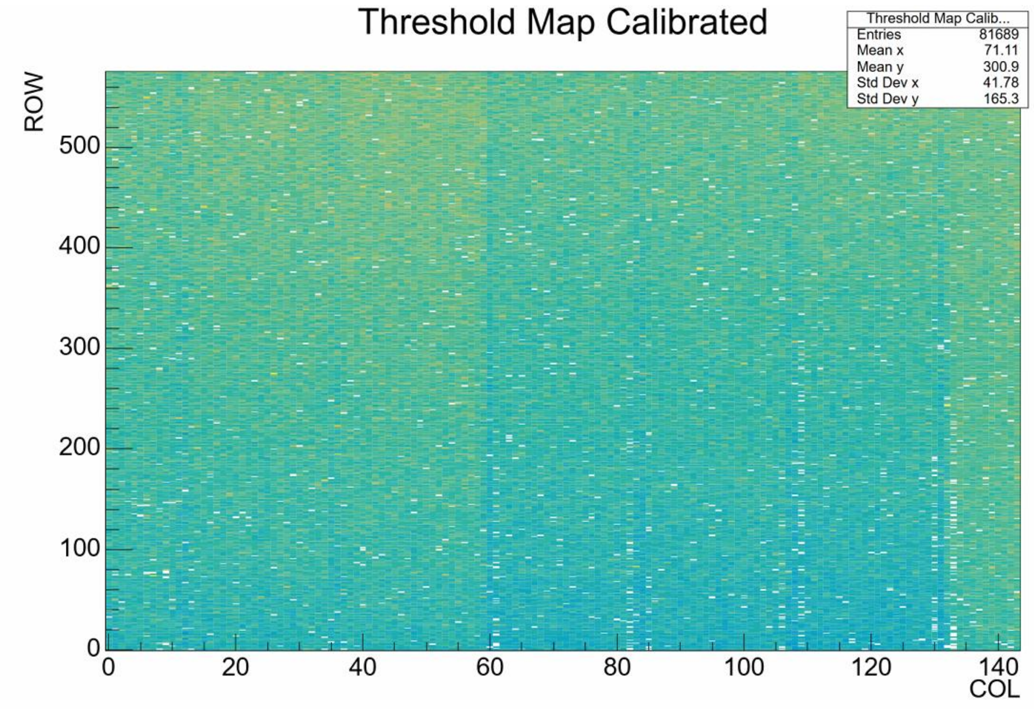


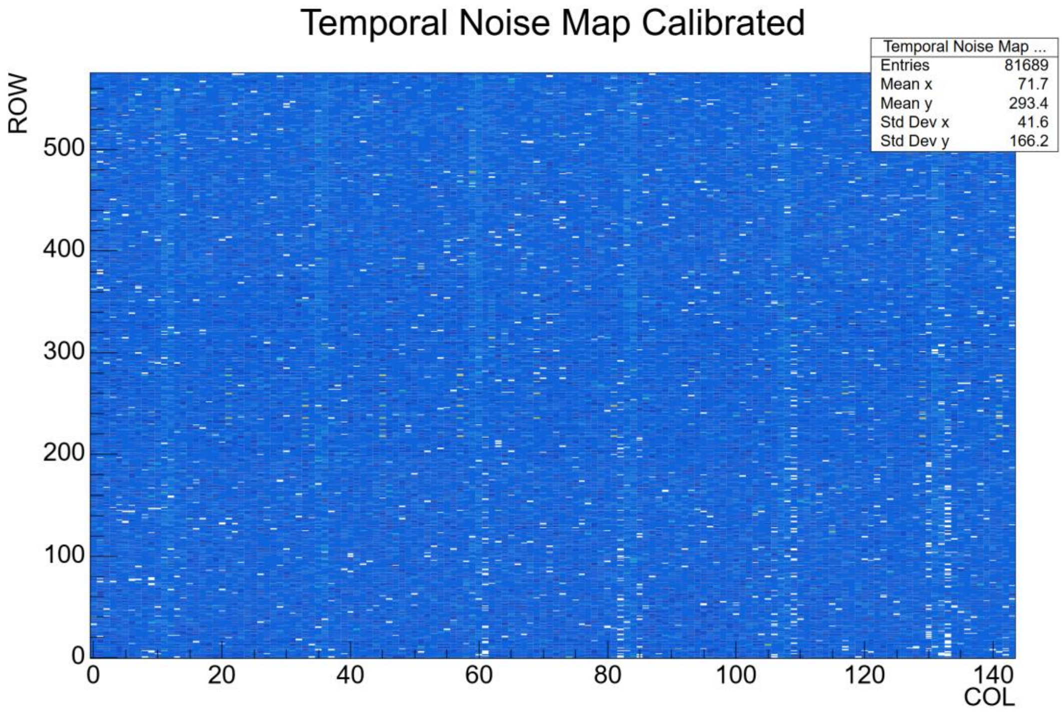


CharTPix_130 – Electronics Test

CharTPix_130 MAPS with super-pixel readout

- Threshold: 252.0 Mismatch: 31.0
- TN: 7.1 TN sigma: 2.3(@SUB = -4 V)

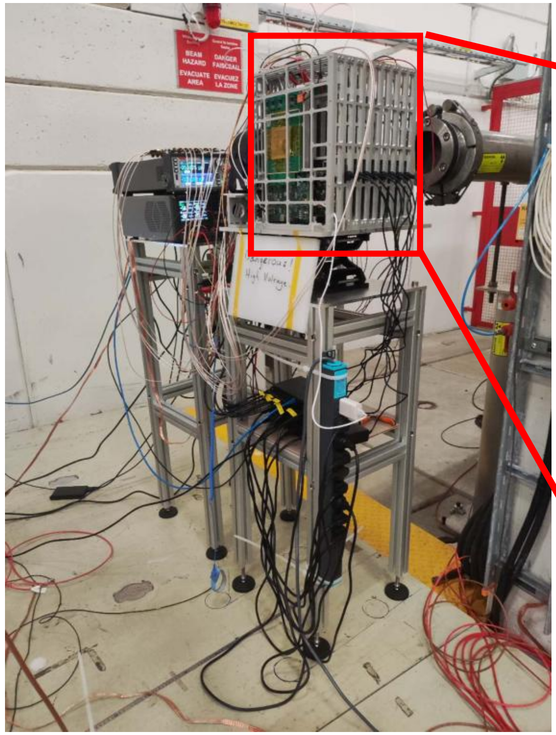


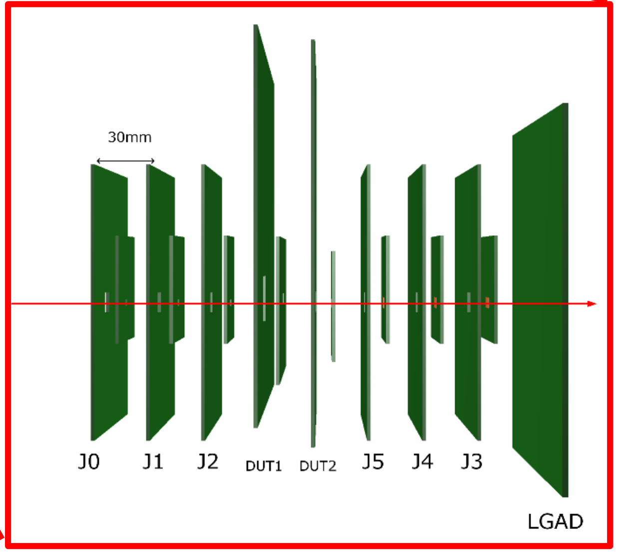


Beam Test

❖ Telescope System

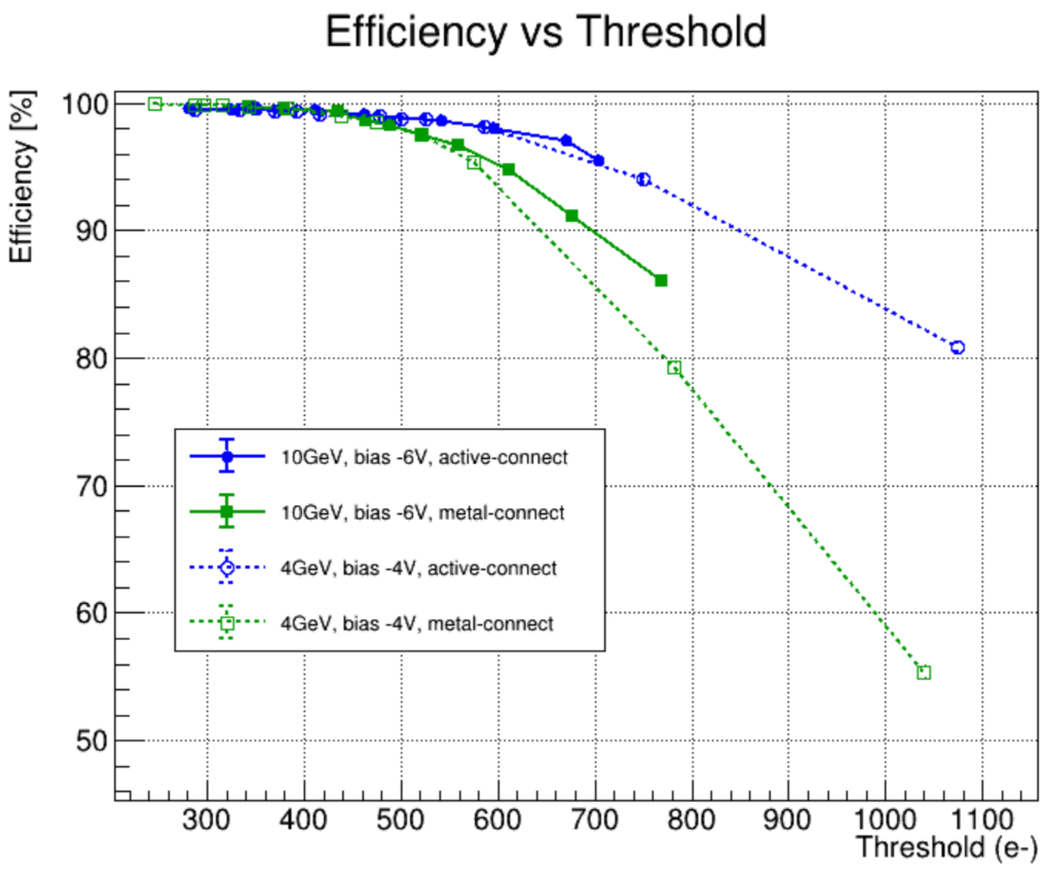
- Six layers of Jadepix-3 chips serving as reference tracking detectors (J0-J5)
- One layer of LGAD as the timing reference detector
- Two DUT layers: CharTPix_180 and CharTPix_130

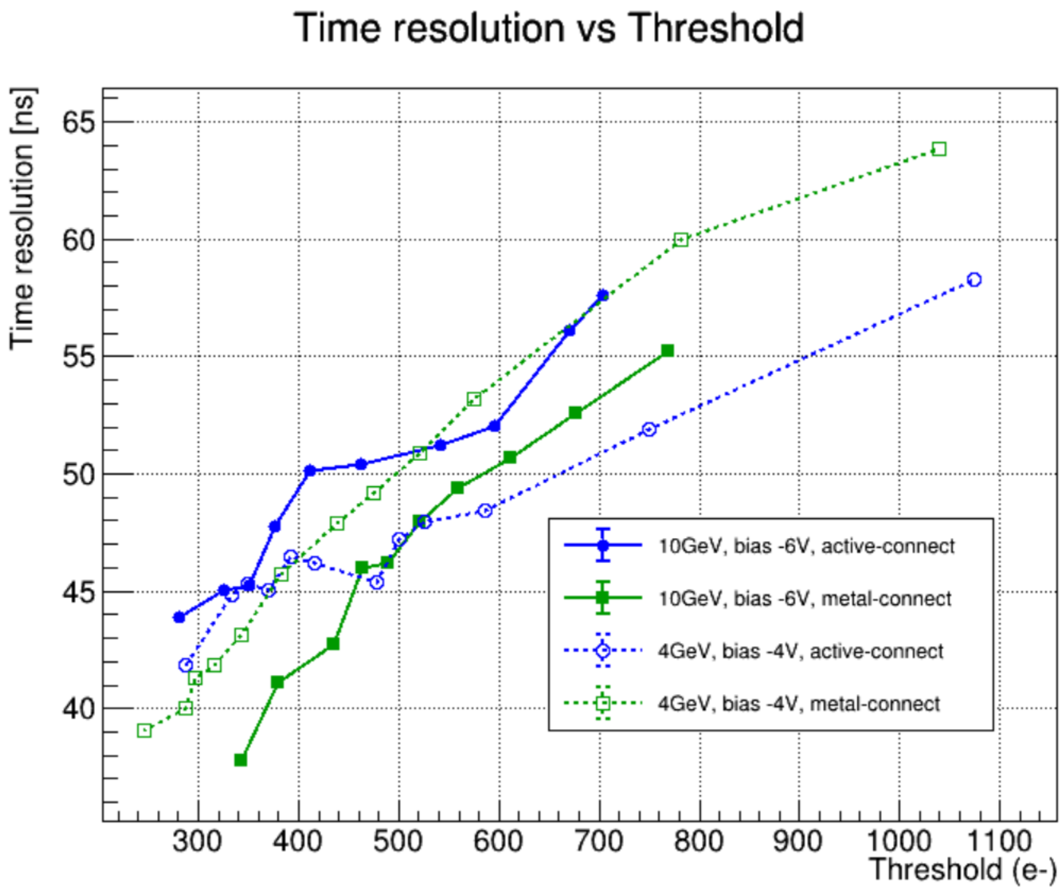




✓ Particle Species
- 4 GeV hadron
- 10 GeV hadron
- 10 GeV muon
- 1 GeV electron

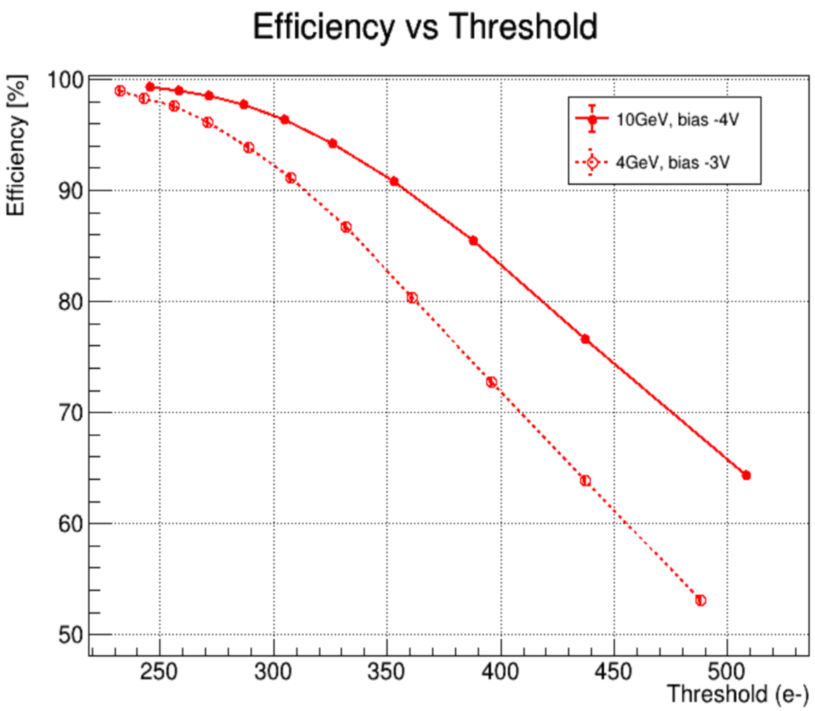
Test Result – CharTPix_180

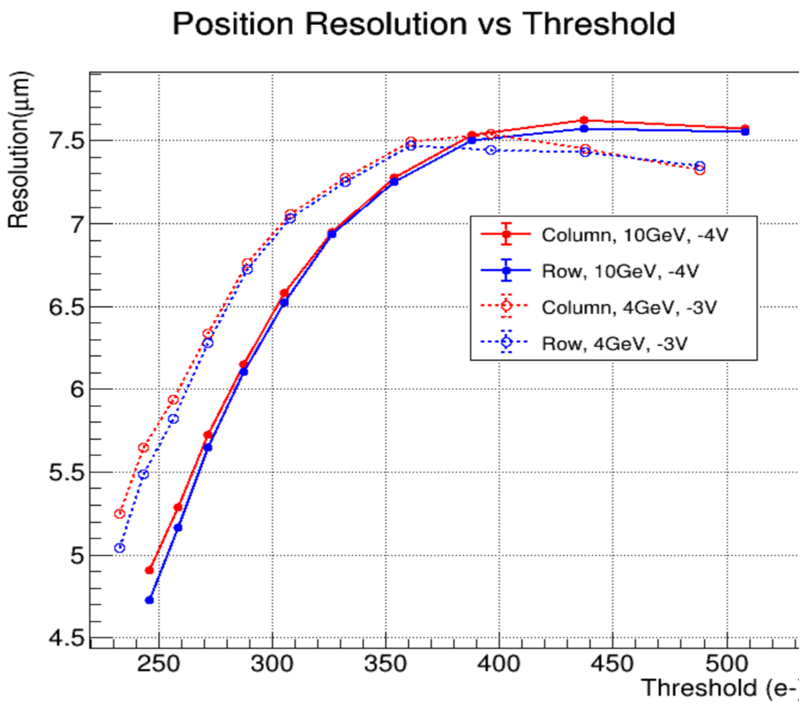


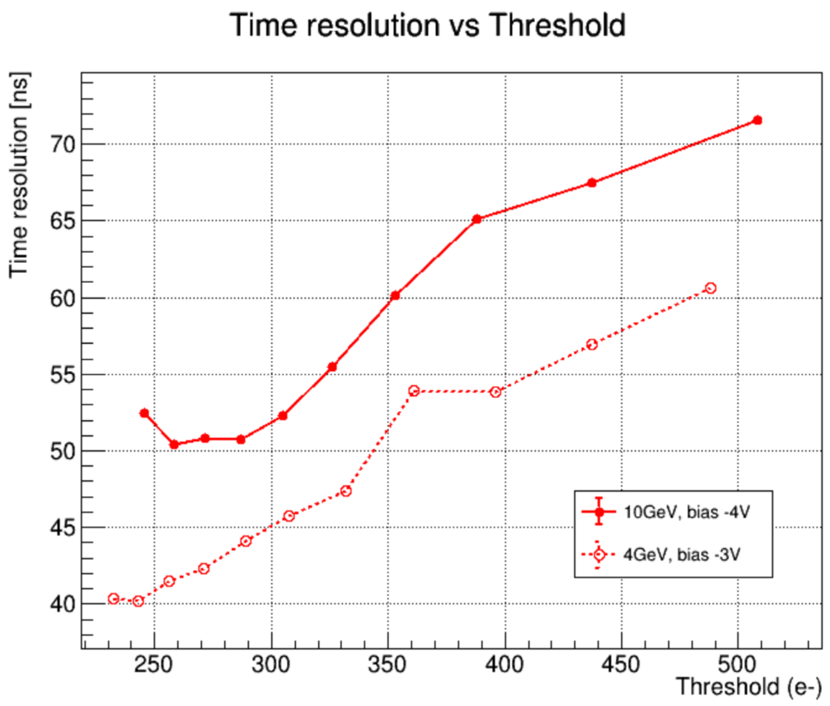


- The efficiency of strip-based pixel is better then that of pixel-based pixel
- ~ 40 ns time resolution is achieved without time-walk correction

Test Result – CharTPix_130







- Efficiency drops rapidly as the threshold increases
- ~ 5 μm spatial resolution is achieved with charge center of gravity applied
- ~ 40 ns time resolution is achieved with time-walk correction

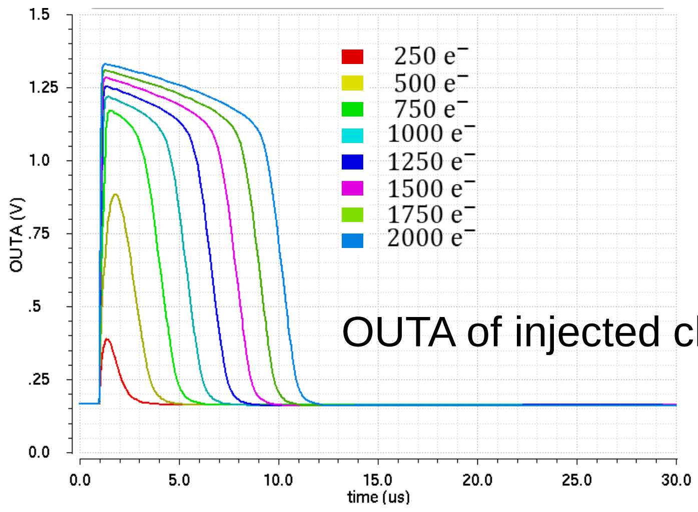
Summary

- MAPS with low power consumption, high spatial resolution and timing resolution, and TOT measurement is required for STCF inner tracker
- MAPS prototypes are developed
  - Large size pixels are explored in 180 nm process
  - Spatial resolution： ~ 5 μm with super-pixel design @ 250e- threshold
  - Time resolution： ~ 40 ns → 20 ns
- Irradiation performance will be evaluated in the near future

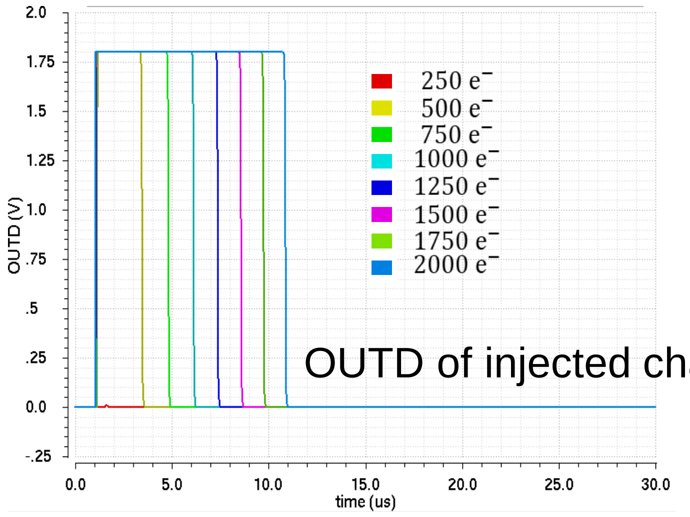
Thanks for your attention !

In-pixel: analog front-end

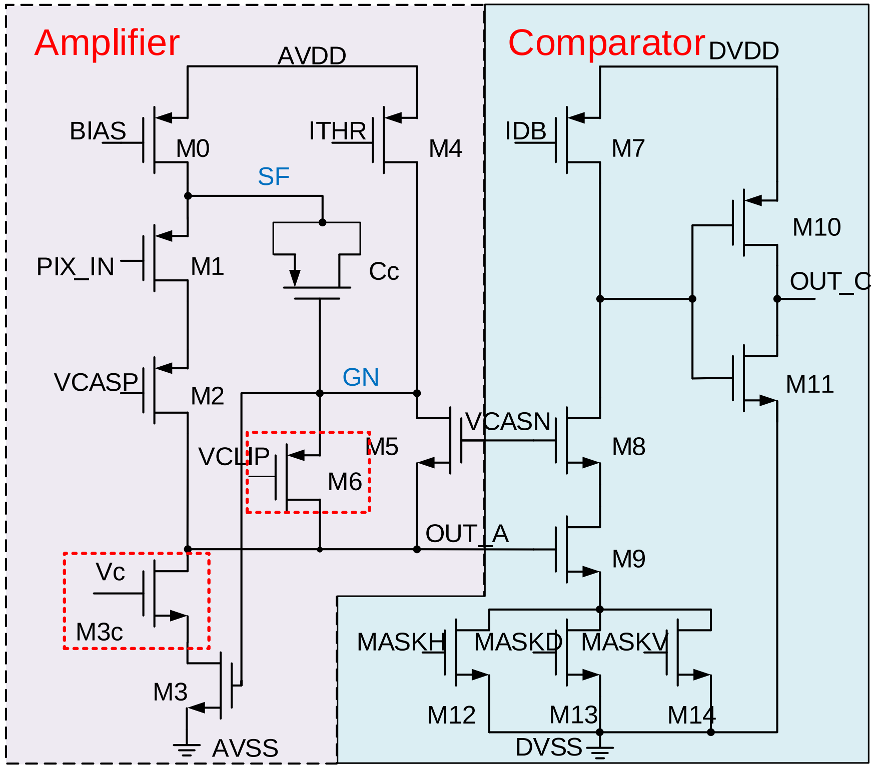
- Amplifier + Comparator
- Simulated performance (180mm×30mm,strip-based sensor)
  - ENC ~14 e-， MISMATCH ~ 6.6 e^-
  - Power consumption: ~800 nA/pix， ~26 mW/cm^2
  - $\Delta ToT/\Delta Q_{inj}$=4.8 μs/$ke^-$



OUTA of injected charge



OUTD of injected charged



In-pixel: digital

- ❖ In-pixel digital circuits
  - – Priority readout based on TOKEN (FE-I3)
  - – Timestamp frequency: 20 MHz
  - – 8-bit leading-/falling-edge
  - – Readout clock: 10MHz