



Quiet Detector, Clear Signals: ENC Noise Studies and Performance Tests of STS Silicon Modules

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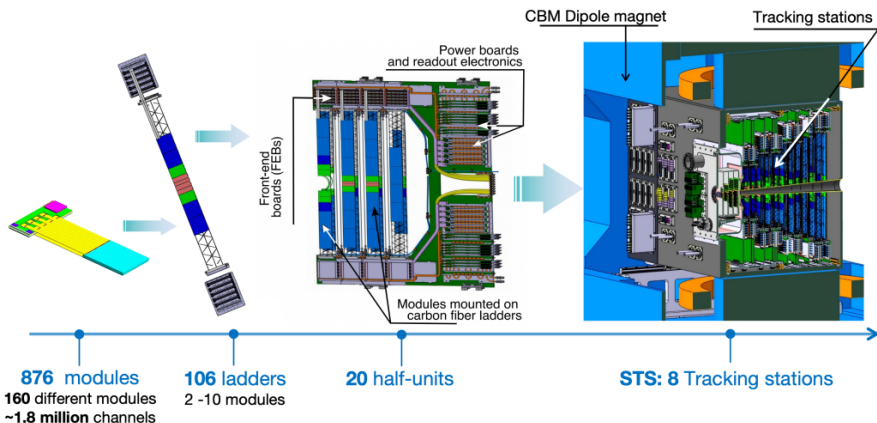


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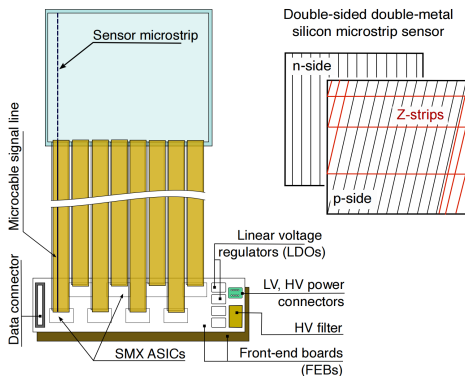
Brief Introduction to the Silicon Tracking System

STS comprises 8 stations (20 half-units) built from 106 ladders using 876 sensors of length 2.2–12.4 cm (6.2 cm wide).



The STS Module

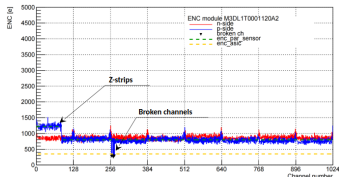
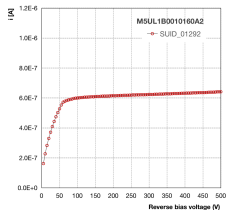
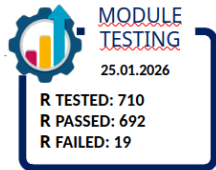
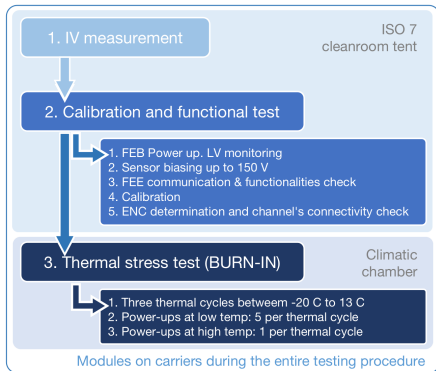
- All components were produced (2019–2024).
- Assembly, testing, and custom module verification setups have been fully operational since 2023.



- 1024 channels per sensor side, read out by 8 ASICs(128 each).

- 876 modules for STS.
- 160 module variants (sensor + microcables).
- Experience with more than 50 pre-series objects built with different form factors.
- Built with different versions of the SMX ASIC.

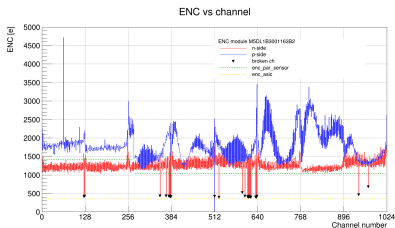
Module Testing in a Nutshell



- All tested modules operate up to the projected end-of-line bias.
 - Early breakdown or high leakage current.
- ENC matches capacitance expectations.
- Robust performance under thermal stress.

ENC Noise Pattern: An Issue to Be Addressed

- ENC quantifies the noise performance of the sensor strip, micro-cable, and front-end SMX ASIC chain.
 - An ENC pattern is observed in both ladder and standalone modules, predominantly on the p-side of 12.4 cm sensors.
1. Micro-cable shielding and routing optimization
 2. Shaping time (90 ns)
 3. Feedback resistance
 4. CSA bias current
 5. Buffer and cascode currents
- ENC pattern suppression is achieved by optimizing Reg(130,14), which controls the CSA buffer and cascode currents.



Testing Approach

- The global register Reg(130,14) controls buffer current (Buffer_CSA) and cascode current (CAS_CSA).
- Reg(130,14) is an 8-bit register: bits 5–3 set buffer current; bits 2–0 set cascode current.
- A 12.4 cm silicon microstrip sensor is used in this study.
- Ladder ID: L5DL1B3
- Module ID: M5DL1B3001163B2

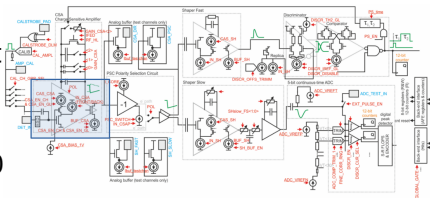


Figure 1: SMX2.2 ASICs.

Buffer	Cascode	Register (130,14)
1	[1–7]	$8 + [1-7] = [9-13]$
3	[1–7]	$24 + [1-7] = [25-31]$
7	[1–7]	$56 + [1-7] = [57-63]$

Table 1: Buffer–cascode current settings.

Analysis Procedure

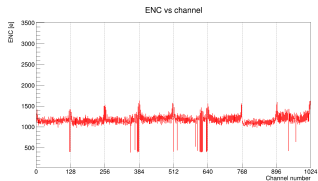


Figure 2: ENC noise vs channel (N-side).

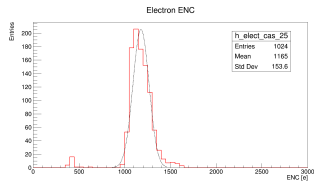


Figure 3: ENC noise distribution (1024 ch.).

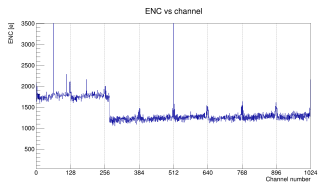


Figure 4: ENC noise vs channel (P-side).

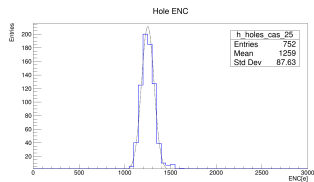


Figure 5: ENC noise distribution (752 ch.).

ENC Noise for Reg(130,14)

- The ENC pattern is fitted with a Gaussian; mean values are plotted versus Reg(130,14) with error bars showing RMS spread.

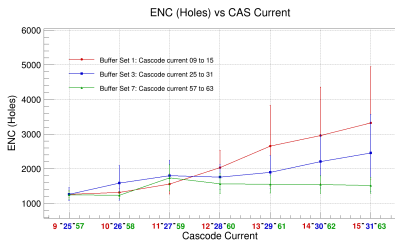


Figure 6: ENC pattern vs Reg(130,14) on P-side.

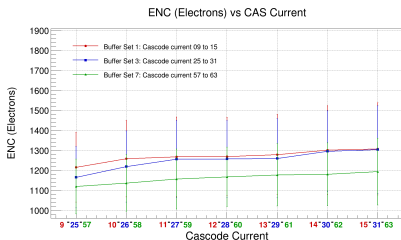


Figure 7: ENC pattern vs Reg(130,14) on N-side.

- The reference point shows less spread at Reg(130,14)=25 compared to 27.

ADC Gain Mean & Sigma for Reg(130,14)

- ADC gain is fitted with a Gaussian; mean values are plotted versus Reg(130,14) with RMS error bars.

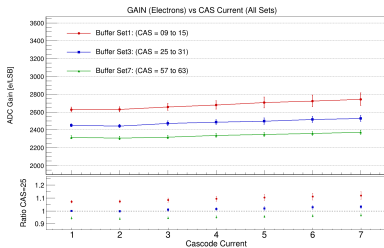
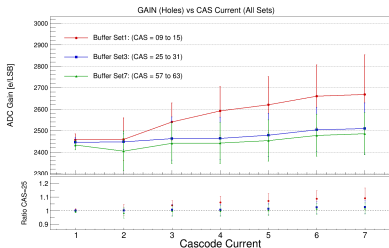
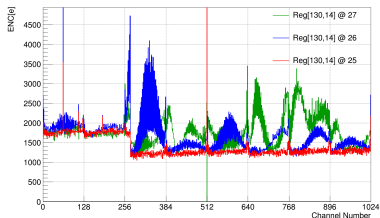
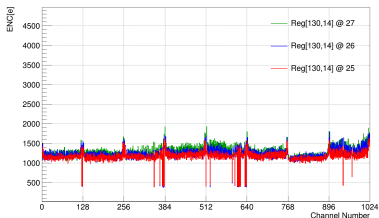


Figure 8: ADC gain vs Reg(130,14) for N-side. Figure 9: ADC gain vs Reg(130,14) for P-side.

- ADC gain at Reg(130,14)=25 differs by less than 5% from Reg(130,14)=27.

ENC Noise Pattern



- A clear ENC pattern is visible at Reg(130,14)=26 and 27; at 25 the pattern is suppressed, and noise levels are lower.
- The ADC Gain at Reg(130,14)=25 is still under 5% as compare to 27 to maintain the signal integrity.

STS Under Construction

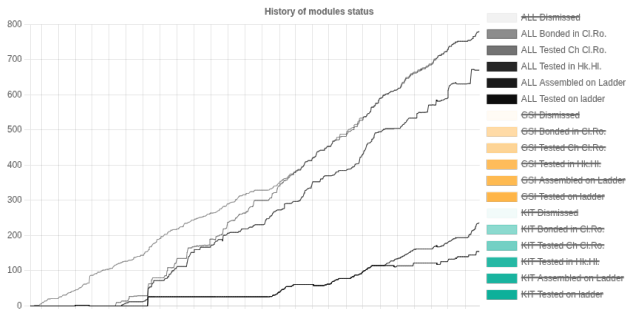


Figure 10: STS Modules Production Stage

- 768 modules **produced** (87%).
- 669 modules **tested** (76%).
- 28 ladders **built** using 226 tested modules (26%).
- 19 ladders fully **tested** (145 modules, 17%).

Thank You!



Even in the coldest paths, purpose keeps us moving!

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ENC Noise σ for Reg(130,14)

- The ENC pattern is fitted with a Gaussian; RMS values are plotted versus Reg(130,14).

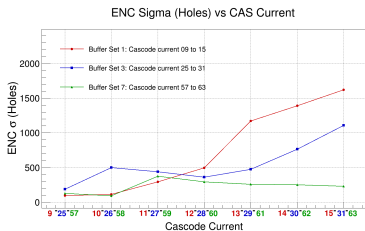


Figure 11: ENC spread (RMS) vs Reg(130,14) for P-side.

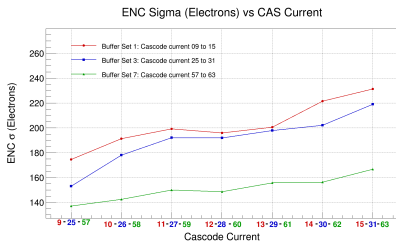


Figure 12: ENC spread (RMS) vs Reg(130,14) for N-side.

- The reference point shows less spread at Reg(130,14)=25 compared to 27.