Development of HV-CMOS Pixel Sensors in 55nm Process

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On behalf of the HV-CMOS pixel sensors in 55nm process collaboration

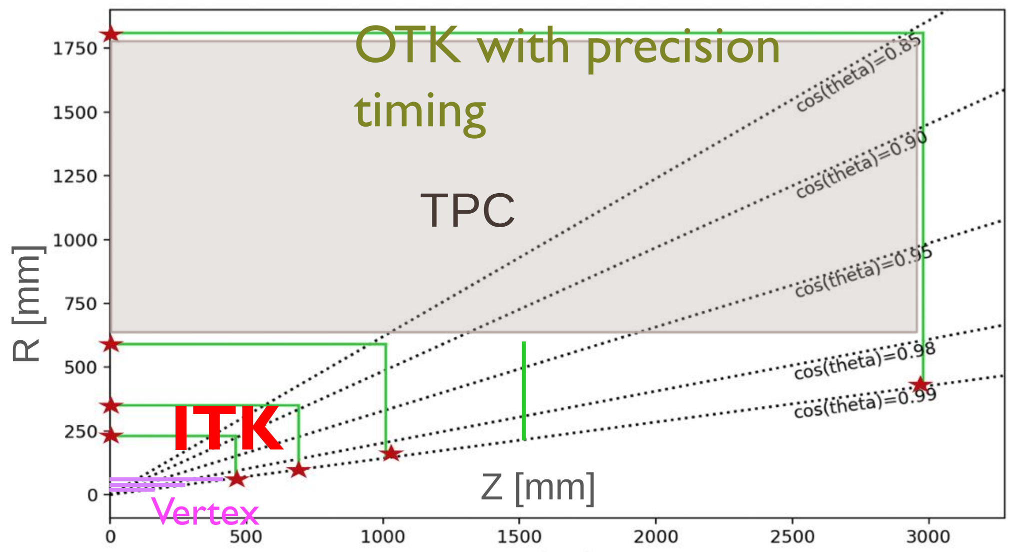
COFFEE

CMOS SENSOR IN
FIFTY-FIVE NM PROCESS

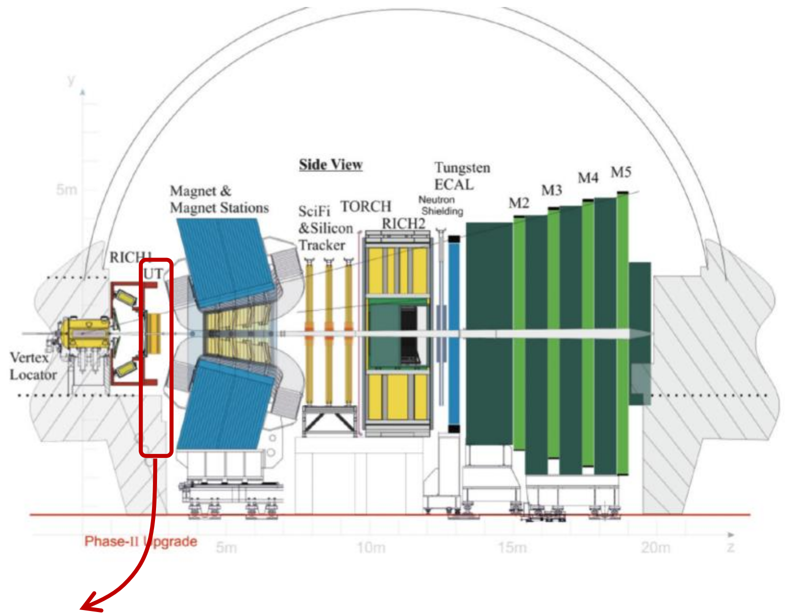
The TIPP 2026, TIFR, Mumbai, Feb. 2-6, 2026

Background & Motivation

Current R&D targets for two applications：



CEPC Inner Tracker (ITK)

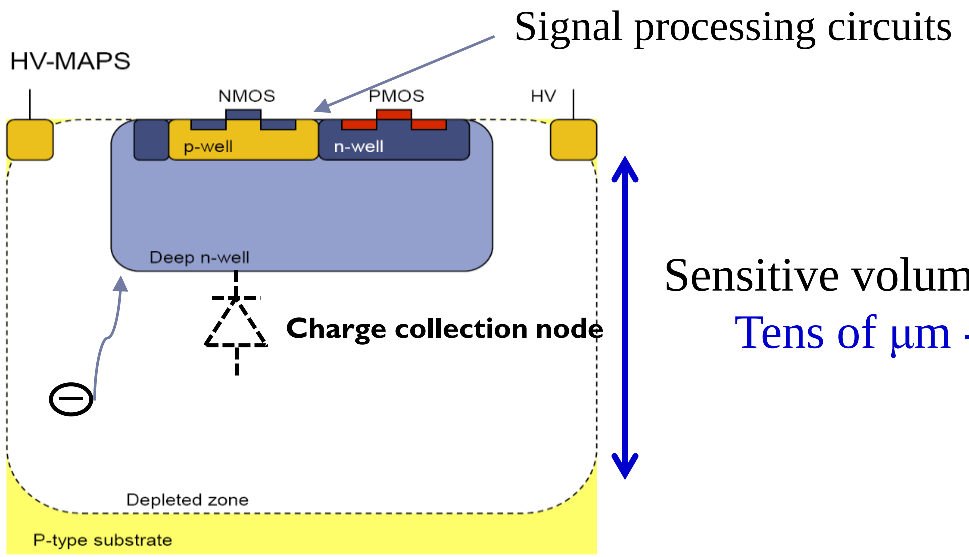


LHCb Upstream tracker upgrade II (UP)

- **Requirements**： Time resolution ~ ns； Spatial resolution ~10 μm; Power dissipation < 200mW/cm^2 ；
- **Differences**：
  - LHCb UP requires higher hit density processing capability (~100 Mhz/cm^2) and higher radiation resistance (> 100 Mrad , >10^{15} N_{eq} /cm^2);

HV-CMOS Pixel Sensor： a promising candidate for both applications

It is also called the "Depleted Monolithic Pixel Sensor (DMAPS)"



Sensitive volume:
Tens of μm -> hundreds of μm

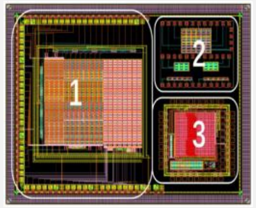
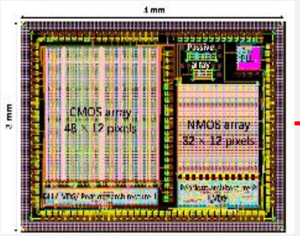
Cross section of a single pixel of a typical HV-CMOS pixel sensor

- Fast charge collection: ~ ns;
- Radiation tolerance (NIEL): $>10^{15}\ N_{eq}\ /cm^2$;
- Power consumption
- Position resolution
- Radiation tolerance (TID)

More advanced process nodes bring potential benefits! (180 nm -> 55 nm)

COFFEE Series Development Roadmap

CMOS sensOr in Fifty-Five nm process

COFFEE2	COFFEE3	CHiR 1.0	CHiR_x	Final version
			0.5cm × 2cm	2cm × 2cm
55nm HV-CMOS process	Small prototype	Process modification and validation	¼ full size sensor	Full size sensor

COFFEE series development — 2023.08 — 2025.01 — 2026.01 — 2027

Key progress:

- Verified the technical principles
- Chip design architecture verification
- Process modification and verification

Design Overview of COFFEE2

Three independent regions in COFFEE2:

1. **Passive diode arrays:**
   - Various sensing structures: DNW size, distances, with/without P-stop ;

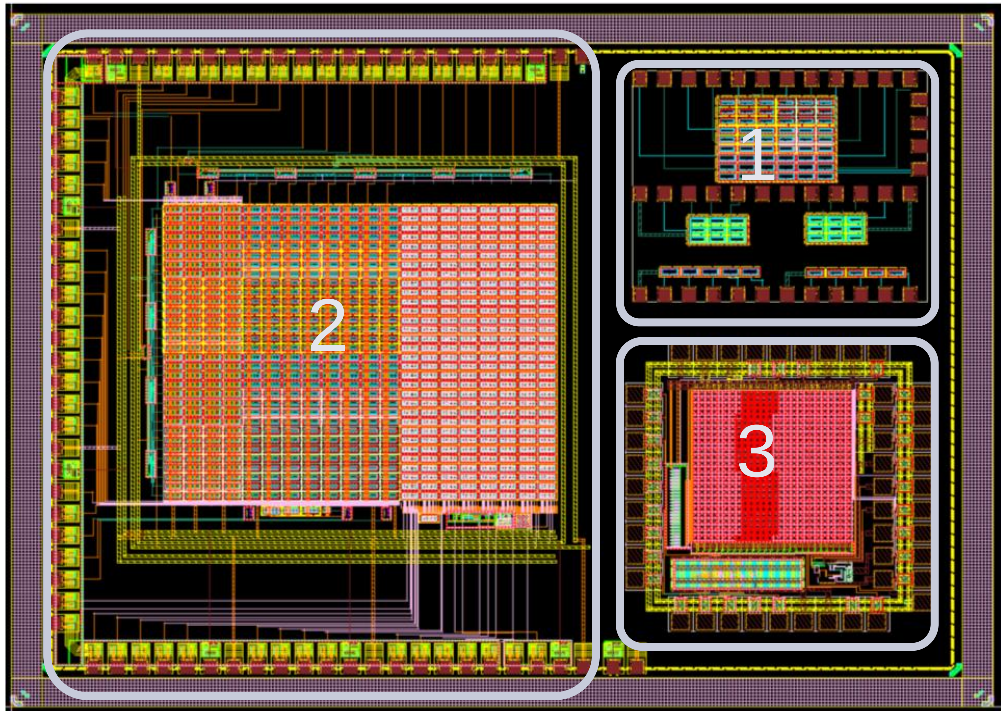
   For the commercial process characteristics study

2. **An active pixel matrix including 3 variations of pixel design:**
   - To quantitatively evaluate the "cross-talk" issue of HV-CMOS pixel sensor technology in the new process and guide the overall design of the future detector chip

   For charge sensing diode + in-pixel AFE study

3. **An active pixel matrix with a new readout architecture:**
   - Very small pixel size 25×25μm^2 (for a HV-CMOS pixel sensor);
   - New matrix readout architecture;
   - Digital peripheral data processing included;

   For new architectures in 55nm process @ Designed by KIT



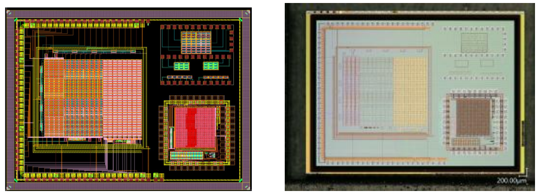
The COFFEE2 design includes three independent regions.

Published paper: 1. NIMA Volume 1069 P169905 (2024) https://doi.org/10.1016/j.nima.2024.169905;
2. 2025 JINST 20 C03023 . https://doi.org/10.1088/1748-0221/20/03/C03023;
3. 2025 JINST 20 C10011. https://doi.org/10.1088/1748-0221/20/10/C10011;

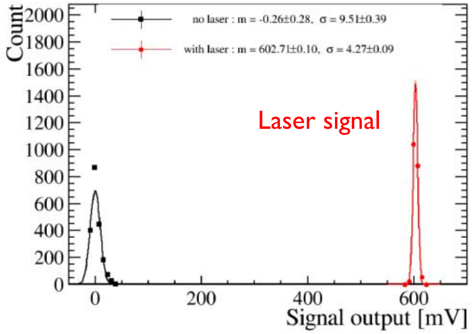
Results from COFFEE2

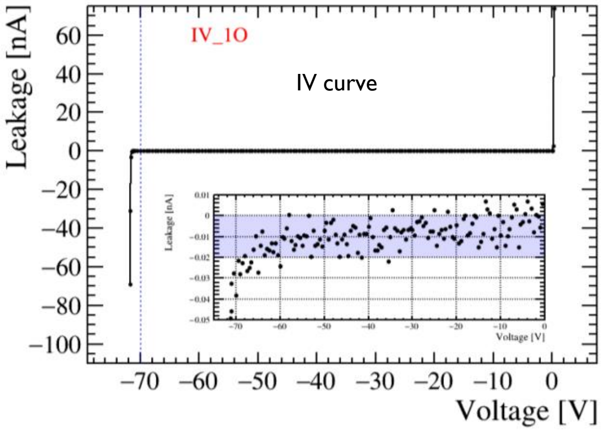
Feasibility study of a commercial 55nm HVCMOS process for future R&D

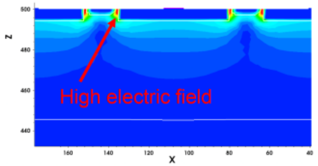
- For the sensor: breakdown voltage ~ -70V for regular resistivity wafer (10 Ω·cm)
- For electronics: the in-pixel amplifier & comparators work as the simulation predicts
- For the sensing diode + in-pixel amplifiers: clear response to laser/ ^{55}Fe / ^{90}Sr sources
- Leakage current increase from ~10pA/pixel to ~1nA /pixel after irradiation of 10^{14} n_{eq}/cm^2.

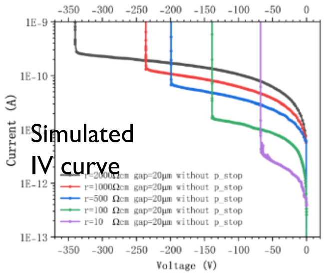


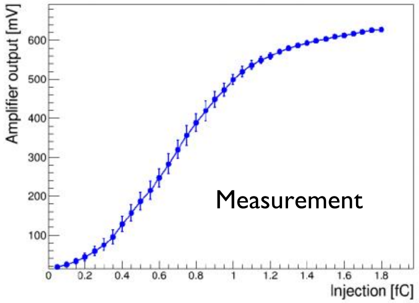
COFFEE2, the first prototype in 55nm HV-CMOS process

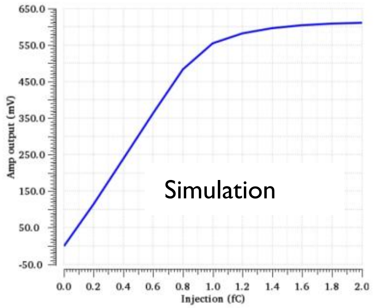




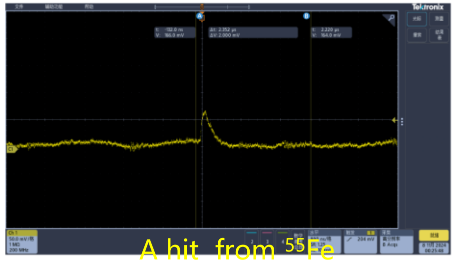






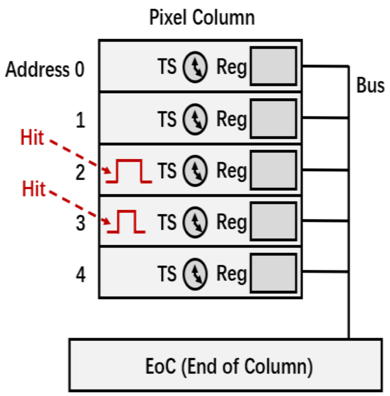


CSA output as function of charge injection

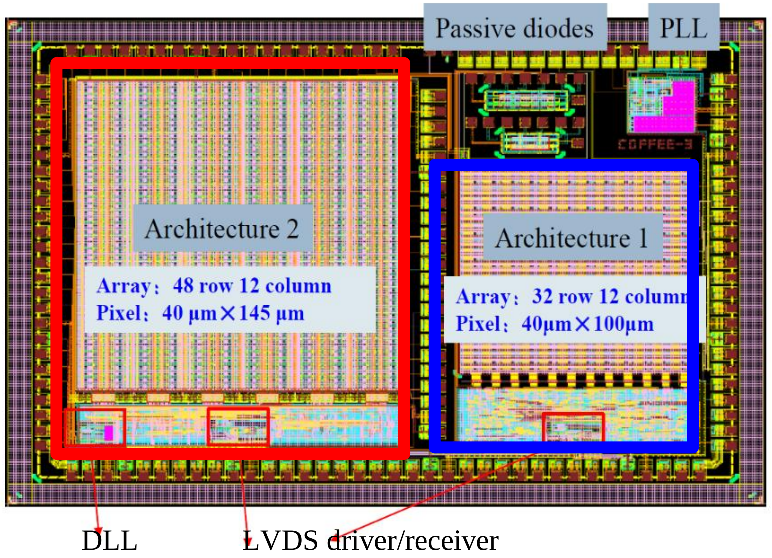


Layout and Targets of COFFEE3

Architecture 2：In pixel TDC，hit signal readout in priority to EoC

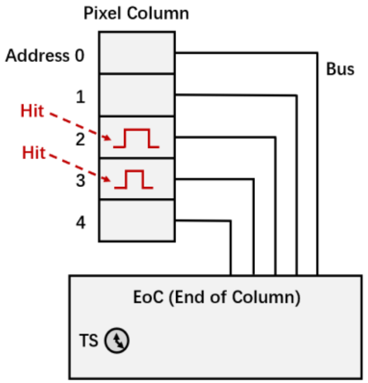


- **High incident flux processing capability** （>100 Mhz/cm²）



COFFEE3 layout，3×4 mm².

Architecture 1：In pixel digitization，hit signal readout in parallel to EoC



- **Low power consumption and high potential for position resolution** （~100 mW/cm²，~5 μm possible）

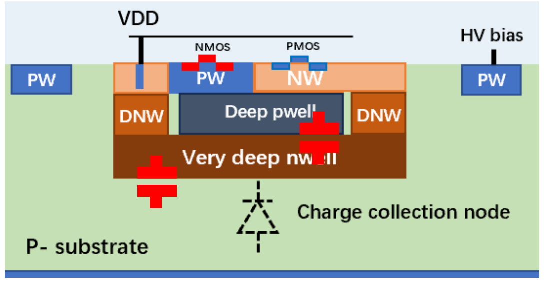
Main design:

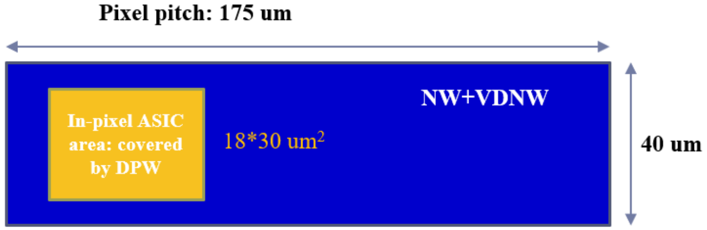
- ➢ **Two independent readout architecture**, both could be scaled to large sensor (~2×2 cm²);
- ➢ Necessary digital and analogue Peripheral Function Modules;

To answer:

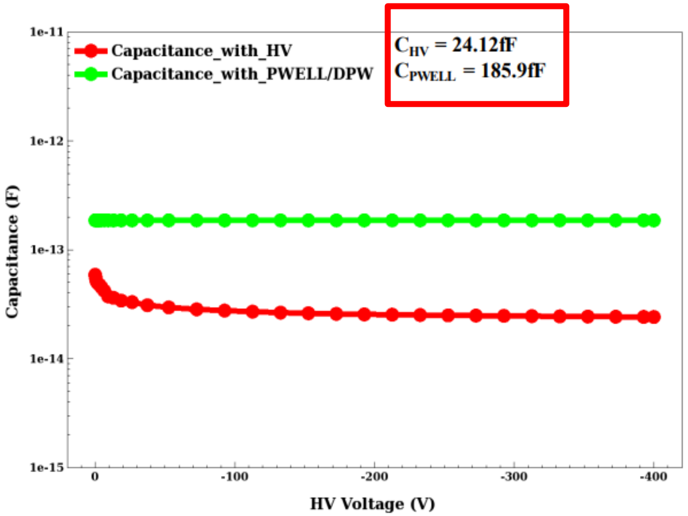
1. **If it possible to meet**（**Time resolution** ~ ns； **Spatial resolution** ~10 μm; **Power dissipation** < 200mW/cm²） **at the same time;**
2. **What's more can 55 nm process bring to DMAPS?**

Architecture 1: a simple in-pixel design leads a small C_{diode}





*Cross section (left) and top (right) view of "a pixel": VDNW and P-substrate formed the charge collection electrode. Capacitance of the diode contributes from the "**DPW with VNDW**", and "**VDNW with Psub**".*



TCAD simulation of the C_{diode} of "the pixel" vs the biasing voltage of the substrate.

- **The C_{diode}:**

Capacitance between DPW and VDNW is the main source of C_{diode}. A simple in-pixel electronic structure (small DPW size) is crucial for small C_{diode}.

- **The power consumption:**

$$\tau_{CSA} \propto \frac{1}{g_m}\frac{C_d}{C_f} \qquad TW \propto \tau_{CSA}\frac{V_{TH}}{V_{sig,min}}$$

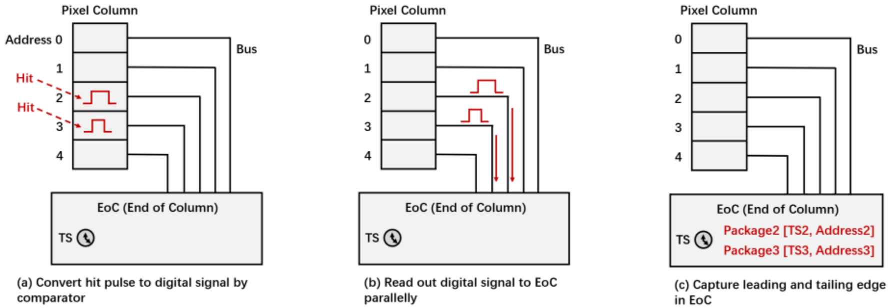
For a determined temporal response, **a smaller C_d** and **larger signal** are crucial to reduce the power consumption of the in-pixel amplifer.

Architecture 1: only a CSA and a comparator in pixel → very compact in-pixel ASIC layout.

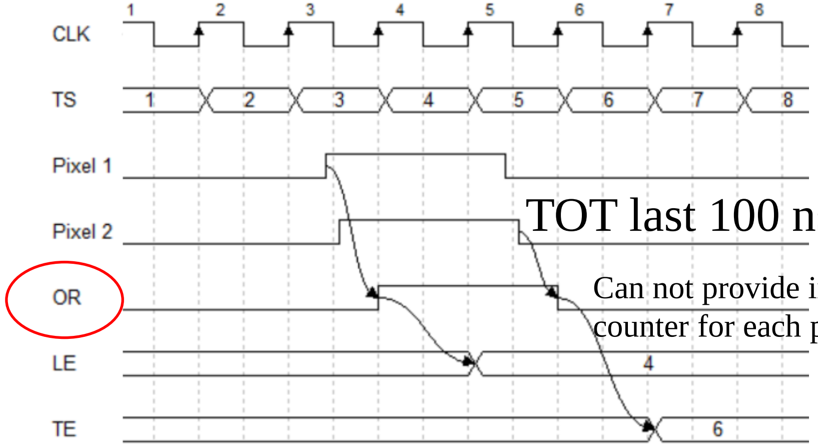
--» potential for low power & small pixel size (high position accuracy)

Architecture 1: design for Higher Hit Density Processing Capability

Architecture 1: Pixel Hit Parallel Transmission to Array Bottom



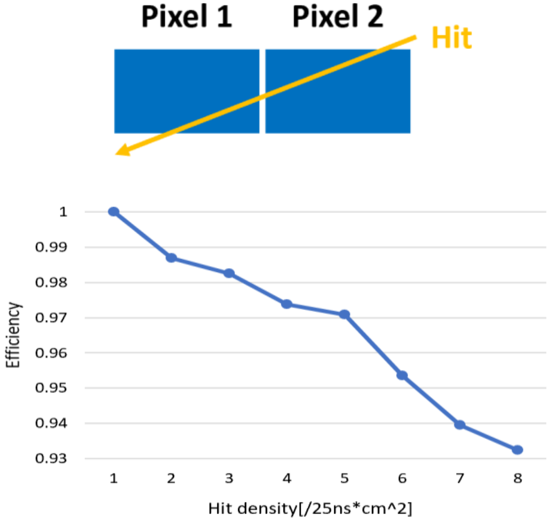
Each column shares an EoC module



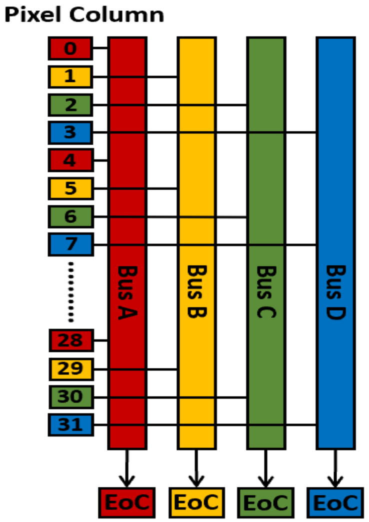
TOT last 100 ns -1.6 μs

Can not provide independent time stamp counter for each pixel at EoC

- ➢ This concept with 1 EoC for each column, while hit density increase, the timestamp information maybe inaccurate.



For high hit density, there will be some loss in efficiency.

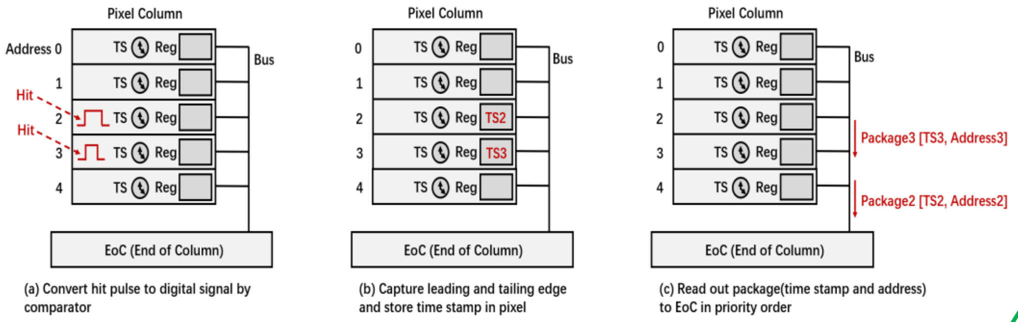


One pixel column architecture in COFFEE3.

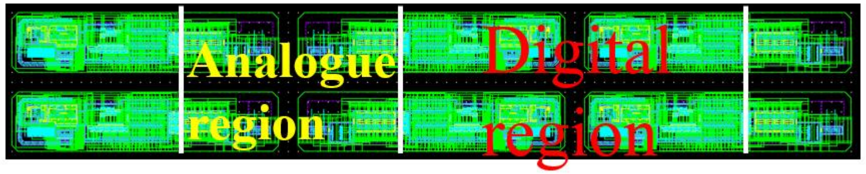
- ➢ **Limitation: while hit density increase (eg. > several tens of Mhz/cm^2)**
  - ➢ **Timestamp information inaccurate;**
  - ➢ **Efficiency loss;**
- ➢ **To handle higher hit rates: 4 EoC modules for each column, and two FSMs for each Eoc in COFFEE3.** The area of the peripheral digital circuits does not significantly increase (still less than 10% of the whole sensor).

Architecture 2: for more possibilities & High hit density processing capability

Architecture 2: the event time information are **recorded within each pixel**. Then read out to the bottom of the array in order of priority

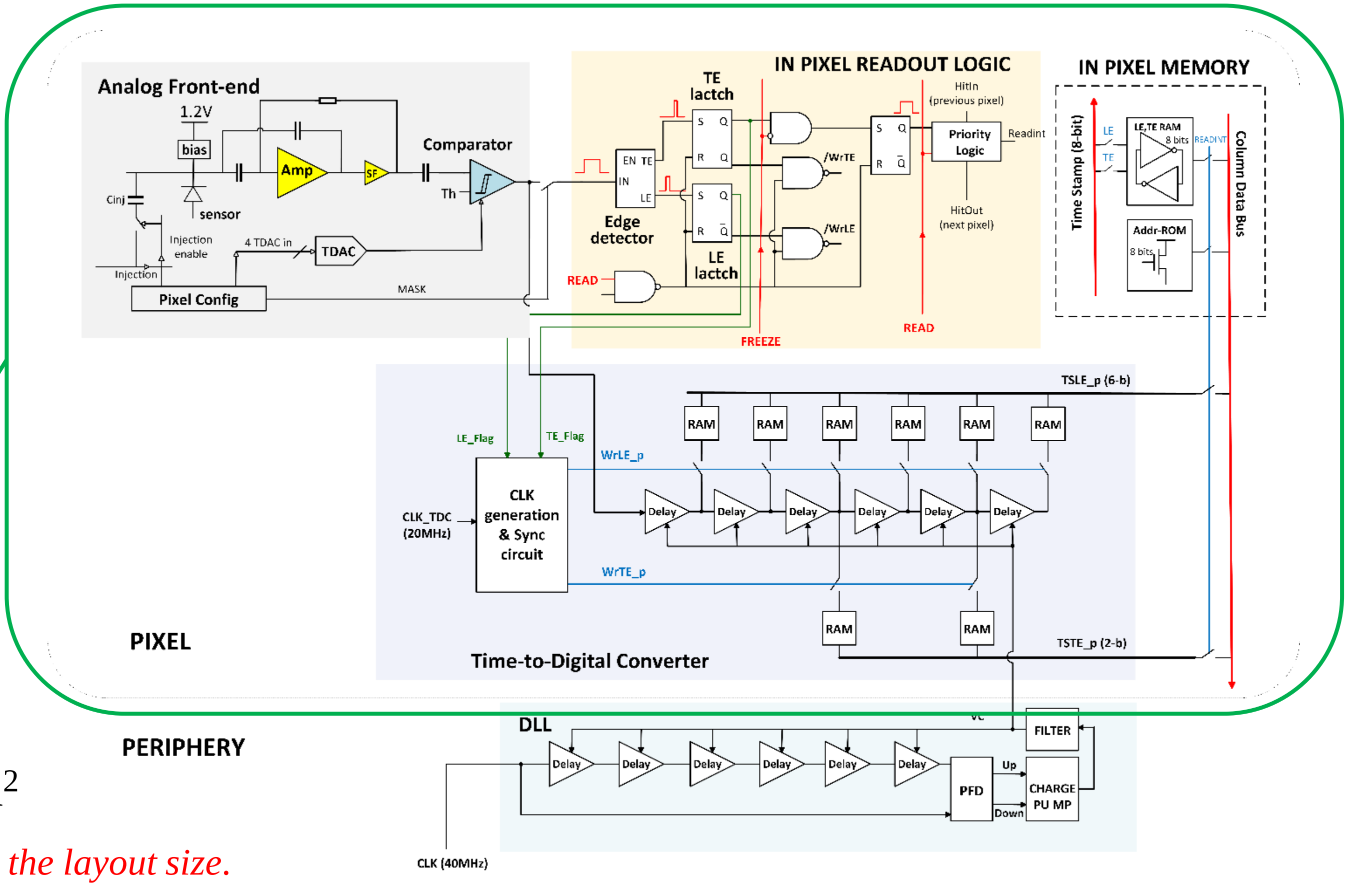


No limitations like Architecture 1, time information is accurate.



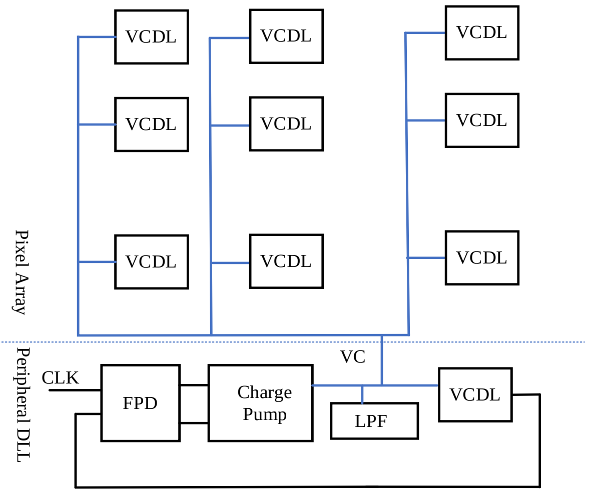
Layout of 2×3 pixels， signal pixel size is 40×145 μm^2

**The actual manufacturing size will be scaled down to 0.9 times the layout size.*

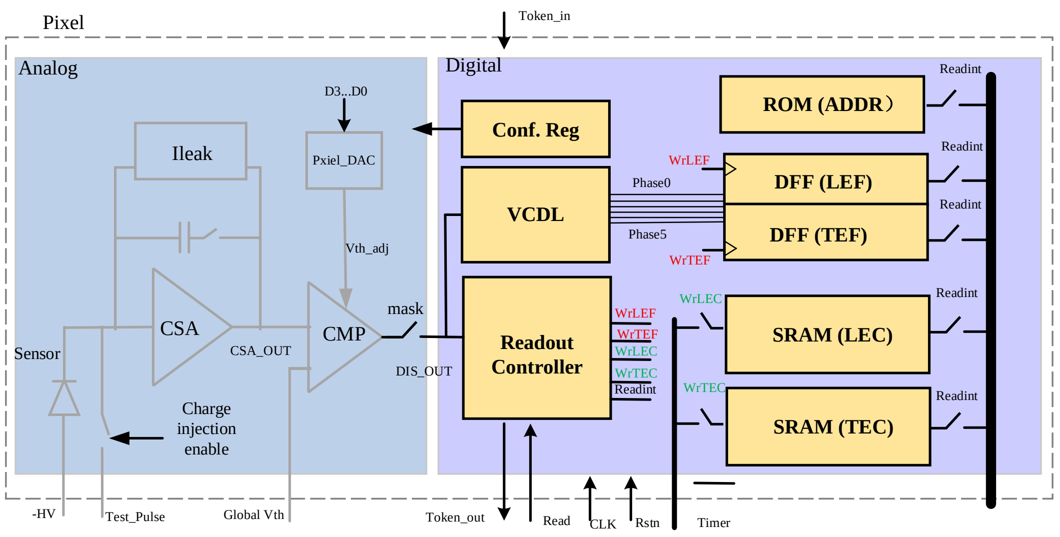


➢ More integration in-pixel: The analog front-end, comparators, in-pixel DACs, priority readout structure, memories, and TDCs have all been integrated within a limited pixel area. This further enhances the capability of HV-MAPS to provide high-precision hit information in high hit density applications.

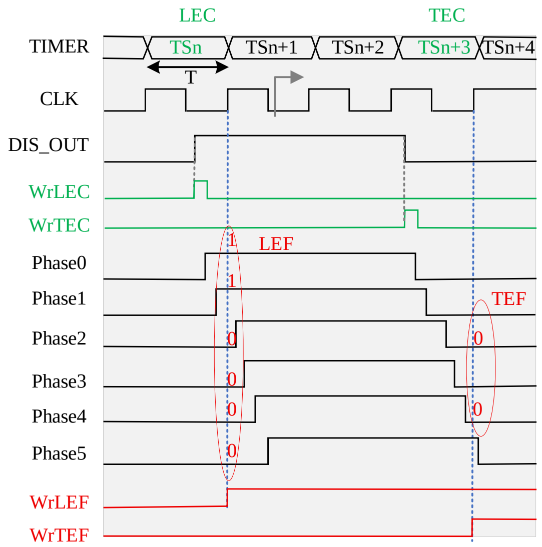
Architecture 2: design for lower power dissipation



Peripheral DLL and duplicated in-pixel VCDL



The comparator output is used for VCDL



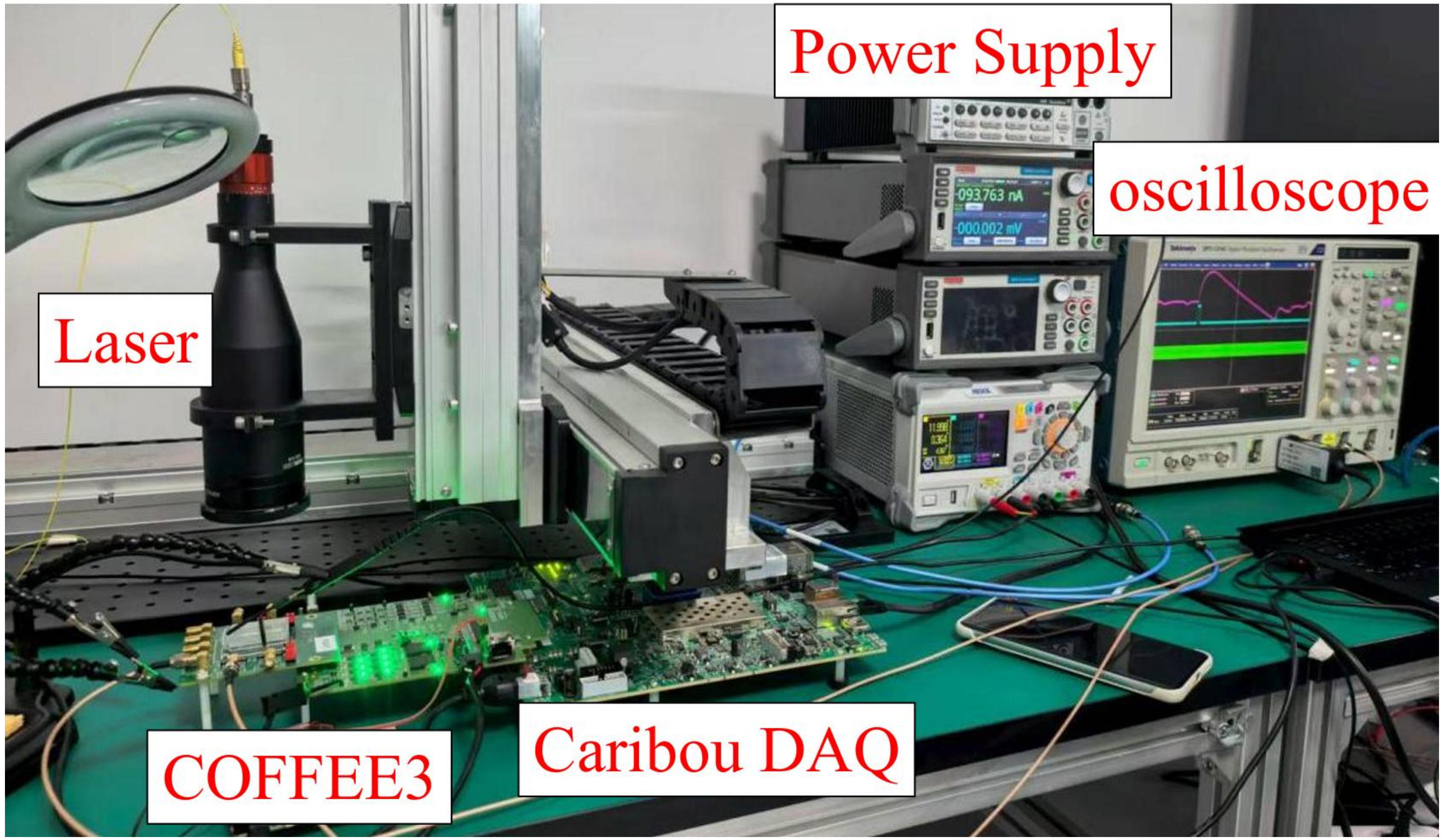
6 phases are used for Leading edge and 2 of them are used for tailing edge.

Deign of in-pixel Coarse-fine TDC: for lower power dissipation

4.16ns fine timestamp for LE

- Only a small VCDL block in-pixel (DLL is at the Peripheral);
- Almost no static power consumption for in-pixel TDC: only works while pixels are fired;
- Low power for Coarse time-stamp distribution into pixel matrix: 20 Mhz (Convert to 40 MHz, within the pixel);
- One delay line for both Leading edge and Tailing edge information (The ToT information is almost free).

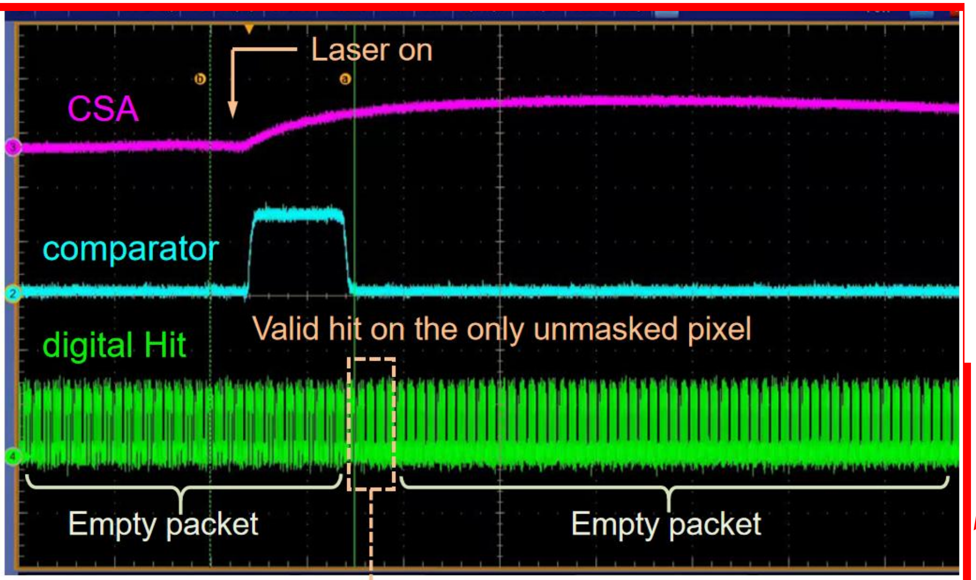
The Preliminary Test Results of COFFEE3



Response of Full Readout Chain with Laser Test

Architecture 2: in-pixel TDC

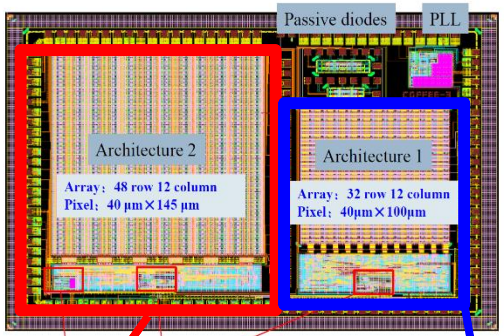
Architecture 1: in-pixel NMOS design



4 bit	4 bit	8 bit	8 bit	6 bit	2 bit	7 bit	3 bit
header	CHIP_TS	LE_coarse	TE_coarse	LE_fine	TE_fine	Addr_Row	Add_Col
0 1 1 0	0 1 0 1	0 0 0 1 0 1 1 0	0 1 1 0 1 0 1 1	1 1 0 0 0 0	0 0	0 0 0 0 0 0 1	0 0 0

A valid transmission packet corresponding to a hit

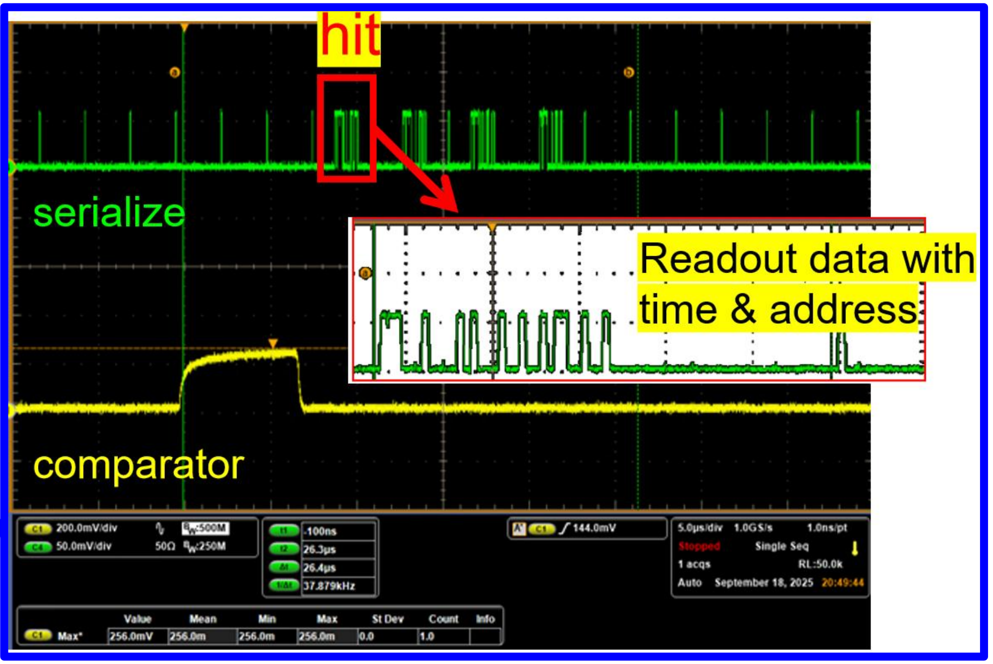
Correct row & column address



DLL

LVDS driver/receiver

Layout of COFFEE3



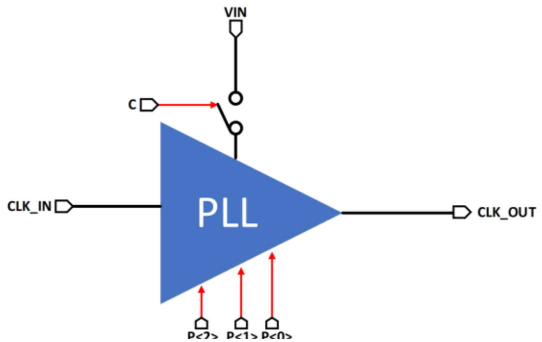
The full readout chain works for both of the two readout architectures.

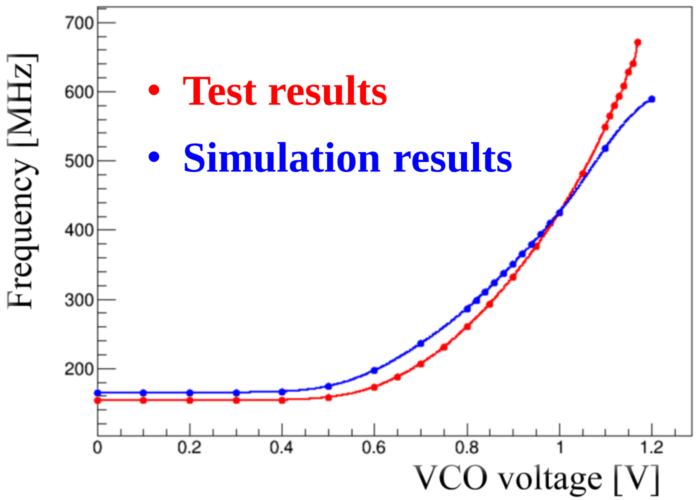
Sensing diode → in-pixel (CSA\comparator\TDC) → EOC (digital peripheral) -> data link-> DAQ

Test Results of Functional Modules

All the functional modules designed in COFFEE3 work:

- PLL works ups to 640Mhz





- LVDS driver/receiver works at 640 Mhz support 1.28 Gbps data link

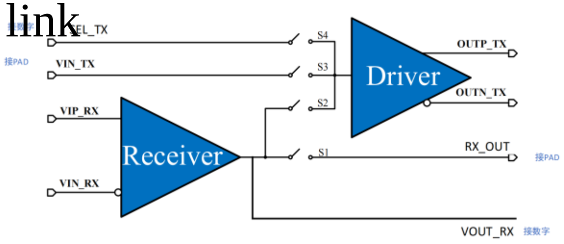
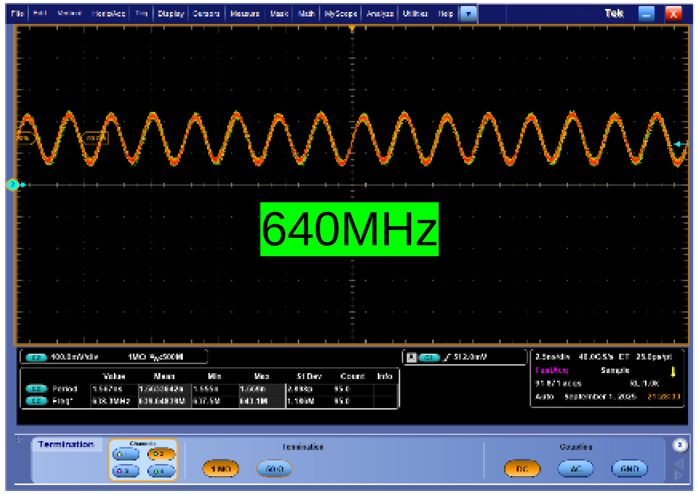
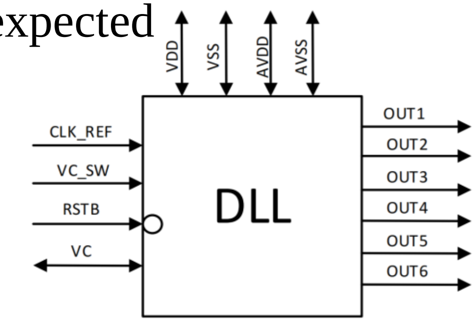


Fig 3.1.1 LVDS block diagram

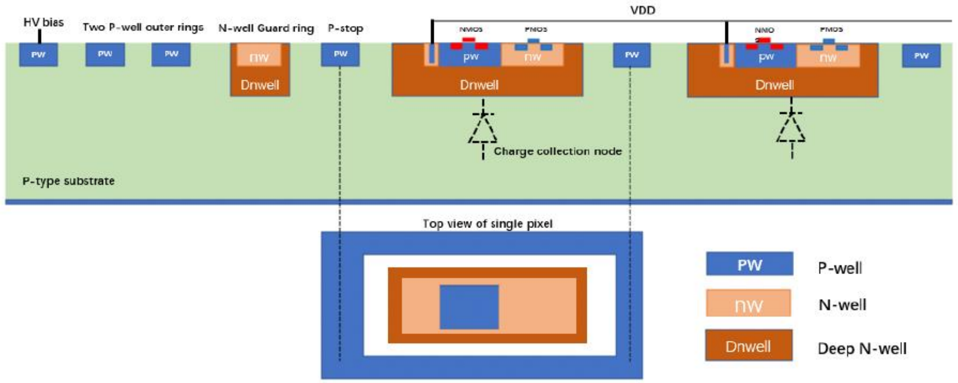


- Delay line for in-pixel TDC works as expected



The preliminary test results are positive

However, standard commercial 55nm HV-CMOS process is by no means the ideal MAPS process



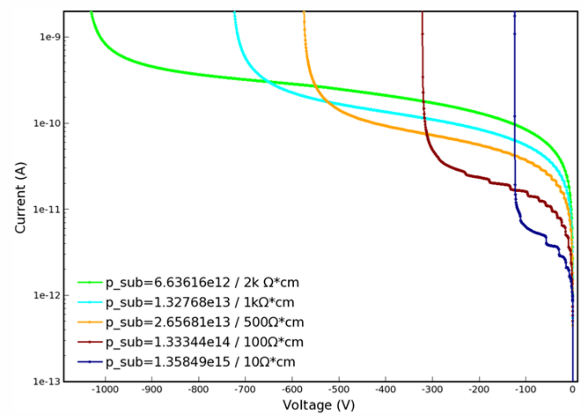
1. Triple-well process → cross-talk risks between sensor (deep-n) and PMOS transistors； **→ Restrict the flexibility of in-pixel design;**
2. Break down at ~-70V; **→ Extremely limits the SNR.**
3. No access of high-resistivity wafers;

In collaboration with the Foundry, some process modifications have just been made

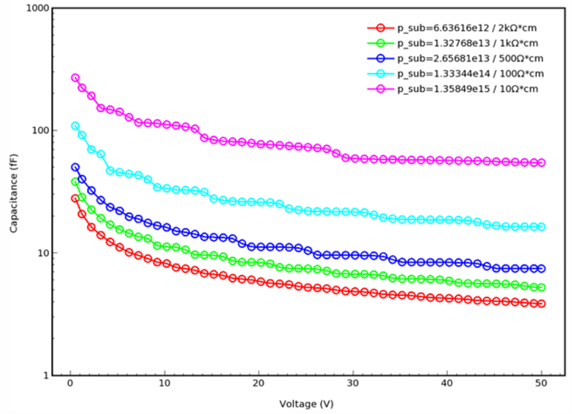
for better sensor performances

Process Modifications for better Sensor Performances

Modifications：

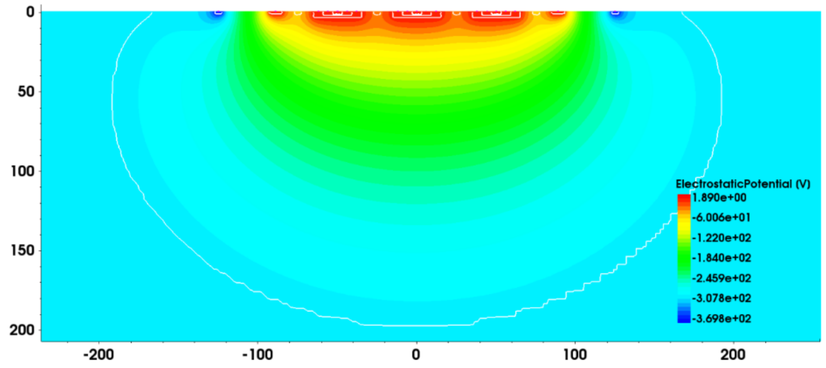


- Breakdown V: **70 --> > 400V**



- Capacitance of VDNW/p-sub: **~ hundreds fF --> ~ tens of fF**

- Add layers: Deep-PW & Very-deep-NW;
- Change doping rules affecting breakdown voltage;
- Replace wafer: from 10 Ω·cm --> >1k/2k/4k Ω·cm;



- Depletion depth: ~10 μm → >200 μm

Huge S/N gain : Signal increase >10 times, while C_{diode} reduce

First Design based on Modified Process: CHiR 1.0

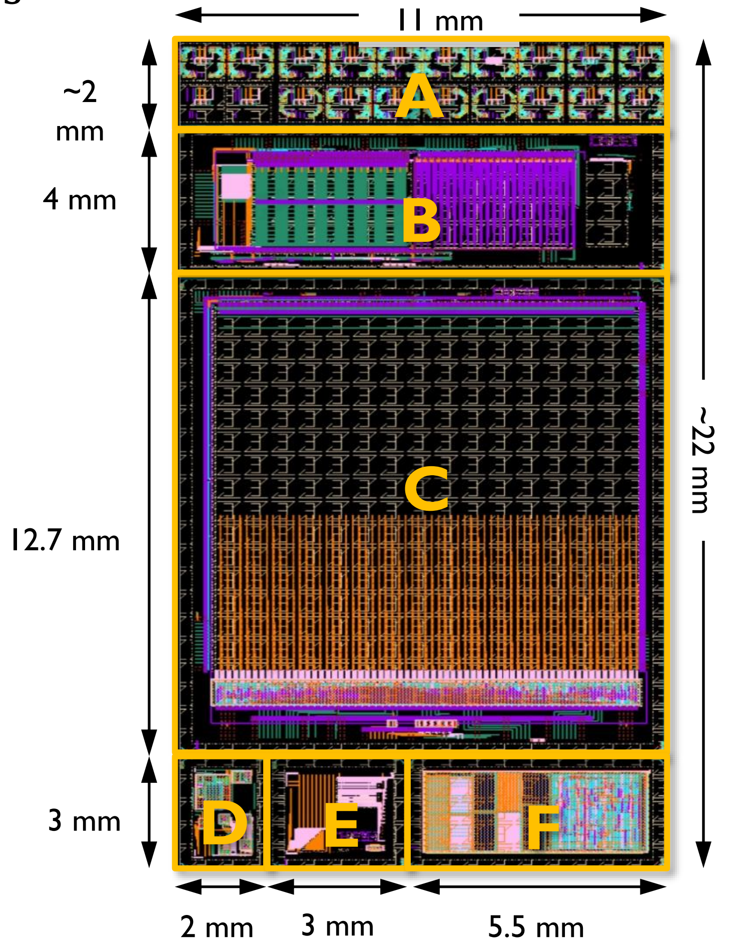
*CHiR (COFFEE-HiRes)

20 times the layout size of COFFEE3, can be diced into a number of chips serving various goals:

- **Guard rings & Passive sensor design validation:**
  - **(A)** 20 arrays of 3x4 passive pixels with diff guard ring designs, each can be diced into individual 1x1 mm^2 chip;
- **In-pixel FE and Active pixel matrix design validation:**
  - **(B)** 9 variations of in-pixel FE designs & 12 variations of pixel sizes;
  - **(C) A** 256 × 64 pixel matrix (pixel size 38 μm x 150 μm) with digital periphery
- **Analogue IP & Digital modules and transistors validations**
  - **(D)** necessary analog IPs: PLL, DAC, LVDS, SLDO …
  - **(E)** alternative small pixel arrays and two more SLDO versions
  - **(F)** digital modules and transistors for TID and SEE studies

The design was completed and submitted just one week ago.

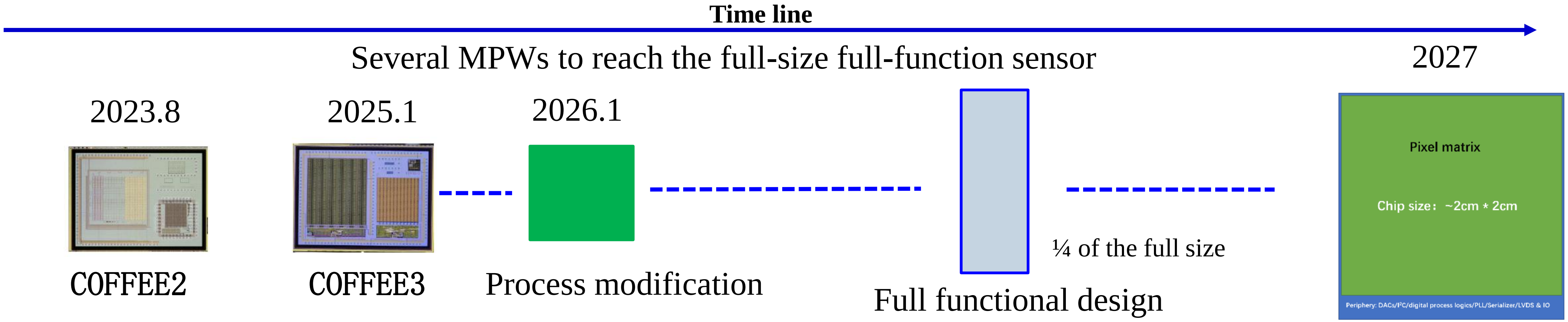
Answers to many key questions can be expected!



Layout of CHiR1.0, submitted Jan. 24, 2026

Summary and Outlook

- We have complete the design of COFFEE2/3 in a commercial 55nm HV-CMOS process； The preliminary test results are positive, more performance tests are in progress;
- The first design CHiR 1.0, based on the modified process has been submitted; answers to many key questions can be expected!
- Hopefully, we could have the full-function and full-size chip at the end of 2027.



Target: Time resolution ~ ns； Spatial resolution ~10 μm; Power dissipation < 200mW/cm^2 ;

Acknowledgements

Name list: Random ranking

Leyi Li, Xiaoxu ZHANG, XiaoMin WEI, Weiguo LU, Pengxu LI, Mei ZHAO, Yang ZHOU, Bingchen Yan, Anqi WANG, Yuanhong JIAO, Yang CHEN， Yujie WANG, Huimin Wu, Zexuan ZHAO, Yu ZHAO, Zheng Wei, Jianpeng DENG, Zhan SHI, Kunyu XIE, Xinhao XIE, Xiaolong WANG, Ziying ZHANG, He HUANG, Junyuan YAN, Shenyao TANG, Hui ZHANG, Ruoshi DONG, Yang CHEN, Xuekang LI， Xinyang GUO, Zhuojun CHEN, Hui ZHANG, Zhiyu XIANG, Zijun XU, Zeng CHENG, Kang LIU, Menke CAI, Boxing WANG, Yuman CAI, Mingjie FENG, Lei ZHANG, Meng WANG, Hongbo ZHU, Yiming Li, Jianchun WANG

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