



U.S. DEPARTMENT OF  
**ENERGY**

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Science



**ATLAS**  
EXPERIMENT

# ATLAS Inner Tracker (ITk) Upgrade Technological Challenges and Lessons Learned

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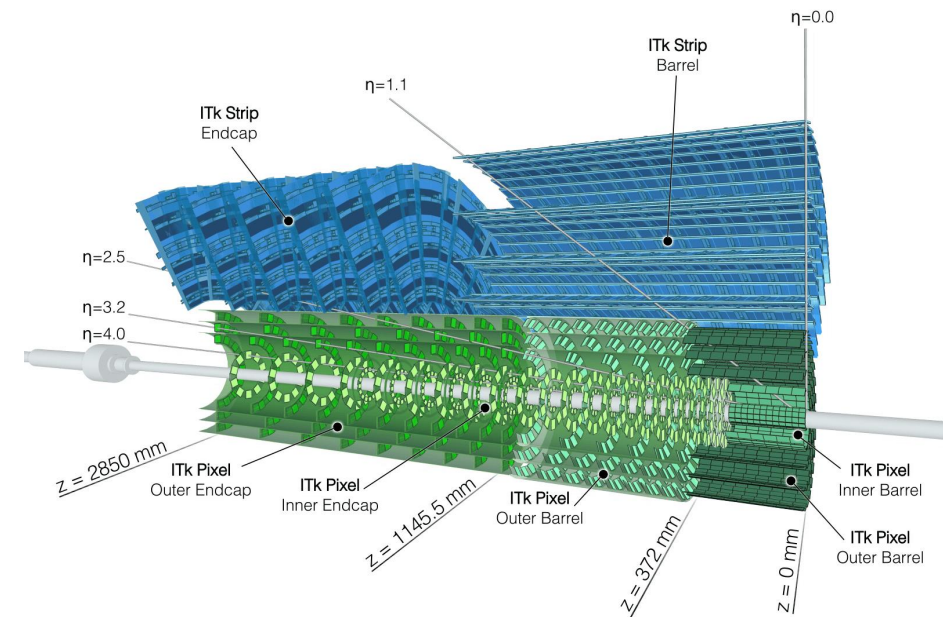
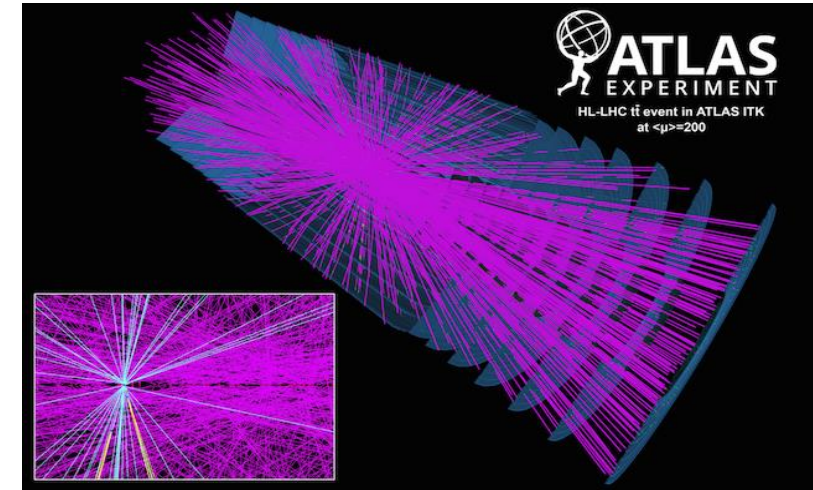
University of California, Santa Cruz

**On behalf of the ATLAS ITk Collaboration**

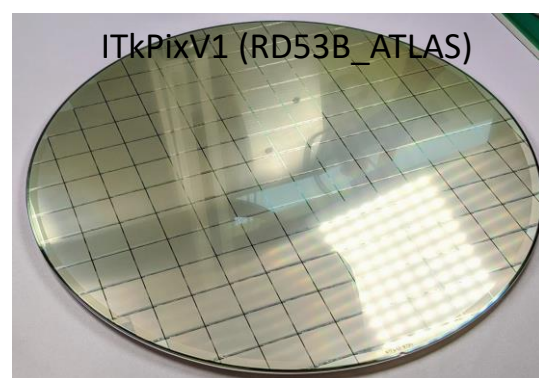
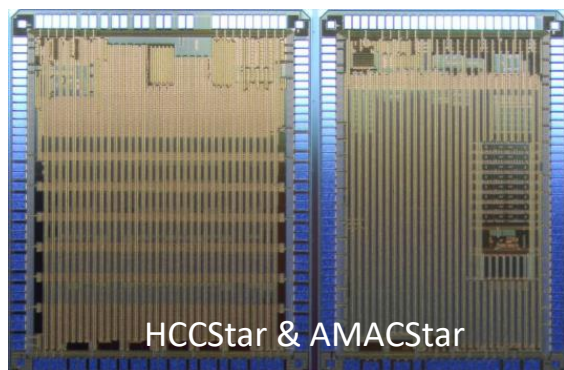
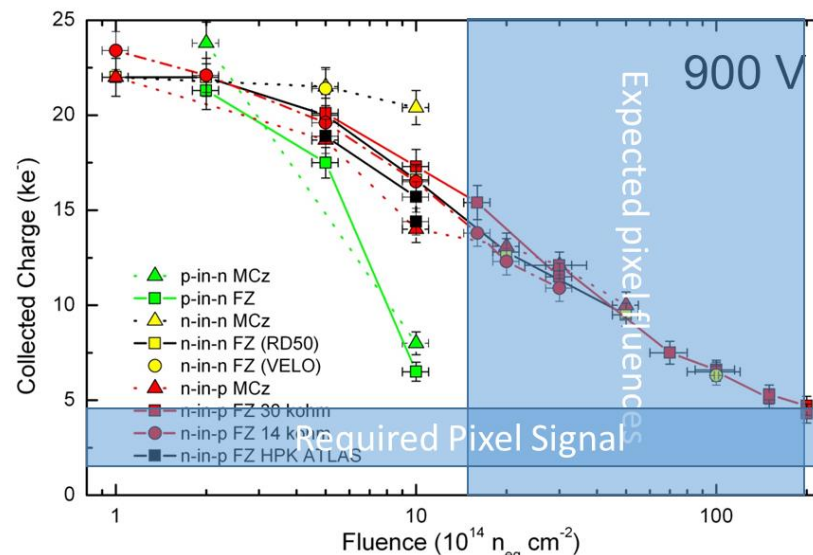
7<sup>th</sup> Technology & Instrumentation in Particle Physics Conference (TIPP2026)

2<sup>nd</sup>-6<sup>th</sup> February 2026

- Tracking detectors measure position and momentum of charged particles
  - Transverse momentum ( $p_T$ ) - curvature
  - Impact parameter ( $d_0$ ),  $z_0$  - distances of closest approach in the x-y, z planes
  - $\phi$  and  $\eta$  - angle of track in x-y, z planes
- ITk completely replaces current ID for HL-LHC
  - Factor of  $\sim 10$  larger fluence
    - Increases segmentation by factor of 4-8 (low occupancy  $< 1\%$ )
    - Radiation hardness (up to  $2 \times 10^{16} n_{eq}/cm^2$ )
      - Equivalent of 50 mins in a TRIGA Reactor
  - 178 m<sup>2</sup> of silicon in the combined system
    - Factor of 2.7 larger than current ATLAS
  - Extends the tracker pseudorapidity ( $|\eta|=2.5 \rightarrow 4$ )
  - Similar tracking performance to ID with increased pile-up (60  $\rightarrow$  200)
  - Faster electronics and larger data throughput to maintain and add to triggering opportunities (100 kHz  $\rightarrow$  1 MHz)

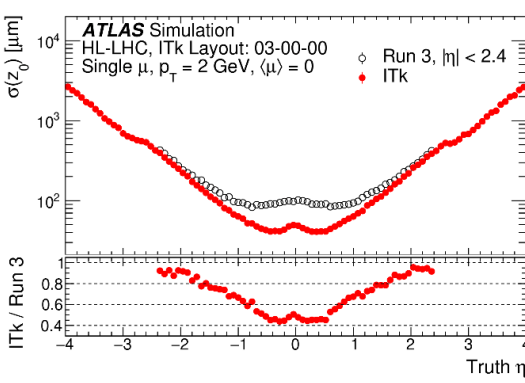
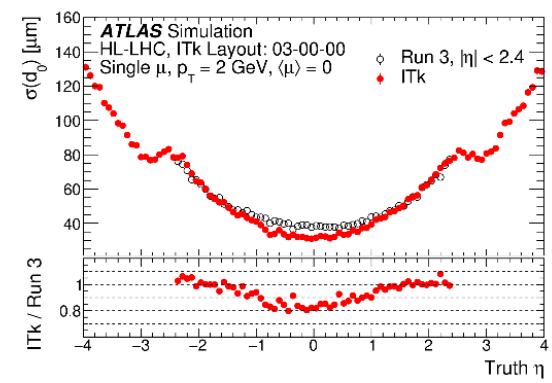
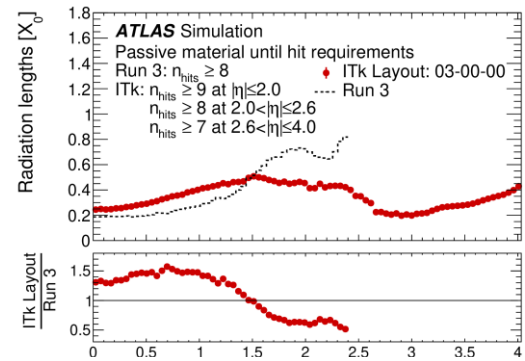
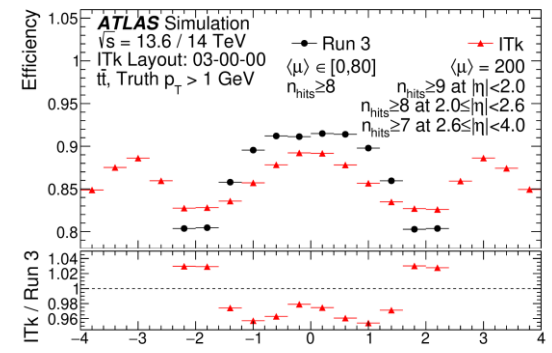
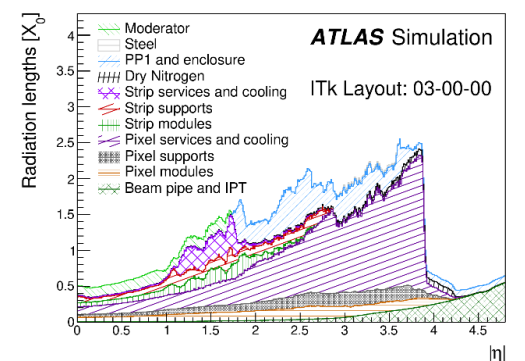
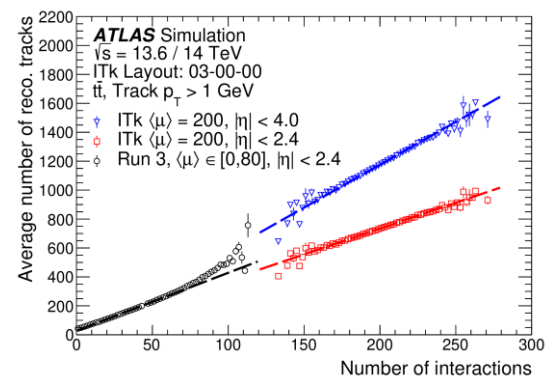


- n-in-p and 3d sensors (RD50)
- Advanced ASICs (GF 130 nm, TSMC 65 nm-RD53) with SEE hardening
  - Triplication + verification
- Carbon fiber support structures, multiplexed services and manifolded CO<sub>2</sub> cooling
  - Serial powering, DC-DC converters



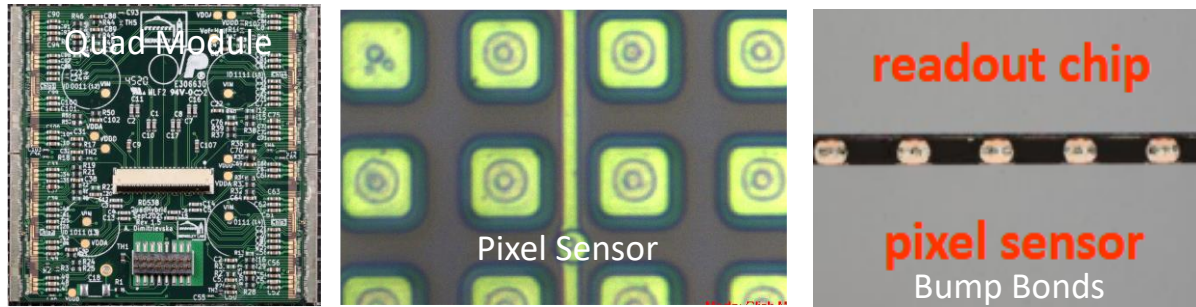
- Excellent track finding at very large pile-up
  - At least 9 silicon hits result in stable track finding to over 250 pile-up interaction
- Minimized material increase in the central region (up to  $|\eta| < 1.5$ ) while reducing material beyond
  - Similar tracking efficiency to current ATLAS up to  $|\eta| < 1.5$  and new tracking capabilities to  $|\eta| < 4$
- Impact parameter improved by finer segmented inner pixel layer ( $25 \times 100 \mu\text{m}^2$ ) at a lower radius
- $Z_0$  improved by finer segmentation of the pixel layers

ATLAS Collaboration, "Expected tracking performance of the ATLAS Inner Tracker at the High-Luminosity LHC", JINST 20 (Feb 2025) P02018 [paper](#)

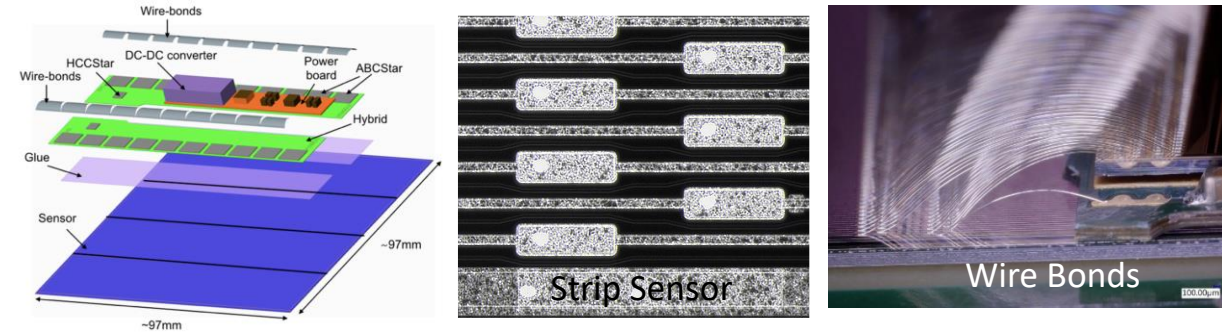


## Smallest Unit Sensitive to Charged Particles

### Pixels



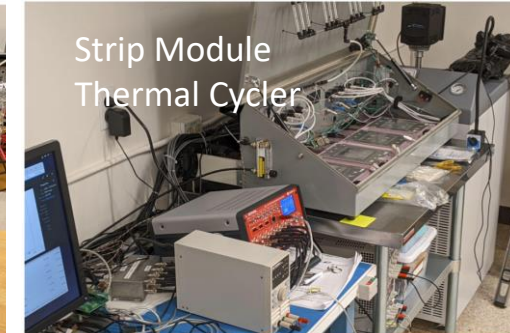
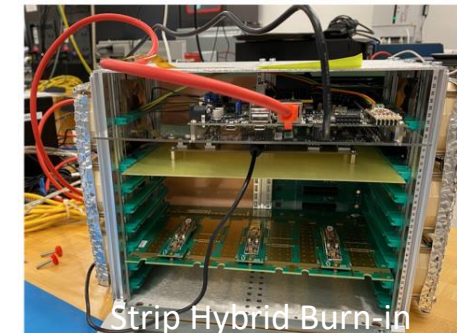
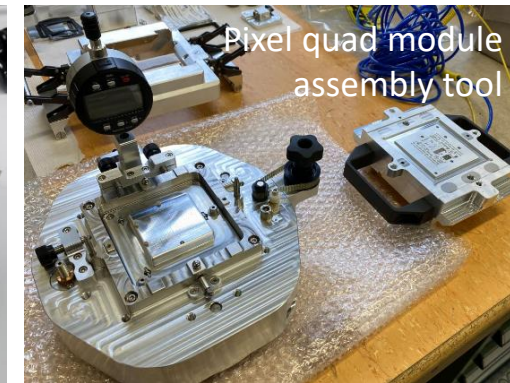
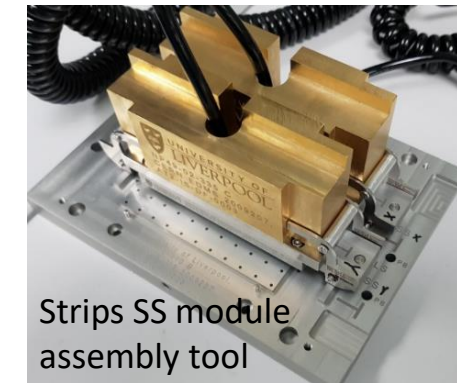
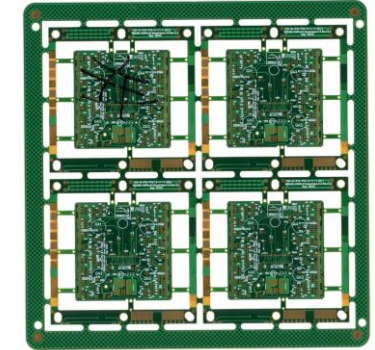
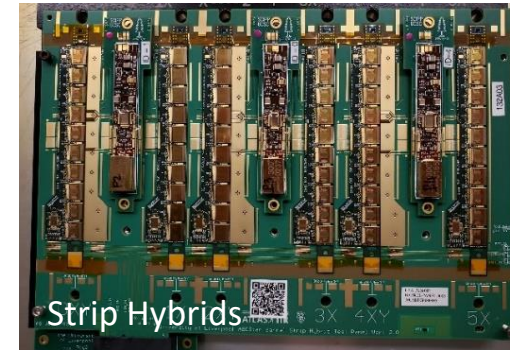
### Strips



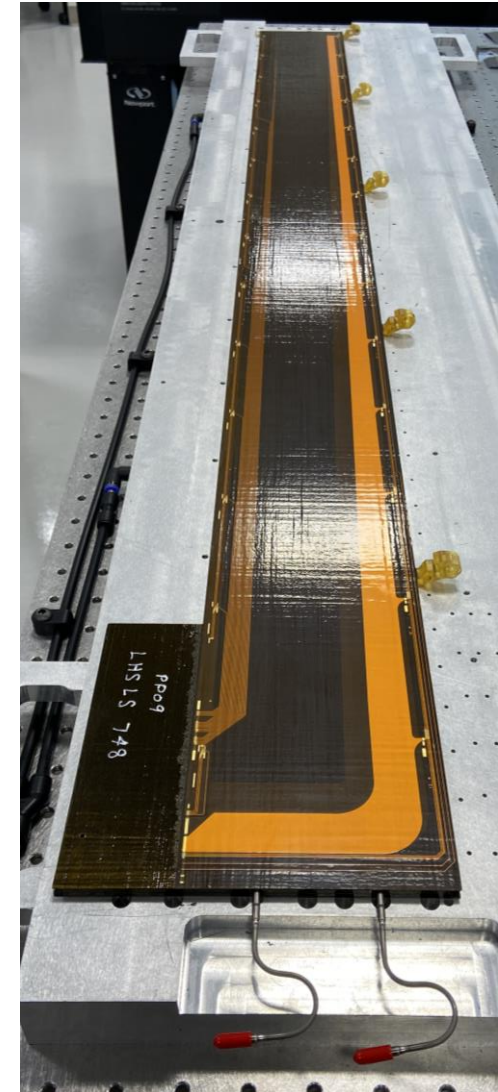
- Sensor: Sensitive elements (nearly) square
  - $50 \times 50 \mu\text{m}^2$  (some  $25 \times 100 \mu\text{m}^2$ )
- Bare Module: 4 pixel readout chips (ITkPixV2) bump bonded to sensor
- Module: Two-layer hybrid flex glued onto back of sensor and wire bonded to readout ASICs
- Serial power control (SHUNT-LDO) built into ITKPixV2
- Nearest to beam where finest segmentation needed to separate tracks
  - Drives  $d_0$  and  $z_0$  resolutions

- Sensor: Sensitive elements long and narrow
  - $75.5 \mu\text{m} \times 2\text{-}6 \text{ cm}$
- Module:
  - Four-layer hybrid(s) flex glued to sensor
    - 6-12 FE chips (ABCStar) per hybrid wire bonded to sensor (4 row bonding)
    - 0-2 control and data aggregator chip (HCCStar) per hybrid
  - Power board with DC-DC converter (bPOL12V) and monitoring/control chip (AMACStar) glued to sensor
- Covers larger area, further from beam
  - Drives momentum and  $\eta$  resolutions

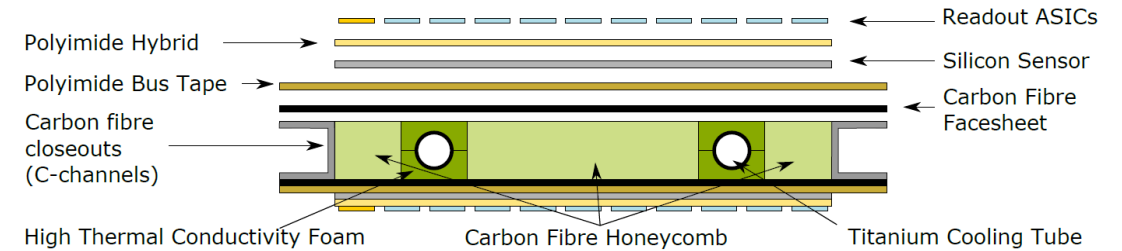
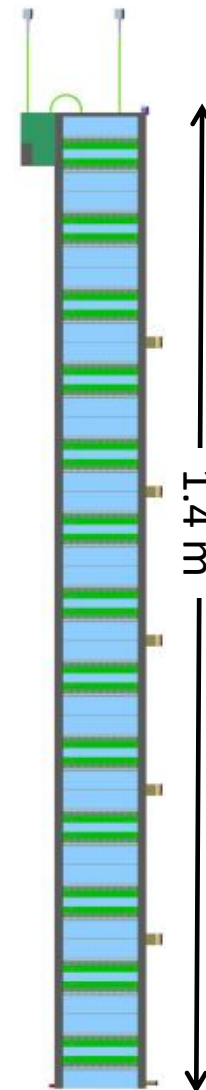
- Large number of modules necessitates early focus on manufacturability and mass testing
  - 8372 (pixels), 17888 (strips)
- Bare flexes use “relaxed” design rules
  - 100  $\mu\text{m}$  track and gap (pixels & strips)
  - Allows for manufacturing by many vendors
- Assembly uses relatively loose, in-plane tolerances
  - Vacuum tools aligned by pins
  - Used at 20/22 module productions site (pixels/strips)
- Hybrids produced in panels for ease of testing and assembly
  - 2 $\times$ 2 panel pixels; 3 $\times$ 7 panel strips
- Test systems designed for multiple units
  - 6 $\times$ 8 strips hybrids; 4-5 strips modules



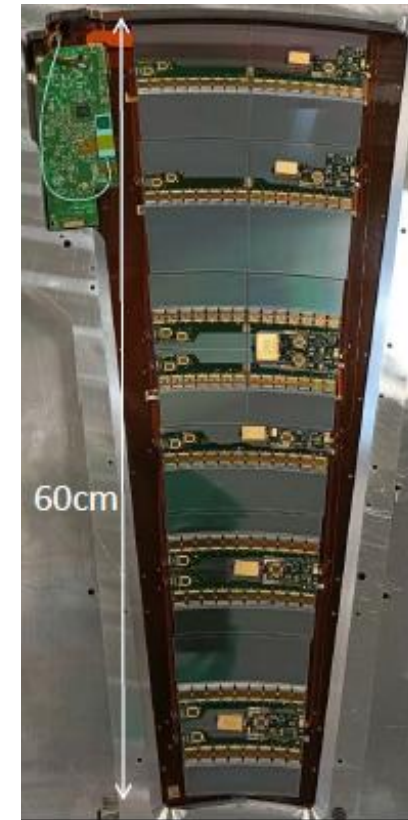
- Bus tapes connects strip modules to power, clock and command
  - 2-layer copper Kapton flex circuit
- During the design stage, barrel stave length increased from 12 to 14 modules
  - Moves service material in gap between barrel to end cap from  $|\eta|$  of 1 to 1.2
- Necessitates 1.4 m long bus tape with a 100  $\mu\text{m}$  track & gap
  - Precise etching necessary to control impedance ( $Z_0 = 100 \Omega$ )
- The length of the bus tapes is slightly longer than standard presses at suppliers
  - Then company which made prototypes withdrew for commercial reasons
  - Undertook a year's long search to find 2nd commercial manufacturer
    - Most lack experience and had difficulty meeting our requirements
  - Ultimately, CERN Micro Pattern Technology Laboratory worked with us to develop and produce tapes
- Lesson: Stay within industry capabilities when making design changes



- Strips local supports provide cooling, mechanical support and electrical services to a number of modules
  - Barrel Staves: long and skinny rectangles
  - End Cap Petals: trapezoidal geometry allows for radial strips
    - Different strip lengths are used to balance occupancy
- Both designs maximize cooling power with minimum material

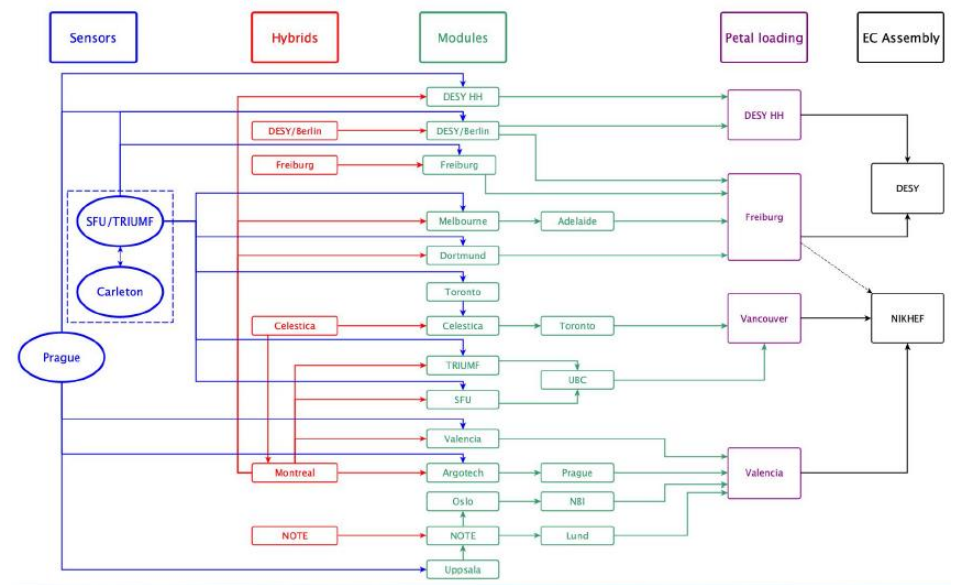
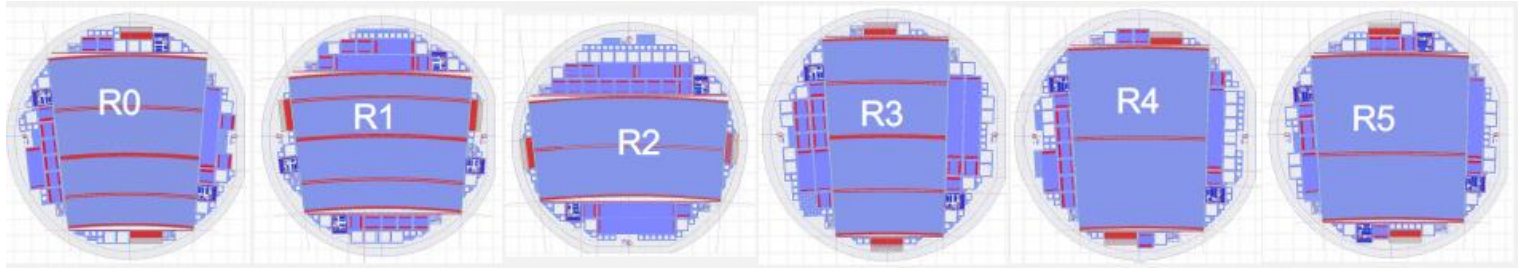
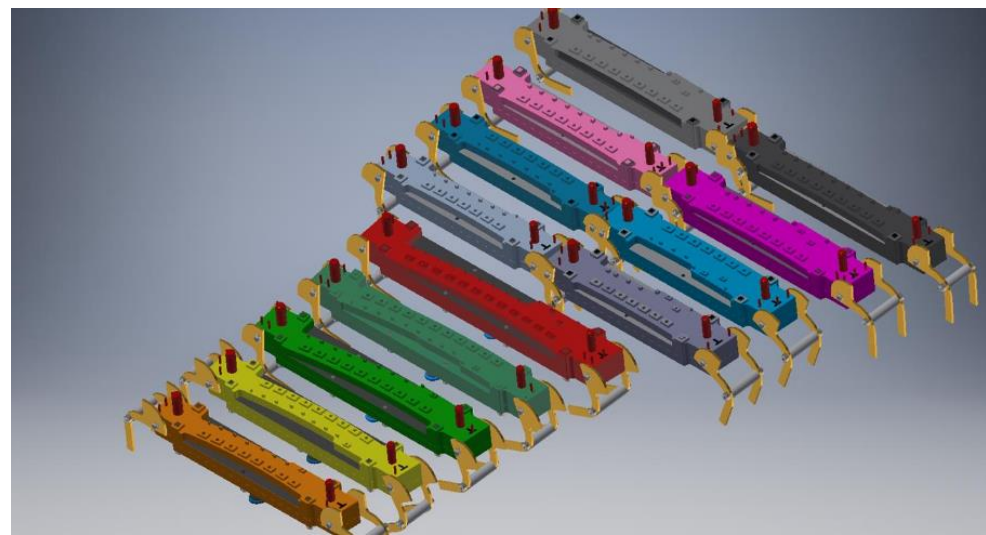


	Staves	Petals
Modules Per Side	14	9
Module Types	2	9
Hybrids Per Module	1 (B2,3) 2 (B0,1)	1 (R2,4,5) 2 (R0,1,3)
Hybrid Types	2	13

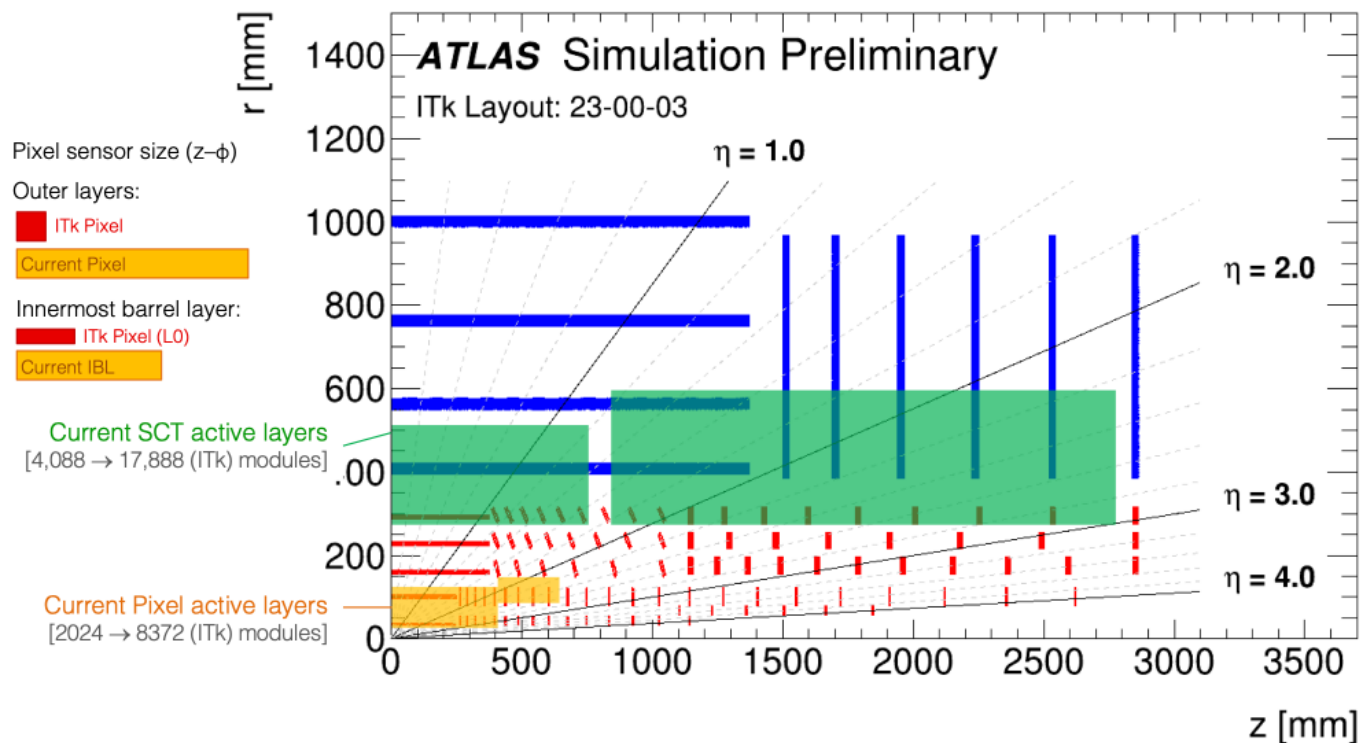


# Strip End Cap Modules

- The trapezoidal geometry results in 6 sensor, 13 hybrid, and 9 module types
  - To finish a petal, all the components must be available at the same time
- Each variant requires custom tools for assembly, bonding, and testing which must be provided to multiple sites
  - Limits the ability to shift production between sites
- Results in complex part flow through multiple countries
- Any technical problem requiring a modification had to be propagated through all design variants and tools
  - Statistics to see issues are divided across all the variants

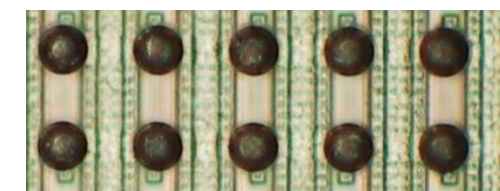
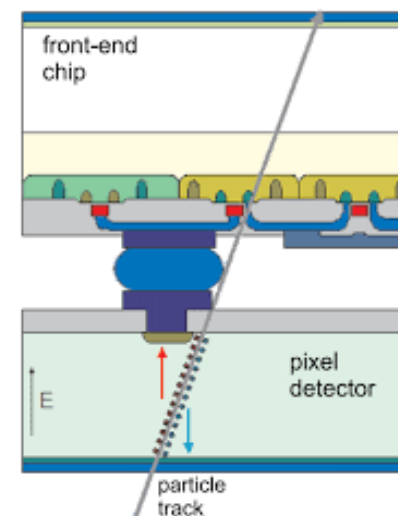


Largest hybrid pixel detector ever built with finer segmentation and thinner sensors/ASICs

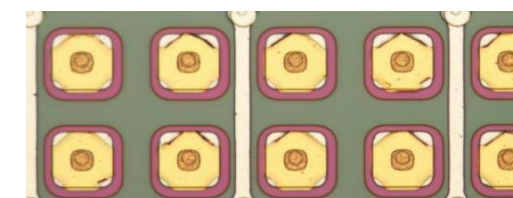


	ID	ITk
# Modules	2000	8372
Area (m <sup>2</sup> )	1.6	13
Channels (M)	92	1400

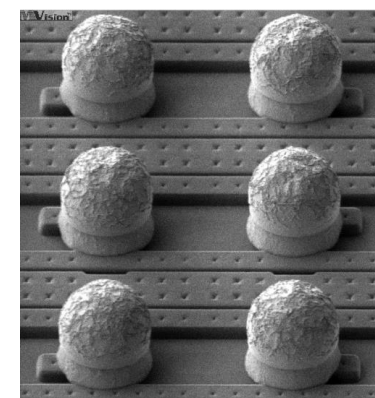
- In hybridization: pixel chips and sensors are joined together
- Design limits potential hybridization industrial partners
  - Limited market for thinned, bump bonded devices with 50x50  $\mu\text{m}^2$  pitch
- ATLAS worked with 3 industrial partners for over a decade to start production in 2<sup>nd</sup> half of 2025
  - Multiple dicing, bump metallization & carry-wafer options explored at each vendor to find a working solution
    - Difficult due to reticle-sized ASICs and thick metal layers in TSMC 65 nm
    - Made even more challenging with the 5 different sensor varieties
- Two collaborators are also developing in-house bump bonding capabilities
- 9 combinations of sensor, bump metallization, and hybridization vendor
- Early work allowed for our large 5-layer pixel system
  - Over-constrained pixel only track finding with 1 allowed missing layer
    - Improves tracking purity



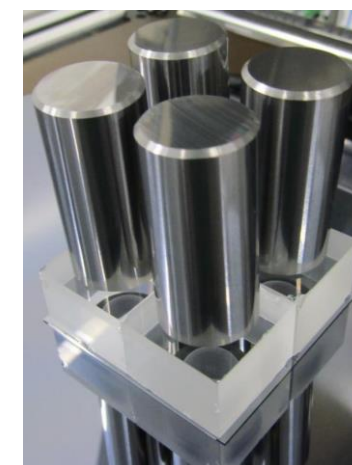
ITKPixV2 w/SnAg bumps



Sensor w/ UBM

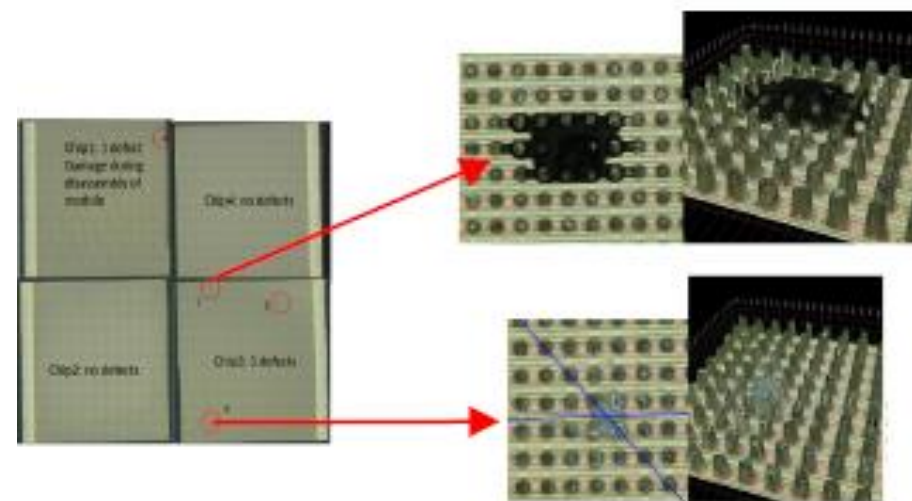
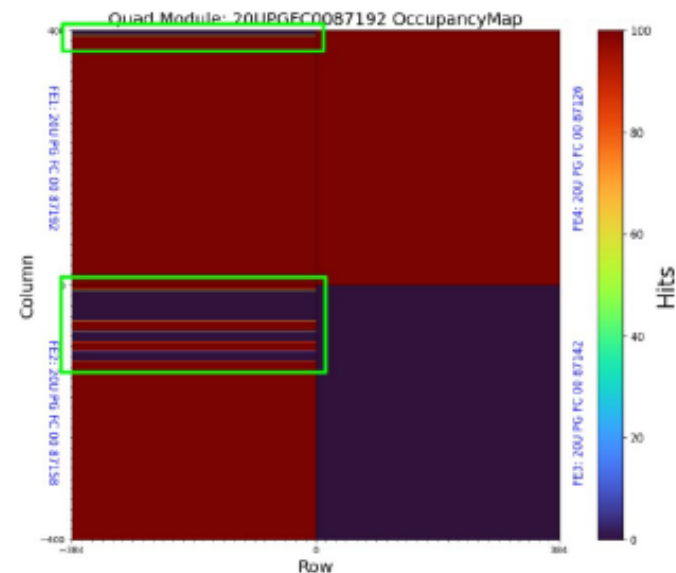


ASIC bump metallization



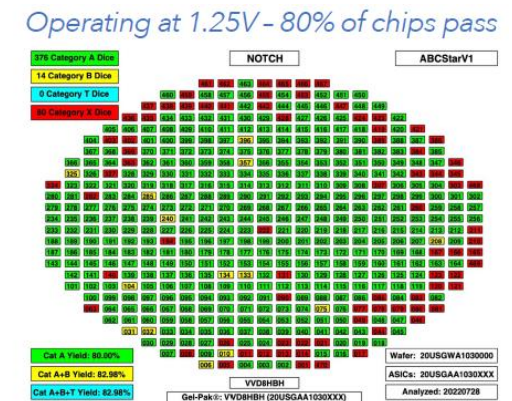
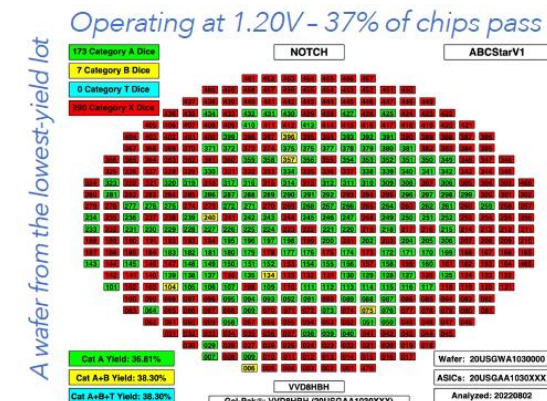
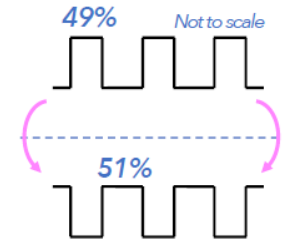
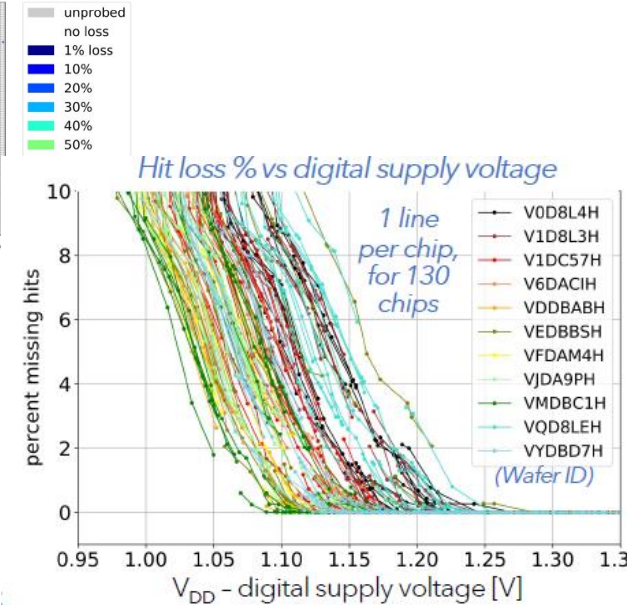
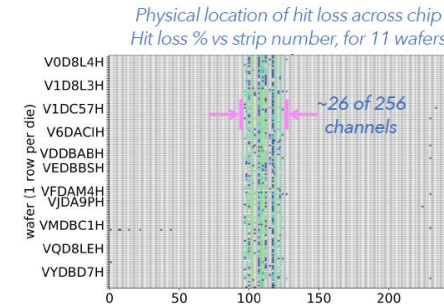
Advafab flip chip bonding

- In pre-production, a large fraction of chips (8%) needed a whole core-column disabled for the chip to communicate (2% of pixels per column)
  - After much study, the dominant sources found to be debris in bump bond grid which damages the ASIC when bump bonded & damage to the periphery during dicing
    - Finding solution was not made easier with 9 combinations of sensor- bump metallization - dicing- bump bumping vendor
- With changes in cleaning and dicing, rates have been reduced by a factor of 2-4
- Lessons Learned
  - Unexpected surprises happen when you increase segmentation, make devices thinner
  - Investigate how to improve fault tolerance for future digital matrices

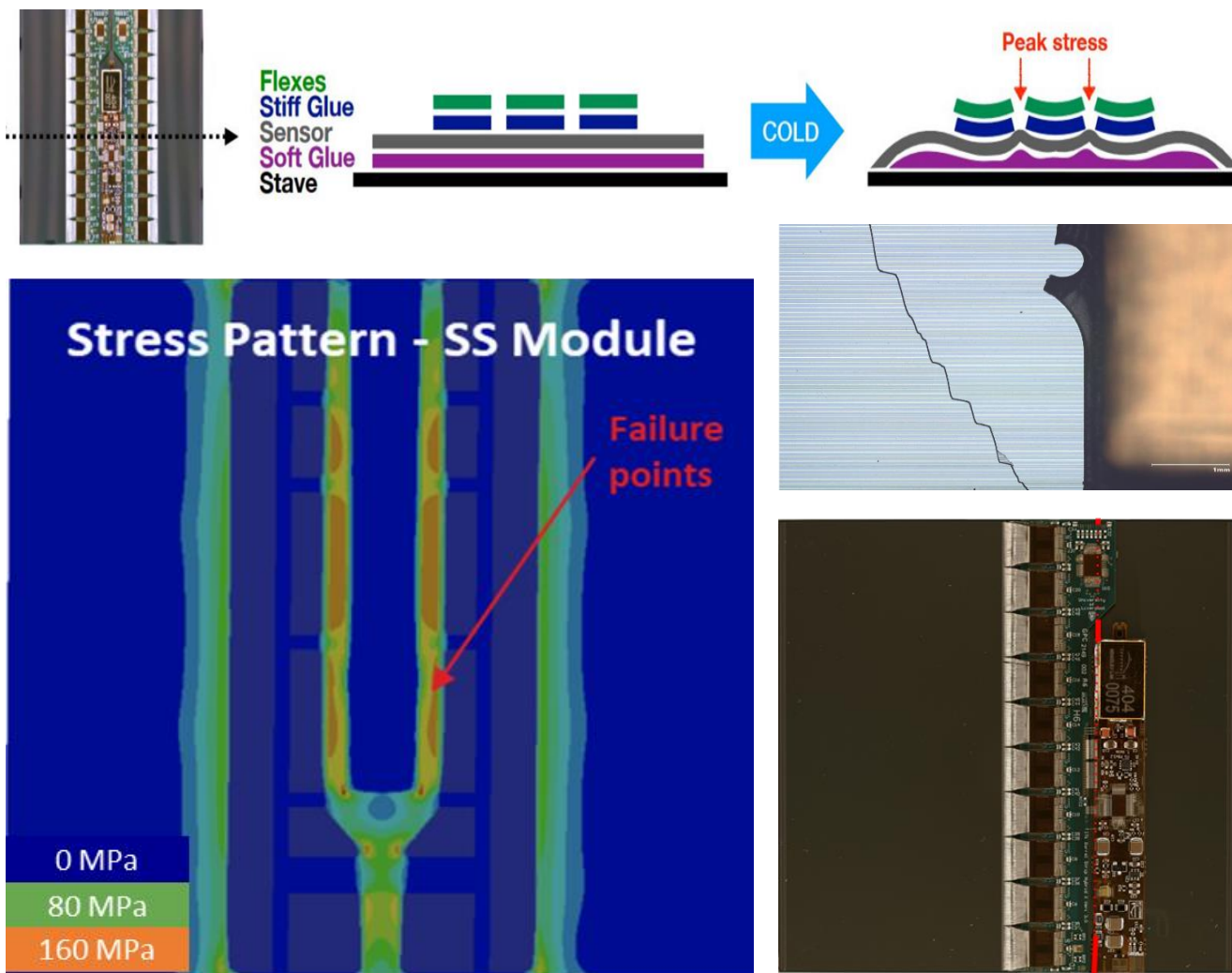


# ABCStar SRAM

- 1/3<sup>rd</sup> through production, batch with 31% yield, typical 86%
  - Hits were lost due to a setup time problem in the SRAM
    - Batch was in the slower transistor corner within foundry rules
- SRAM block had been used in multiple previous ASICs
  - Timing models of block 10 years old at the time of the ABCStar
    - Chip tools had wrong specs; put in too little buffering
- Solution:
  - Increase the operating voltage inside the ABCStar- faster transistors
  - Invert slightly asymmetric clock (52/48)- more time for setup
- Lesson learned:
  - Fully re-simulate all blocks, even if working in previous chips
  - Pay for “striping” run early from foundry
    - Covers a representative range of process outcomes
    - Costs are modest. At our foundry, 150% of an engineering run
    - Learn yield range early for planning



- Early sensor breakdown ( $<100$  V) seen after testing staves at operational temperatures ( $-35$  to  $-45$  C°)
  - After close visual inspection, hairline cracks were found between hybrid and power board
- Simulation confirmed the source to be the CTE mismatch between copper in PCBs and silicon sensor
  - Concentration of stress when module attached to petal/stave ( $\sim 150$  MPa)
  - Stress less than direct cracking stress ( $\sim 300$  MPa)

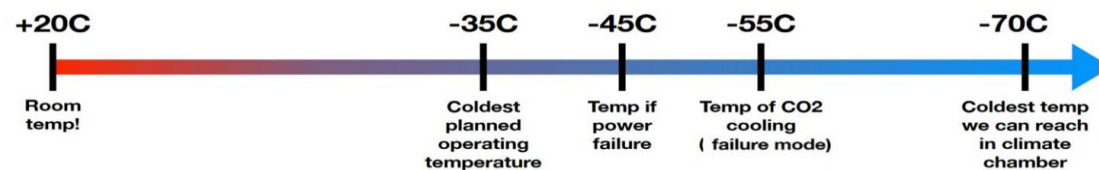
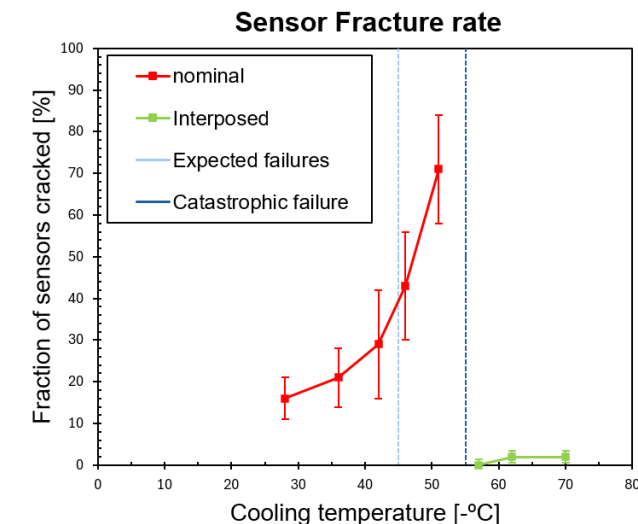
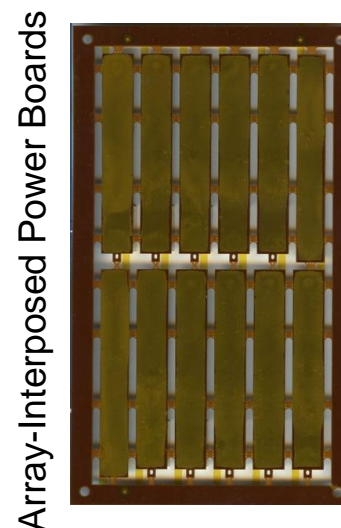
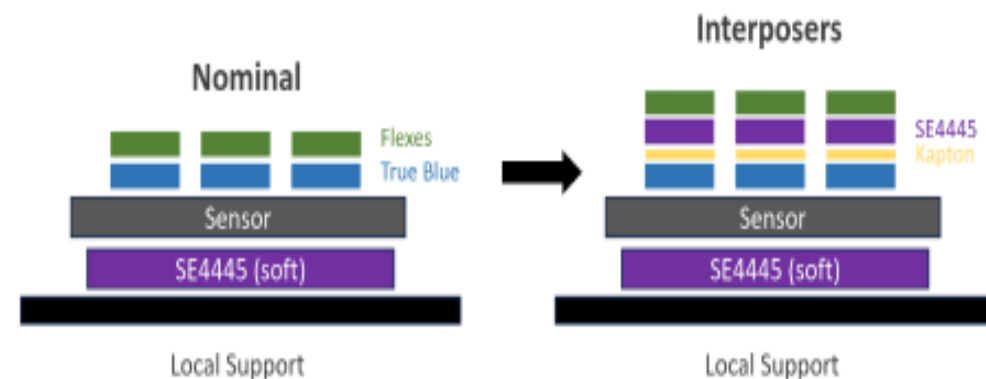


Solid red lines are visible cracks  
Dotted lines connect visible cracks

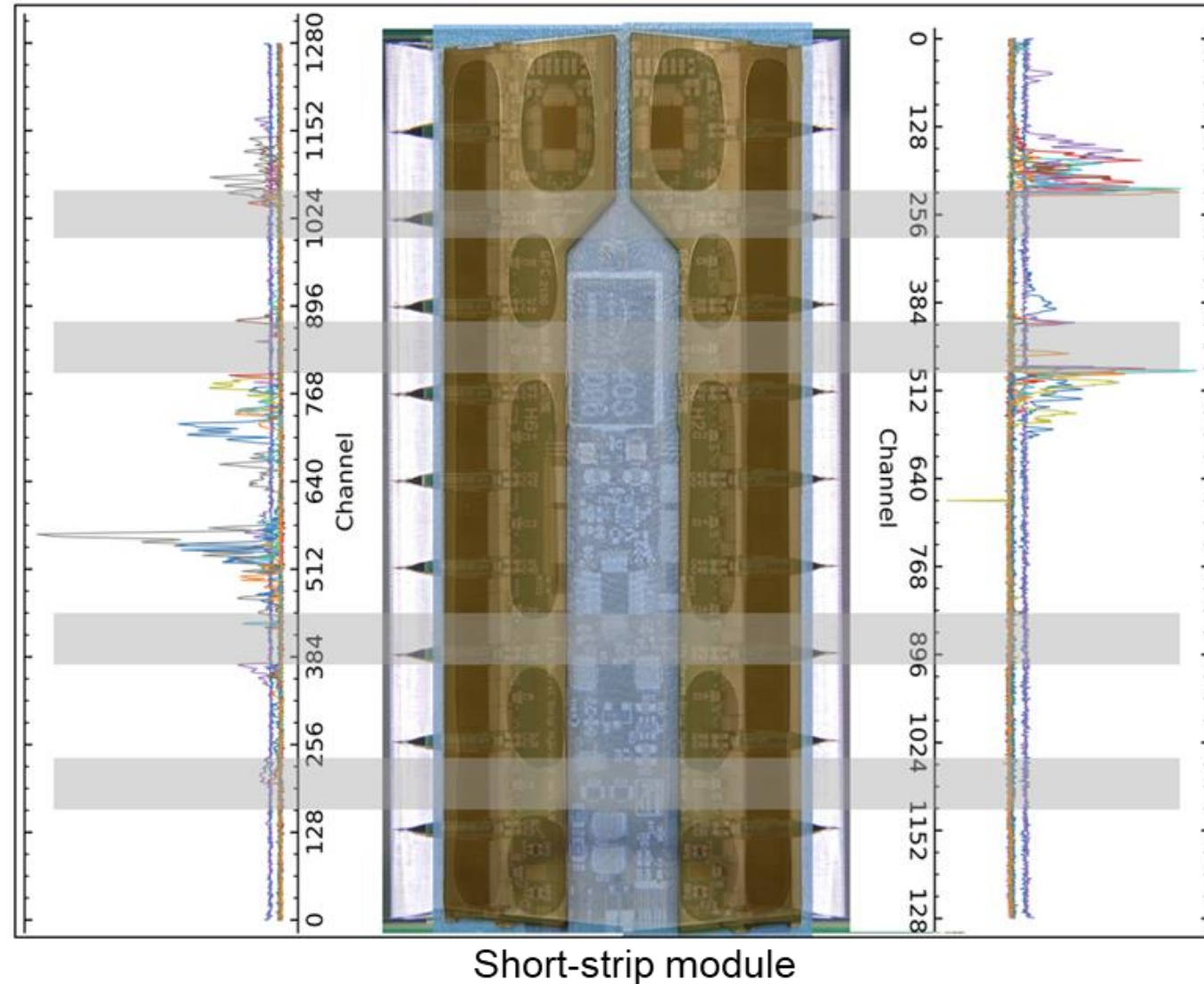
G. Vallone, et. Al. "Investigating Cracks in ATLAS ITk Strips", 12<sup>th</sup> FOTM ([presentation](#))

- Solution was adding a layer of softer silicone (SE4445) between the hybrid/power board and sensor to decouple stress (interposer)
  - Simulation and special strain gauge modules indicate up to 95% reduction in stress
- Fracturing removed at operating conditions (over 15 tested staves)
- Industrialized process to add interposers was developed quickly due to the well-thought-out design of the hybrid and power board panels
- Lessons Learned:
  - Test beyond expected environmental conditions (temperature, dose/fluence) on large objects early in prototyping phase to understand headroom
    - Even if extremely difficult to achieve

A. Fortman, “A new stress-relieving layer in ATLAS ITk strip modules”, NIMA 1081 (Jan 2026) 170896 ([paper](#))

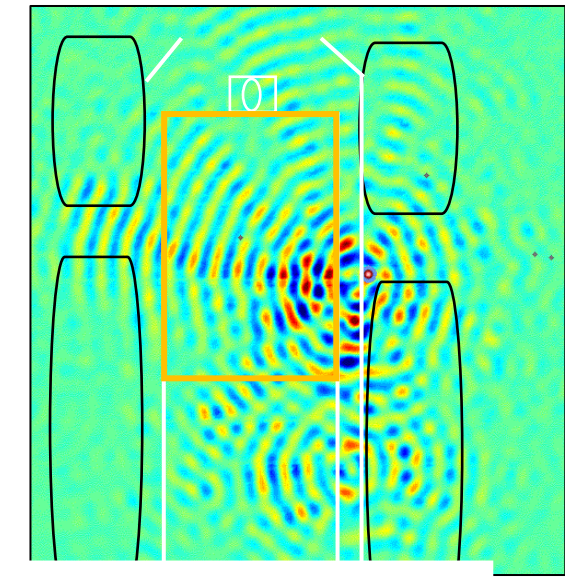


- Vendor for epoxy used for module assembly closed
  - Purchased a reformulation of this epoxy from another vendor
- Upon testing modules with new epoxy at operational temperatures ( $-35\text{ C}^\circ$ ), large sections of channel were seen with extremely elevated noise
  - Noise locations were correlated with position of glue lines under hybrid

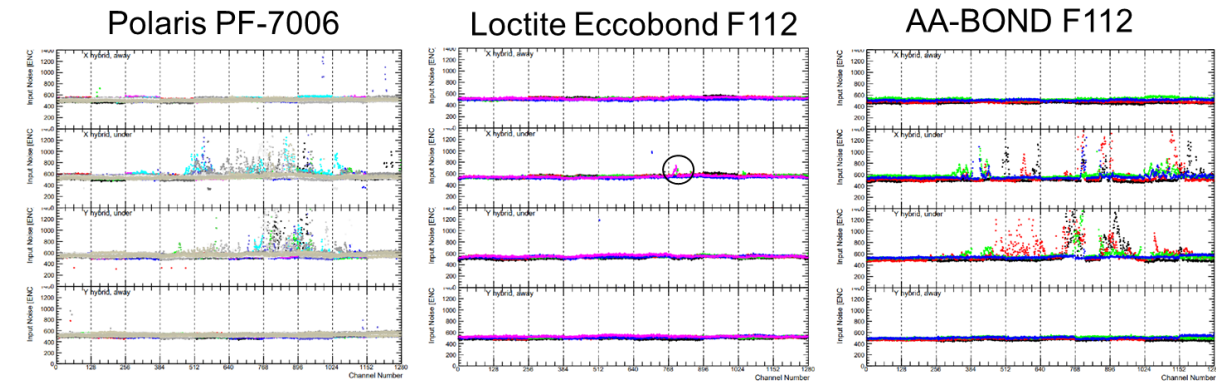
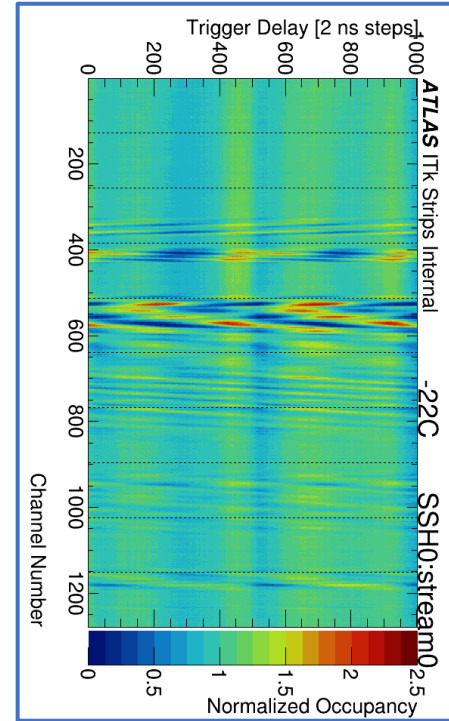
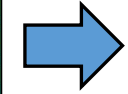


# Cold Noise

- Vibrating capacitors in the DC-DC converter circuit generate 100 pm-scale vibrations in the sensor which is turned into electrical noise at glue interface
  - Noise time profile consistent with Lamb waves
  - Never able to establish coupling mechanism
    - Nearly identical epoxies gave very different noise response
- Changing glues reduced cold noise greatly
  - Interposers removed cold noise completely
- Lessons learned
  - Adhesives are mysterious (chemistry!!)
    - Qualify multiple options if possible
  - Avoid niche vendors, if possible
  - Test beyond operating conditions early and repeat them after any change



Scan from below sensor @ -60C



Ian Dyckes/Matthew Kurth, “How the discovery of Cold Noise delayed the production of ATLAS ITk strip tracker modules by a year”, TWEPP2023 ([presentation](#))

As chips become lower voltage/higher current devices with remote power supplies, on-module power services are necessary

## Serial Powering (Pixels)

- O(1000) serial powering power chains with up to 14 modules each
- Current flows from one module to next
  - Reduces number of supply lines, less material
  - Chips on a module powered in parallel
- Current required to be more than the module with largest draw
  - In chip Shunt Low Drop Output (Shunt-LDO) power regulator
    - Takes constant input current and dynamically adjust shunt current to maintain stable on-chip voltages
- Complications
  - System fault tolerance is not trivial
  - Each module on different potential → AC coupling of data lines
  - HV reduces down the chain by the LV voltage drop per module

## DC-DC Converter (bPOL12V)

- Rad-hard buck converter (11 V to 1.5 V)
  - 72% efficiency
  - Custom flat air-core coil (in magnetic field)
- Cable plant heat losses go as  $I^2R$ 
  - Reduced by factor of 28
    - $(\text{Conversion ratio} \times \text{efficiency})^2$
- Complications
  - DC-DC convertors are noisy (high frequency switching)
    - Development required for light-weight EM shielding and for conducted noise reduction.
  - Can not measure V or I per module at power supply
    - Developed AMACStar for monitoring

As chips become lower voltage/higher current devices with remote power supplies, on-module power services are

## Serial Powering (Pixels)

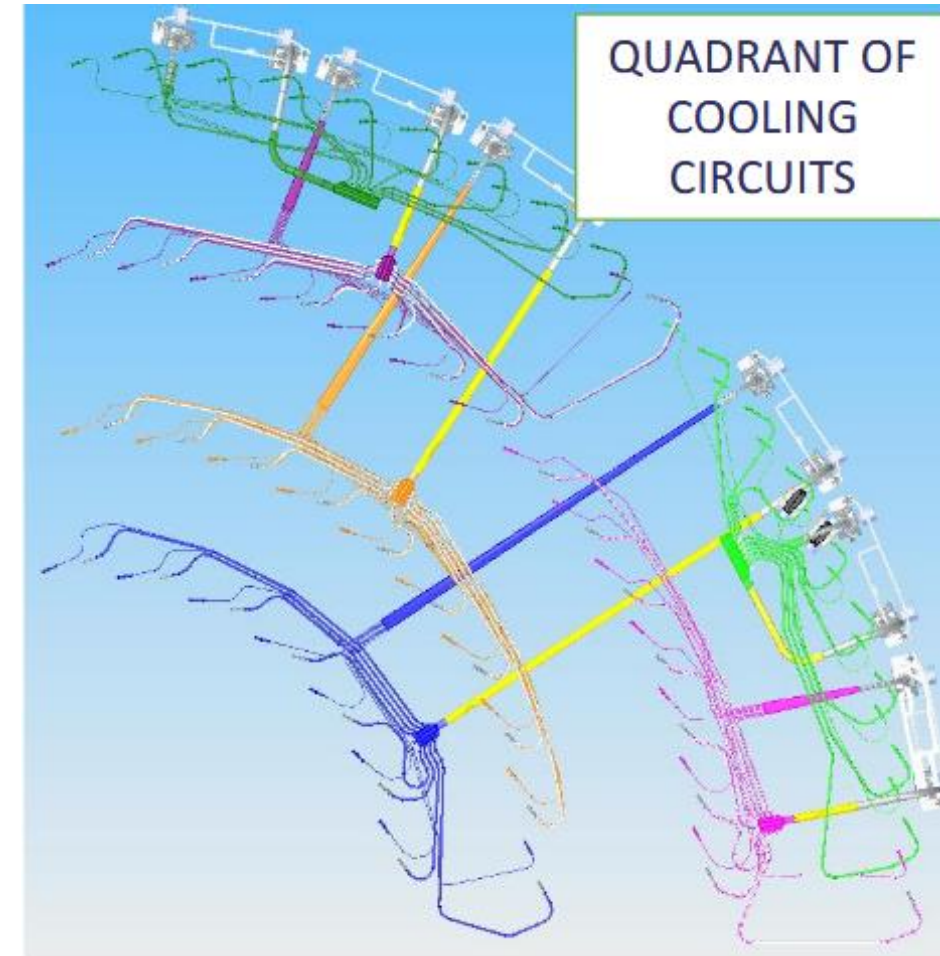
- O(1000) serial powering power chains with up to 14 modules each
- Current flows from one module to next
  - Reduces number of supply lines, less material
  - Chips on a module powered in parallel
- Current required to be more than the module draw
  - In chip Shunt Low Drop Output regulator
    - Takes constant current to just shunt
- Complications
  - Not trivial
  - Different potential → AC coupling of data
  - Losses down the chain by the LV voltage drop per module

## DC-DC Converters

- Rad-hard (e.g. 1.5 V)
- Inductor (in magnetic field)
- Heat losses go as  $I^2R$ 
  - Reduced by factor of 28
  - (Conversion ratio × efficiency)<sup>2</sup>
- Complications
  - DC-DC converters are noisy (high frequency switching)
    - Development required for light-weight EM shielding and for conducted noise reduction.
  - Can not measure V or I per module at power supply
    - Developed AMACStar for monitoring

As allowed material for services and cooling is decreasing, these power techniques will be even more important for the next generation of experiments

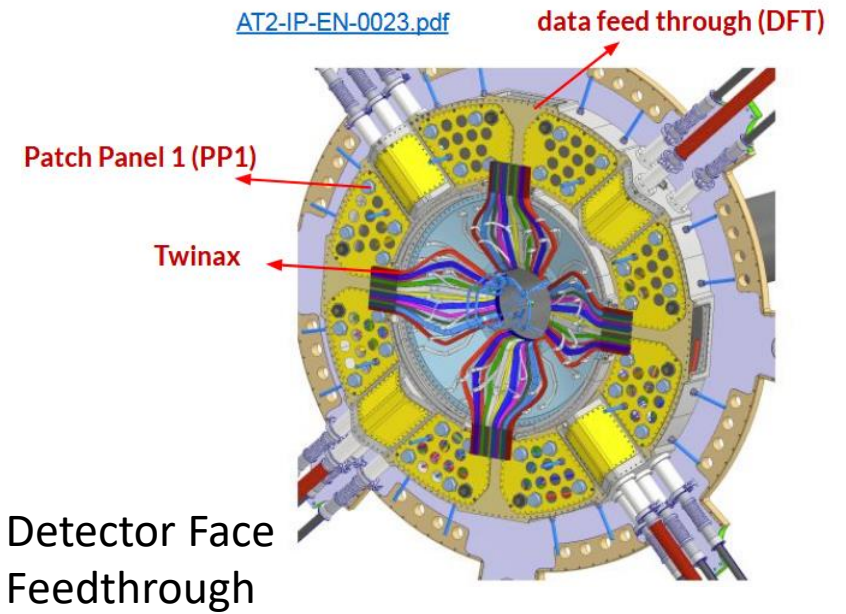
- To minimize material, 0.16 mm thick wall Titanium tubes used for cooling loops within local supports
- Capillaries balance the flow in parallel branches of system
  - To further minimize material, thin-walled Ti capillaries used as well
- Both have much thinner walls than industry standards
- Pressure drop within capillaries was inconsistent (at the level of  $> 0.5$  bar)
  - Pressure drop scales at  $D^4$
  - Most likely due to organic lubricants during drawing process
- ITk is moving to stainless steel capillaries
  - CMS has had success with these
  - Currently confirming reliable methods to join thin wall Ti to stainless steel
- Lessons learned:
  - Make larger scale tests of devices if materials are not industry standard
  - Reconsider balancing material vs. reliability through industrial experience



- As upgrade go into very congested existing space, power services are multiplexed and cooling services are manifolded
- In the active volume, inner pixel system particularly congested
  - Serial powering reduce the number of power lines
  - Up to 6m long custom data transmission lines at 1.28Gbps
    - Optoelectronics outside detector volume
  - 16 different data and power flexes
  - All 80 on-detector service bundles unique
    - Different lengths and routing paths
    - Basically impossible to be made in industry
- Services for next generation vertexing systems will be as complex and congested and target lower mass
  - Much R&D will be necessary



Data transmission connector



Detector Face Feedthrough

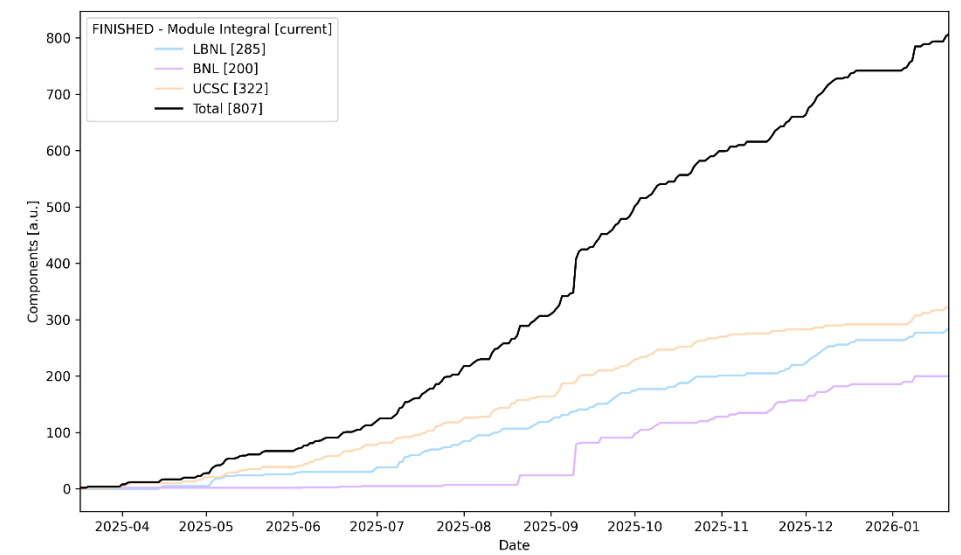
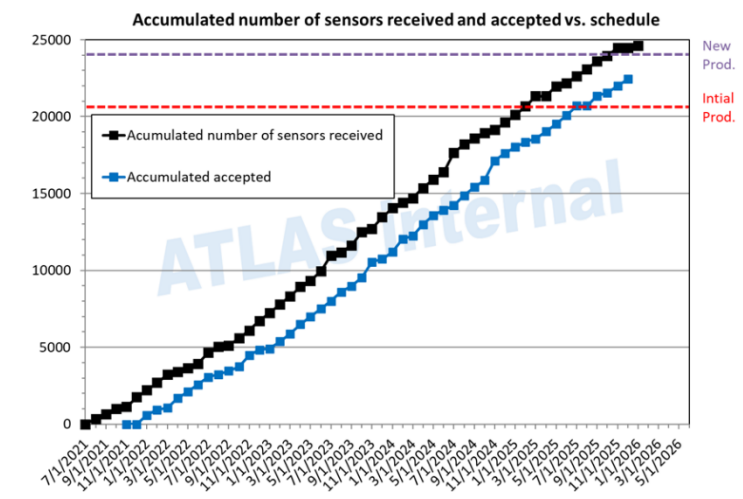
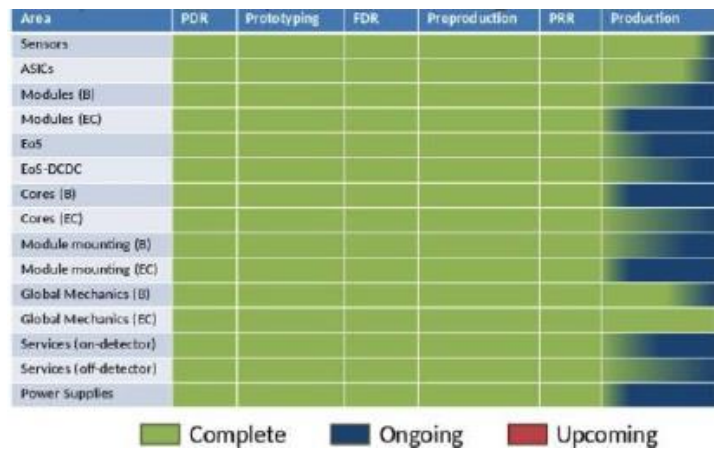


Inner System Service Mockup



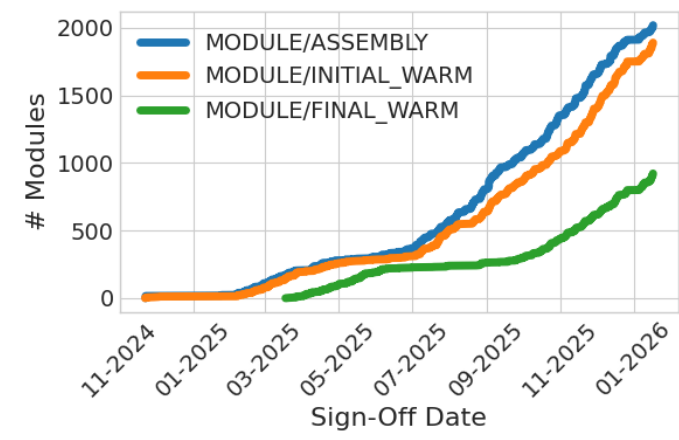
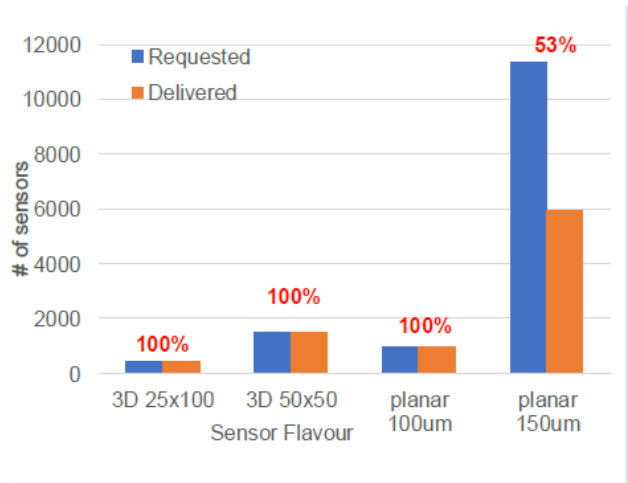
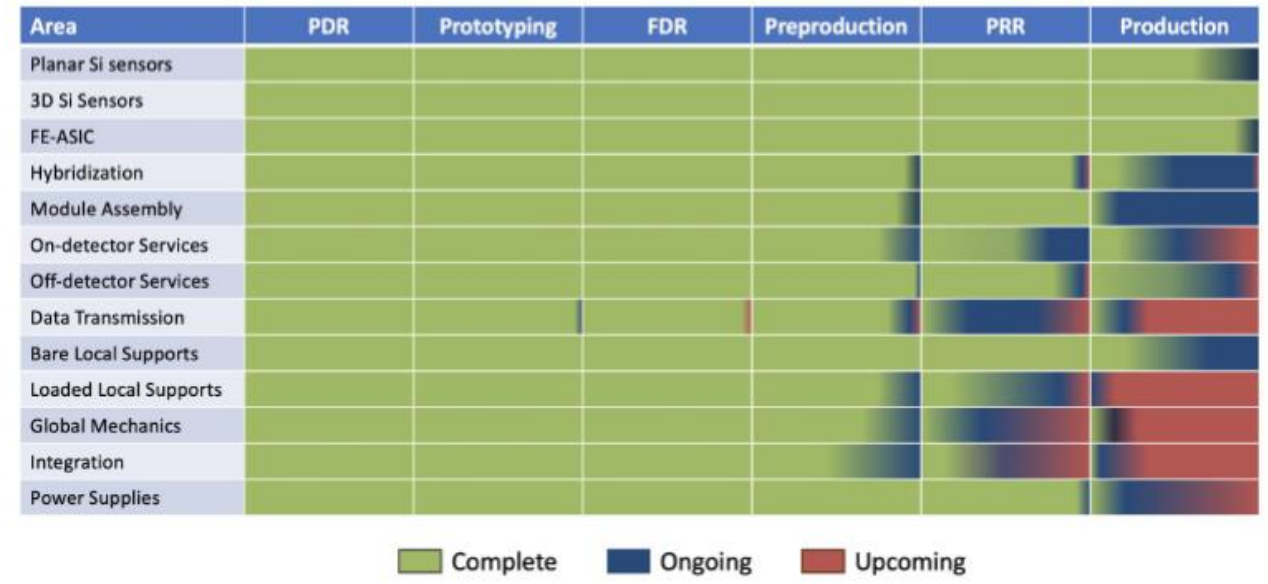
# Strip Production Progress

- All components in production
  - Sensors, ASIC, petal tape complete
  - Petal cores: 40%
  - Modules: 10%
- Module production started in all clusters
  - Yields: ~90% and improving
  - Demonstrated peak rates; currently limited by components
- First installable staves and petals completed



# Pixel Production Progress

- Most components in production or transitioning into production
  - Sensors: ~65% planar, 100% 3d
  - ASIC: 100%
  - Hybridization: 0-30% per vendor
- All module clusters are in production
  - Rate set by component availability
  - Good (~80%) yield including core-column modules



- Planning
  - It will always cost more
  - It will always take more time
  - It will always have more material than planned
  - There will always be large unexpected problems
  - You will always be asked to accelerate
- Design/Technology Choices
  - Listen to engineers and experienced physicists at design phase, especially about buildability
  - Only take on new technology if it makes project possible or huge gains in performance, cost, schedule
    - Prototype early as realistically as possible beyond planned environment (resources for 10-20% scale of the project)
  - Keep it simple- only take only more variants if huge benefits
  - Design for fault tolerance
    - The detector will not be ideal
  - Make sure service and powering is resourced well
    - It is always much harder than it looks and will be even more crucial for next set of experiments
- Social constraints
  - Profit from young people
    - The project will take longer than planned, you needed their energy and passion
  - Build collaborative atmosphere where people work together

For next electron collider, we need much finer segmentation, much less material

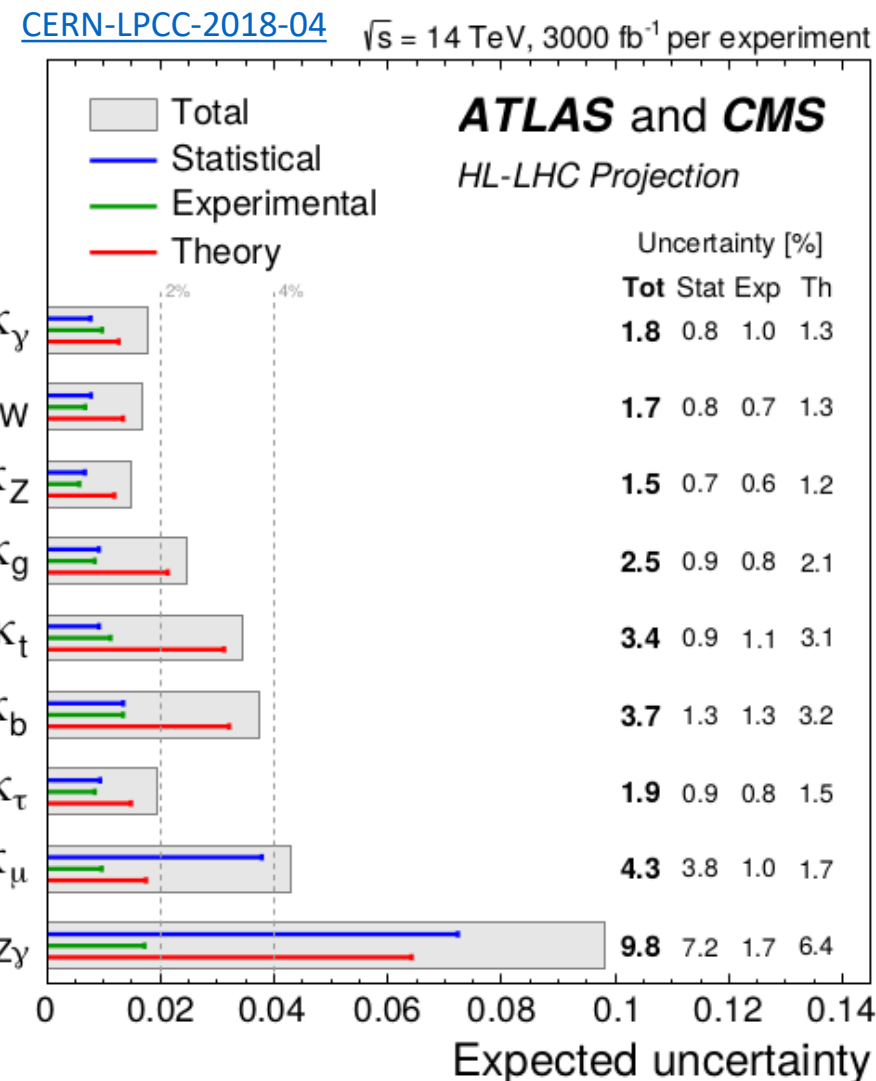
For next hadron collider, we will need another factor of 10 radiation hardness, increased segmentation, larger size,...

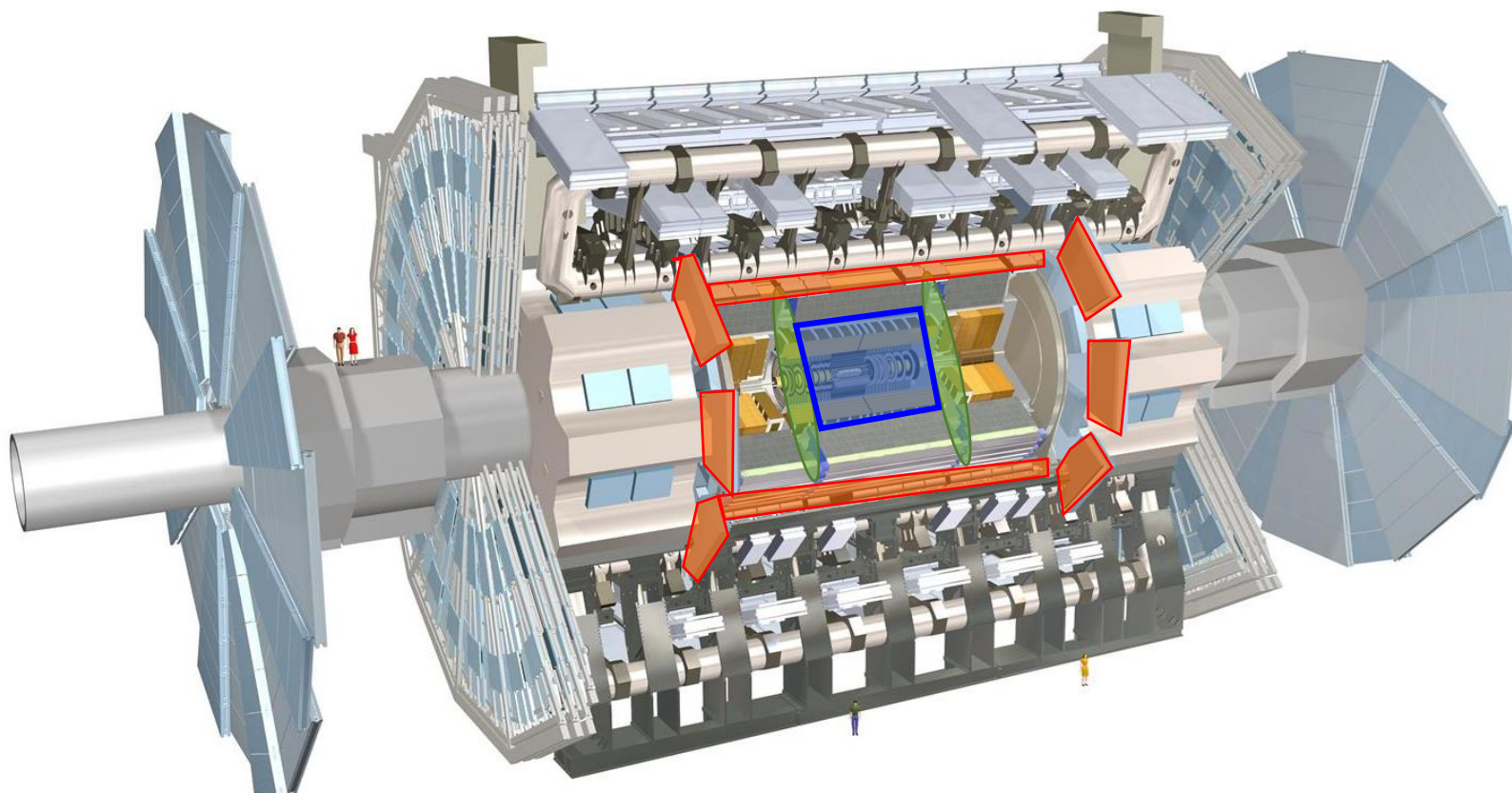
- ITk Strip detector at limits of technology
  - Segmentation
  - Noise
    - Smaller feature size CMOS has worse analogue performance
  - Radiation tolerance
  - Size: Takes a collaboration of 20+ institutes  
3 years to build
- ITk Pixel detector at limits of technology
  - Segmentation (Hybridization)
  - Material (at practical limits of thinning)
  - Radiation tolerance of readout ASICs
  - Cooling (CO<sub>2</sub>)
  - Size: takes world-wide capacity of bump bonding of thinned devices for 2 years

**Need to get started on the next 20-year cycle of technology development**

# BACKUP

- HL-LHC will provide a 10-fold increase in integrated luminosity, enabling a broad program covering all areas of hadron collider physics of ATLAS
  - Installation of upgrade begins in the mid-2020s
  - Operations commence in late-2020's for about ten years
- Highlights include:
  - Measurement of Higgs boson properties: couplings, mass, width, self-coupling
  - Precision electroweak measurements: vector boson scattering, triboson couplings, rare processes
  - Searches for Beyond Standard Model physics: SUSY, dark matter, new resonances, long-lived particles
  - Flavor physics studies: rare bottom and top decays, constraints on CKM
- Recent public studies:
  - Sensitivity to  $H \rightarrow bb$  and  $cc$  in  $VH$  production  
[[ATL-PHYS-PUB-2021-039](#)]
  - Sensitivity to  $WW$  production in photon-photon scattering  
[[ATL-PHYS-PUB-2021-026](#)]





## Upgraded Trigger and Data Acquisition System

- Single Level Trigger with 1 MHz output
- Improved 10 kHz Event Farm

## Electronics Upgrades

- On-detector/off-detector electronics upgrades of LAr Calorimeter, Tile Calorimeter & Muon Detectors
- 40 MHz continuous readout with finer segmentation to trigger

## High Granularity Timing Detector (HGTD)

- Precision time reconstruction (30 ps) with Low-Gain Avalanche Detectors (LGAD)
- Improved pile-up separation and bunch-by-bunch luminosity

## New Muon Chambers

- Inner barrel region with new RPCs, sMDTs, and TGCs
- Improved trigger efficiency/momentum resolution, reduced fake rate

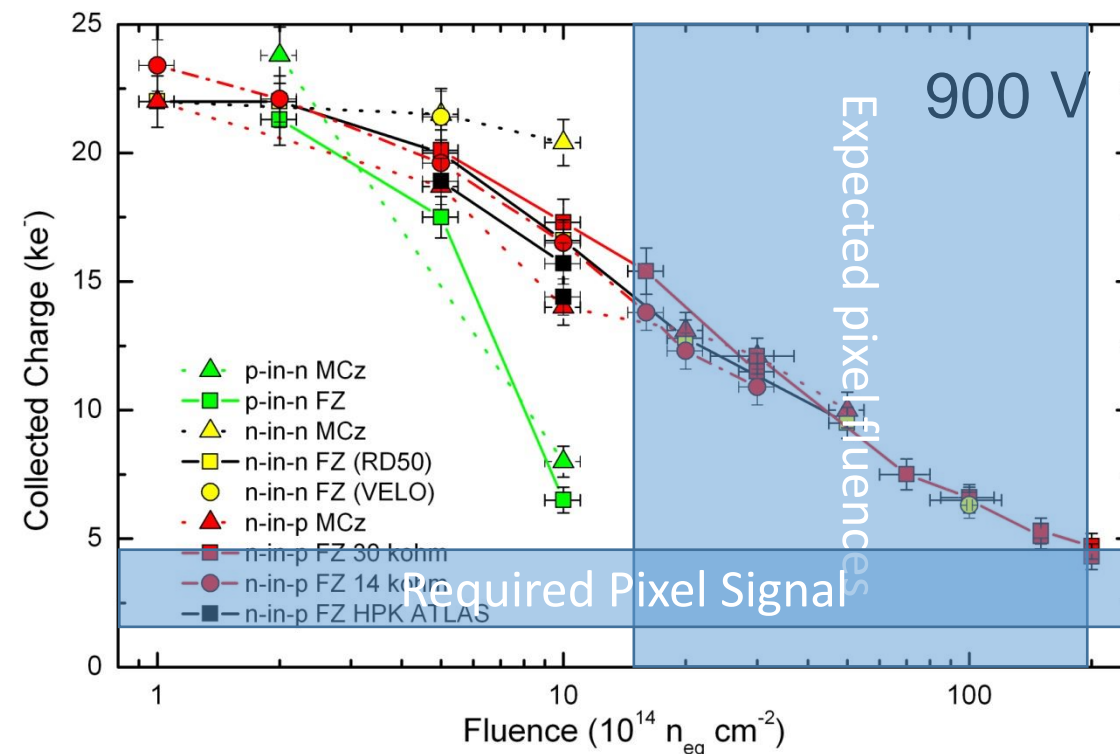
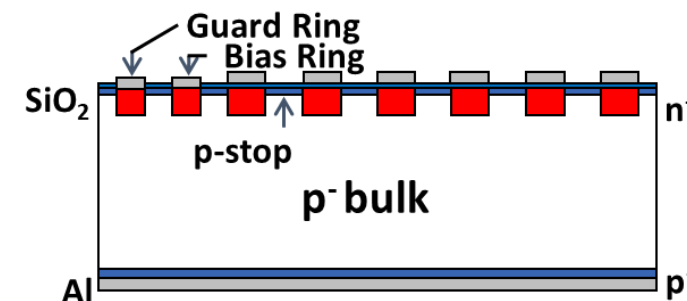
## New Inner Tracking Detector (ITk)

- All silicon with at least 9 layers up to  $|\eta| = 4$
- Less material, finer segmentation

## Additional small upgrades

- Luminosity detectors (1% precision)
- HL-ZDC (Heavy Ion physics)

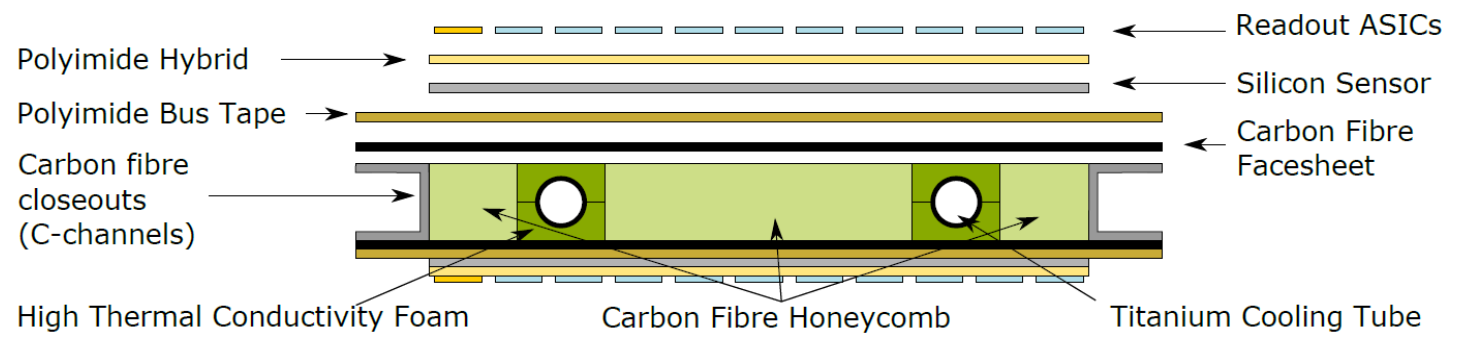
- At the beginning of the proposal for the HL-LHC, it wasn't clear silicon sensors would be radiation hard enough to be used in tracker
  - [RD50](#) collaboration created by CERN to develop required technology
- Bad news:** most developments in adding controlled contaminants and try different silicon crystal growth/processing didn't do a lot
- Good news:** n-type silicon used in current pixel systems turned out to be much more radiation tolerant than first thought
  - Rule of thumb (strips): for efficient tracking signal-to-noise > 8-10:1 required
    - Noise: 500-1000 e<sup>-</sup> (strips)
  - Rule of thumb (pixels): for efficient tracking signal-to-noise > 2.5-4 required
    - Threshold: 600-1200 e<sup>-</sup> (pixels)



- CO<sub>2</sub> cooling made a comeback
  - First in AMS and LHCb VELO
  - And now all silicon-based upgrades
- Minimum temperature of -45 C° (triple point of CO<sub>2</sub>)
- Lightweight structures utilizing thin walled titanium tubes clad in newly developed custom carbon products cools sensors to -15 to -30 C°
  - Pressures up to 143 bar in failure condition
  - Carbon foam, (Thermal) Pyrolytic Graphite



100 kW Demo Plant (Today)



- Hybridization more difficult than current ATLAS
  - More metal in TSMC65 process results in larger bow in heated (>183 C°) bump bonding process
  - ITkPixV2 chip is larger and has 8x higher channel density
- Thinner sensors (100  $\mu\text{m}$ ) was desired to reduce material on inner layers and improve impact parameter resolution
- Very difficult to achieve full bump coverage
  - Reduced area to those with largest impact
  - **Tracking impact??**
- Lessons learned:
  - Understand early in design process where aggressive material results has most impact from simulation with realistic material estimates
  - Consider re-weighing material vs. producibility

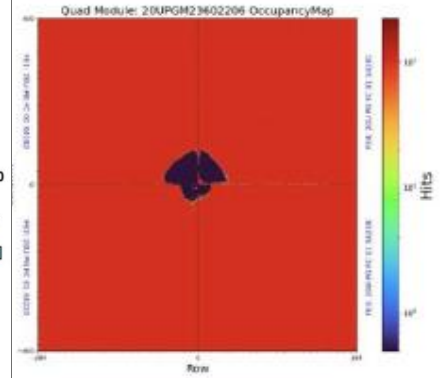
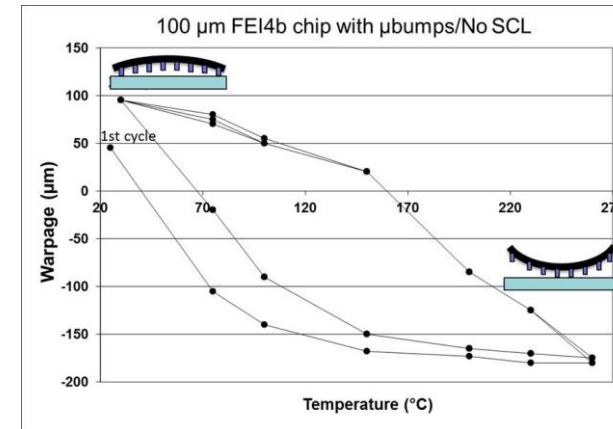
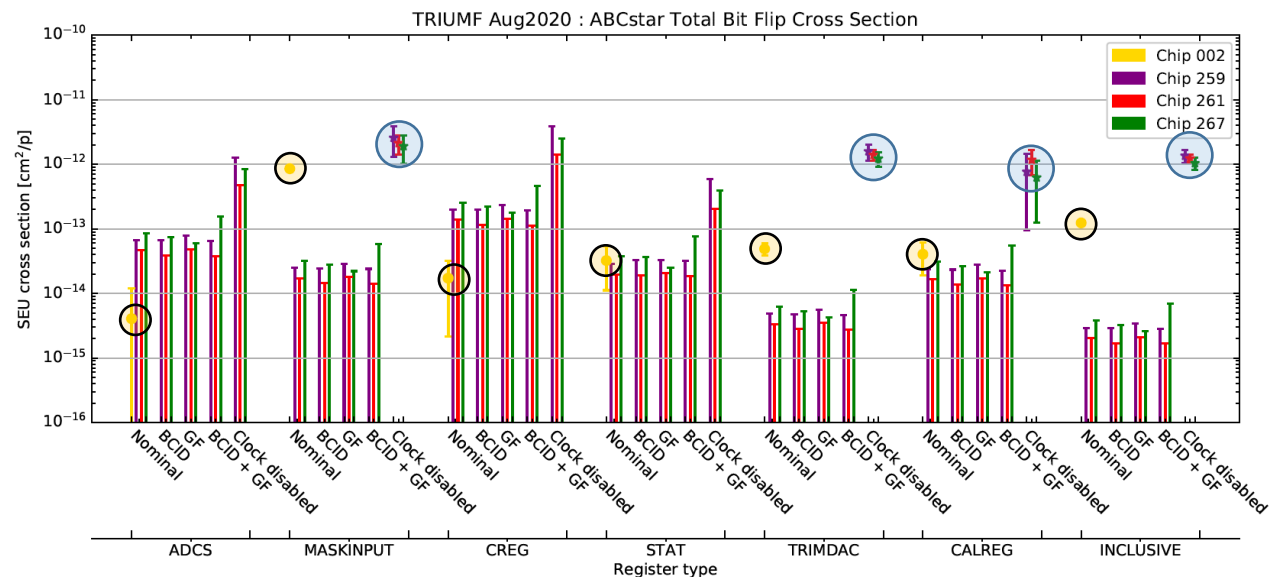


Figure of area where thin sensors were replaced  
And impact on tracking

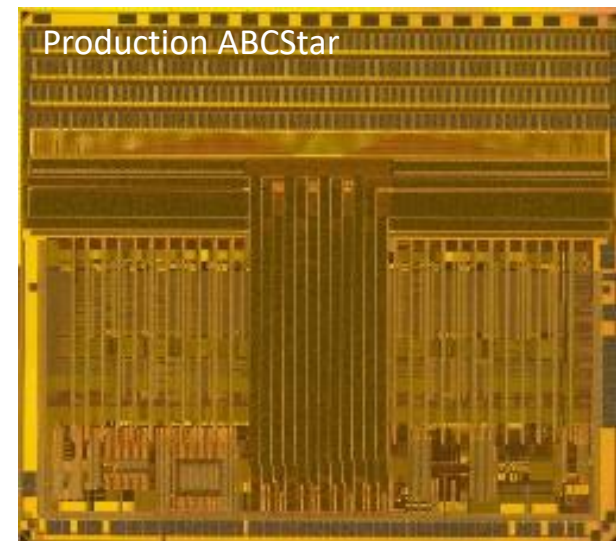


Prototype ABCStar without enhanced triplication

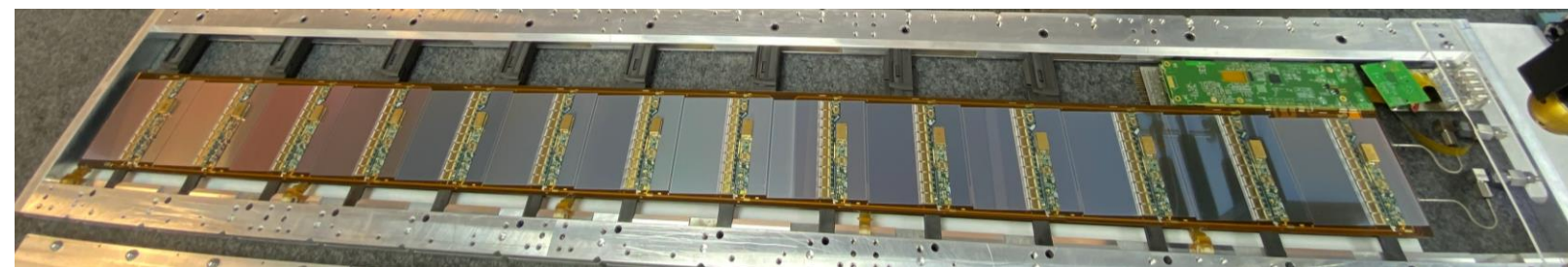
Pre-production ABCStar with triplication disabled

Pre-production ABCStar with triplication enabled had no measured SEUs

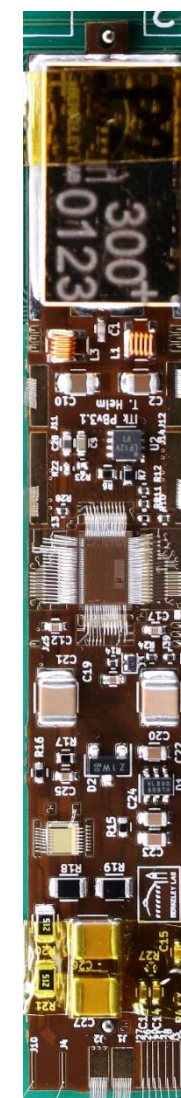
[ITK-2021-002](#)



- The three Strip ASICs went through extensive re-design to significantly increase triplication of logic/controls/clocks:
  - ABCStar (front end), HCCStar (hybrid controller), AMACStar (analog monitor & control)
- ABCStar has been SEE tested in heavy-ions and protons with excellent performance
  - Superb yield in pre-production: 92%
  - Production order placed. First wafers just delivered
- HCCStar/AMACStar pre-production wafers just delivered.



- 14 modules powered on a common bus
- bPOL12V converts from delivered 11 V to 1.5 V for module powering
  - Efficiency of 72% at operating point
- Cable plant heat losses go as  $I^2R$ 
  - Reduction by factor of 28
    - $(\text{Conversion ratio} \times \text{efficiency})^2$
- Complications:
  - DC-DC converters are noisy (high frequency switching)
    - Much development required for light-weight EM shielding and conducted noise reduction.
  - Can not measure V or I per module at power supply
    - Added AMACStar for monitoring
  - As bias on another common bus, developed a custom HV switch to disable individual modules



## bPOL12V

- Rad-hard buck converter
- Custom flat air-core coil
- 0.1 mm Al shield-box to prevent EM noise leakage

## AMACStar

- Control/interlock functionality
- Measurements of temperatures, currents, voltages (LV/HV)

## HV Switch

- Connect/disconnect HV to sensor (in case of faulty sensor)
- GaNFET with 600 V rating

- Powering modules serially with around 1000 chains from 3-14 modules
  - Current flows from one module to next
    - Reduced number of supply lines, less material
    - Chips on a module powered in parallel
  - Power dissipation in services less in services than with parallel powering (30 kW vs 250 kW)
  - Radiation hard on-chip shuntLDO allows regulation of voltage on chip
    - Excess current needs to be supply to accommodate variation due to chip activity (hits)
- Complications
  - Need to add monitoring chip to measure voltage drops and temperature of individual modules

