FPGA and ASIC based algorithms for the present and upgraded LHCb silicon vertex detector

Outline

- LHCb experiment
- VErtex LOcator (VELO)
- Zero suppression procedure for the VELO
- Future vertex detector for upgraded LHCb
- Summary

On behalf of the LHCb VELO project

LHCB Experiment

The LHCb is a forward spectrometer, angular acceptance 15 - 300 (250) mrad or in other 'pseudo-rapidity language' $\eta = 1.9 - 4.9$

A forward spectrometer is sufficient for the physics since produced bb pairs are strongly correlated and forward peaked

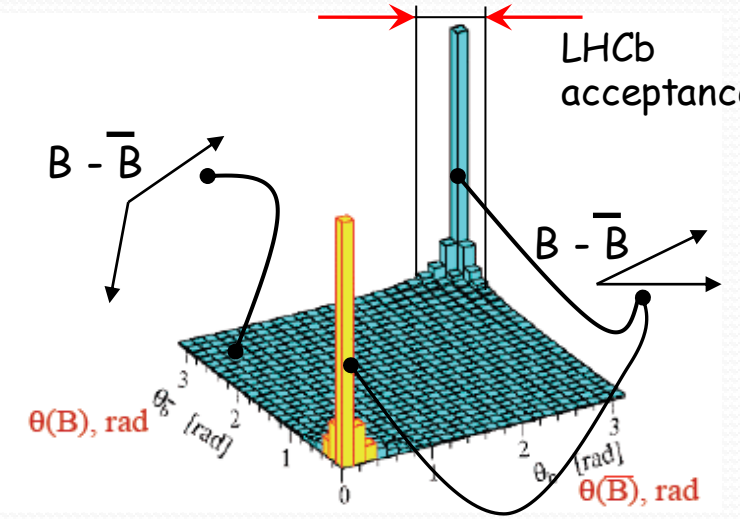
LHC ran at energy of 7 TeV measured cross-section for $b\bar{b}$ is about 290 μb

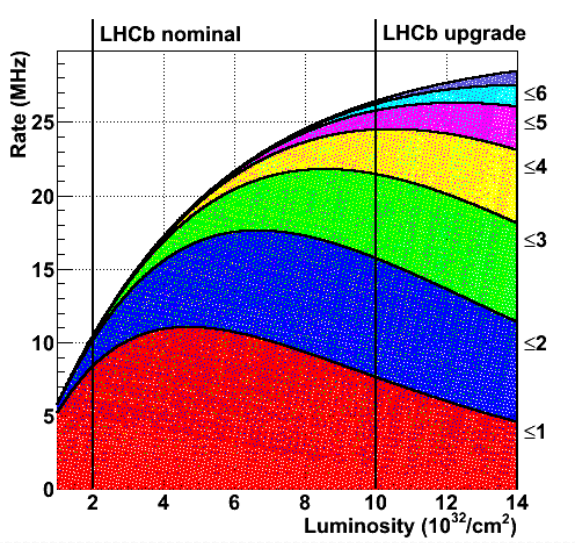
But…, $\sigma_{bb}/\sigma_{Tot} \approx 10^{-2}$, in addition the most interesting events have tiny BR (10^{-6} - 10^{-9})

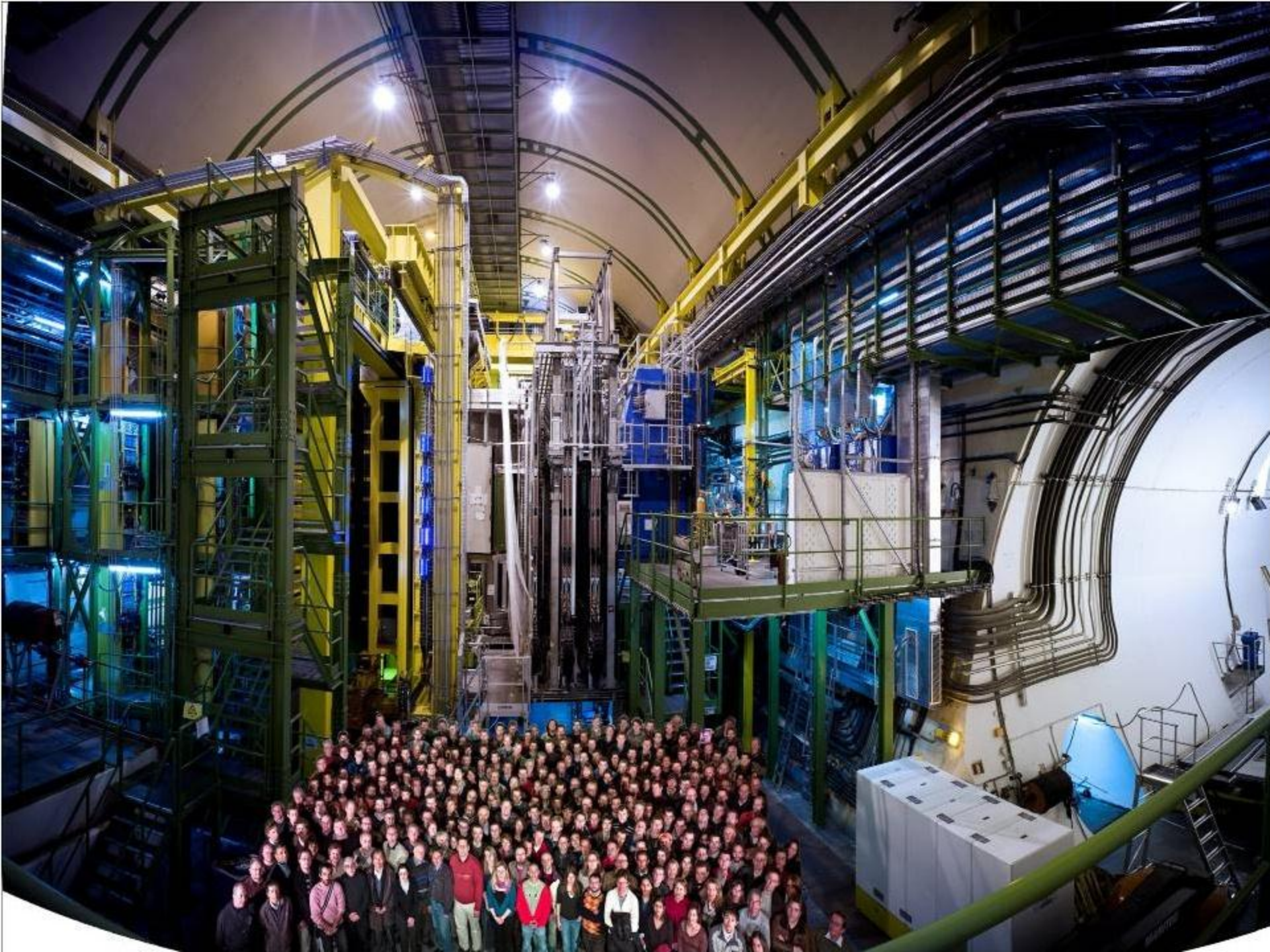
Luminosity ~ $(3 - 4) \times 10^{32}$ cm^{-2} s^{-1} what corresponds to 1.2 fb^{-1} per year

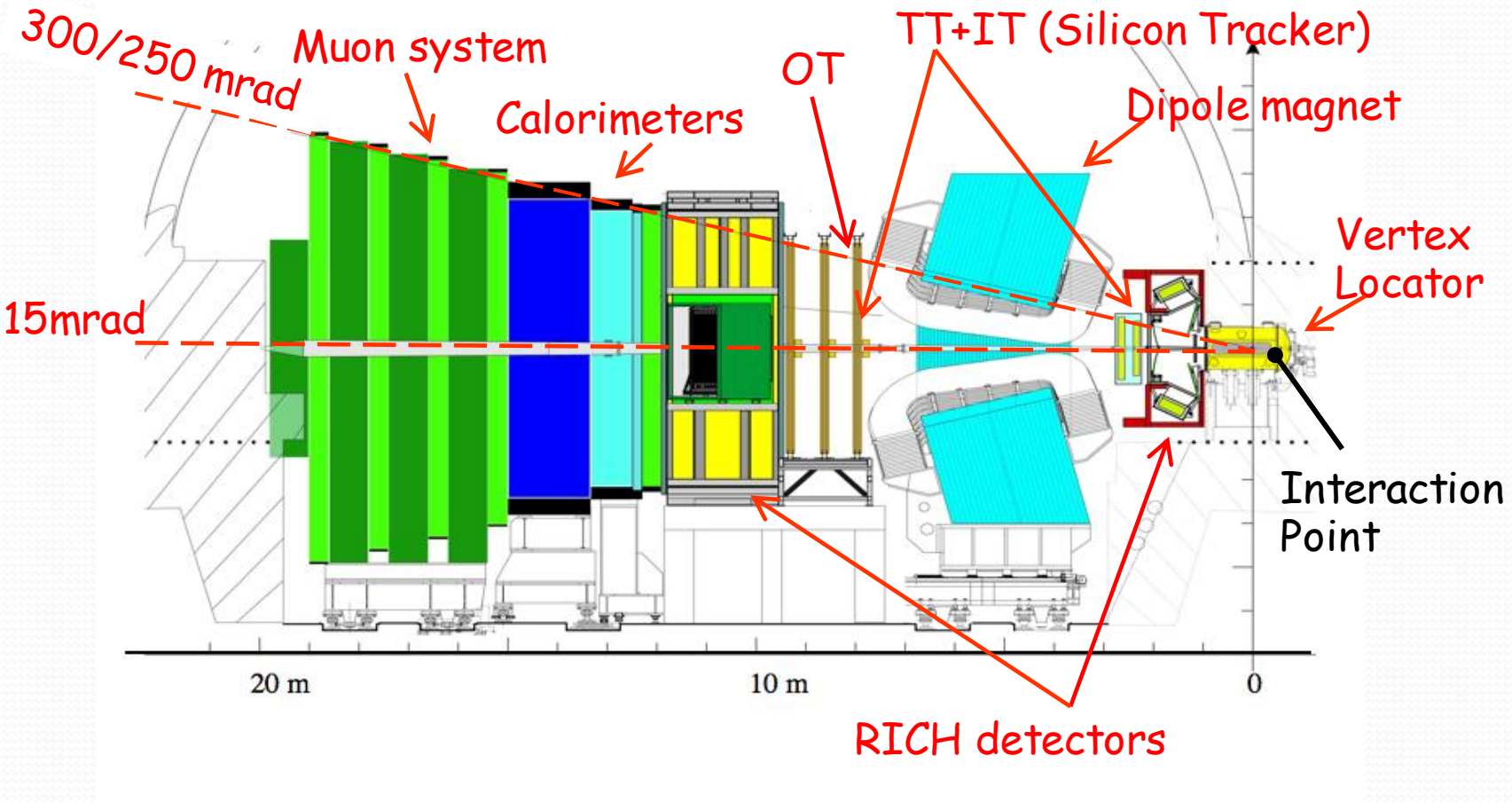
HLT trigger rate ~3 kHz (~ 4 kHz in 2012)

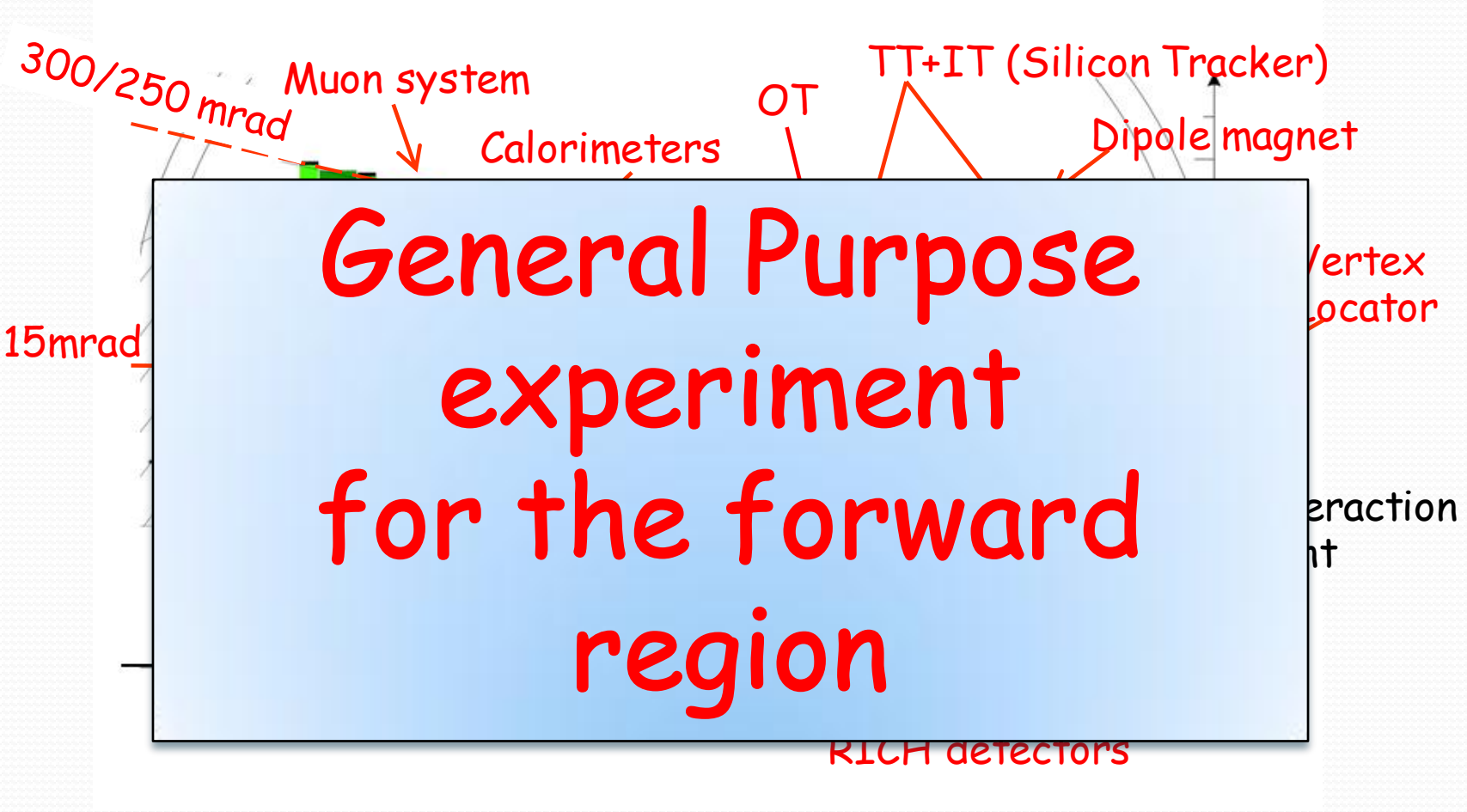
All b-hadron species produced





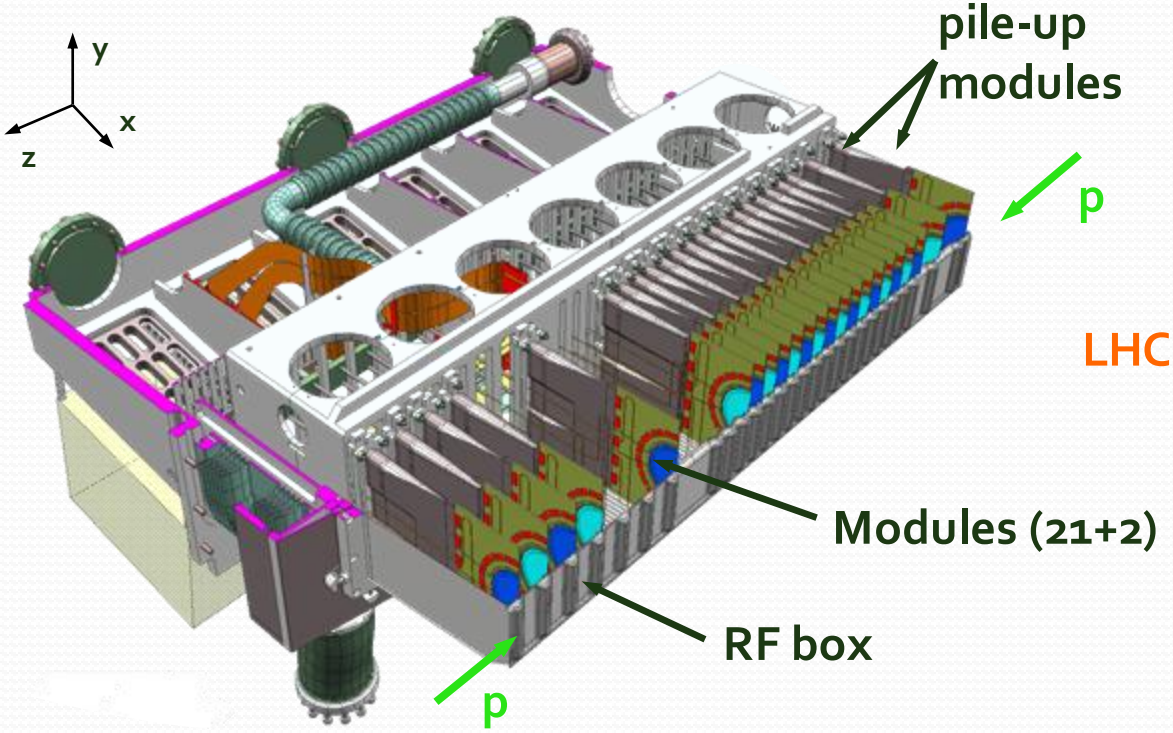


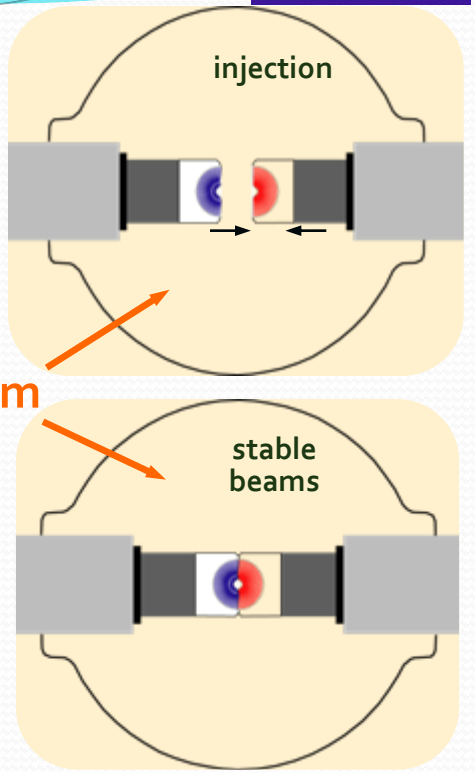

300/250 mrad
Muon system
Calorimeters
OT
TT+IT (Silicon Tracker)
Dipole magnet
Vertex Locator
15mrad
Interaction Point
20 m
10 m
0
RICH detectors



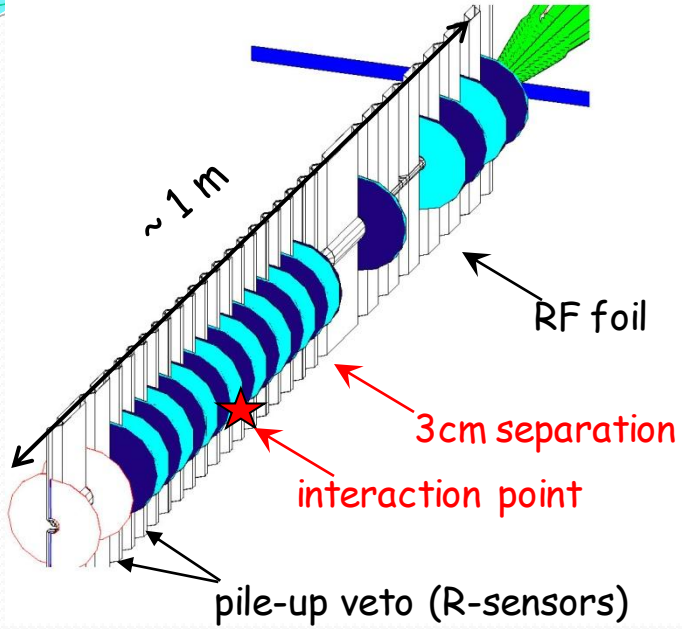
General Purpose experiment for the forward region

Vertex Locator (VELO)

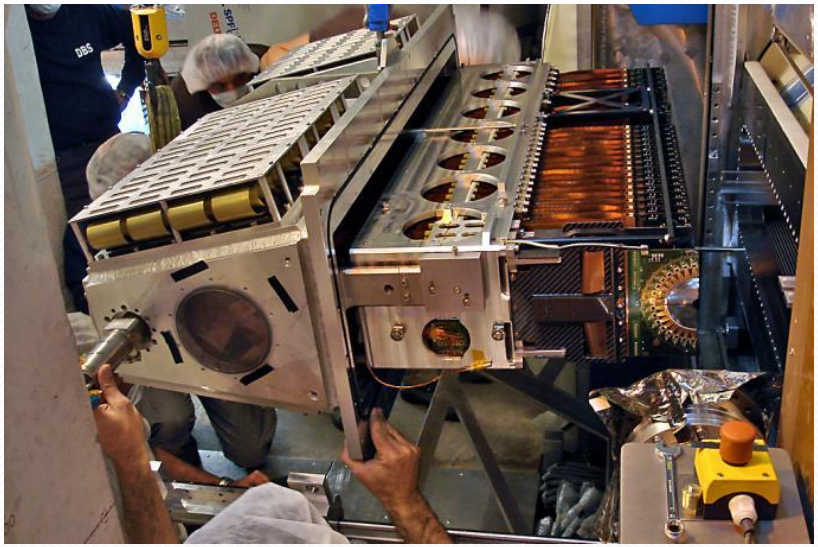


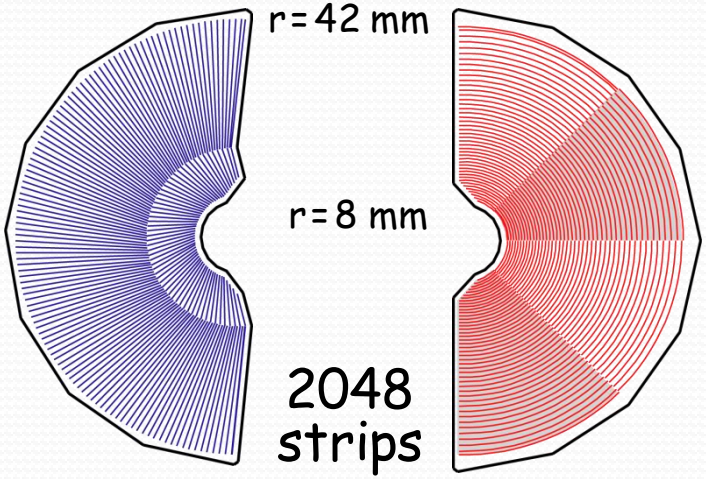


- **2 retractable detector halves:**
  ~8 mm from beam when closed, retracted by 30mm during injection
- **21 stations per half with an R and a ϕ sensor**
- **Secondary vacuum tank**
- **300μm foil separates detector from beam vacuum**



- Detector halves retractable (by 30mm) from interaction region before LHC is filled (to allow for beam excursions before stable beam)
- 21 tracking stations
- Unique R-Φ geometry, 40–100μm pitch, 300μm thick
- Optimized for
  - tracking of particles originating from beam-beam interactions
  - fast 3D tracking in two steps (R-z then Φ)





The LHCb VELO detector is an essential part of the whole spectrometer

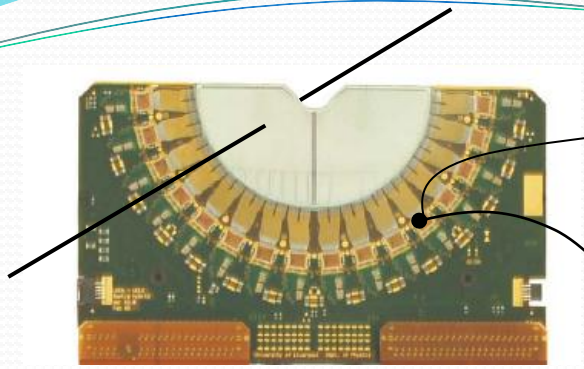
- stand alone tracking
- reconstruct primary and secondary vertices
- precise position measurement around the interaction point

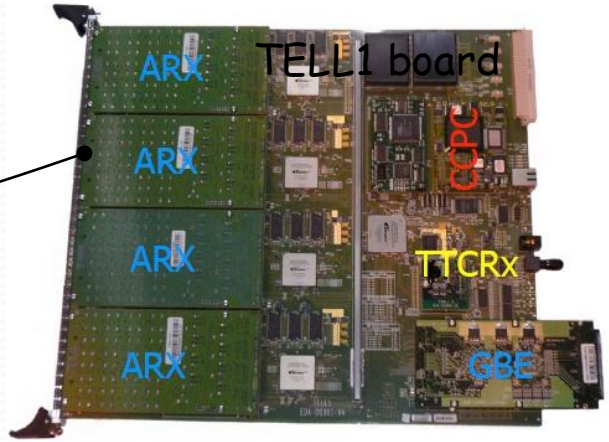
All these critical for the physics performance of the experiment

- Impact parameter
- vertices resolutions
- life time
- …

Thus quality of the data produced by the VELO is critical for the physics

Zero suppression procedure for the VELO





Common electronic acquisition read-out board – **TELL1**

Digital/analogue input (interfaced to gigabit Ethernet)

FPGA based – Altera Stratix

Main goal – synchronisation, buffering and the data zero suppression (factor ~ 200)

From non-zero suppressed (2048 /sensor)

To zero suppressed (clusters only)

Technically it is a farm of parallel stream processors

Processing 36 threads at the same time

Raw cluster buffer

↓

Reconstruction

How to control the hardware based zero suppression?

- not a trivial task
- processing runs in real time using hundred of threads
- huge amount of data
  88 sensors x 2048 channels x 10 bits x 1 MHz

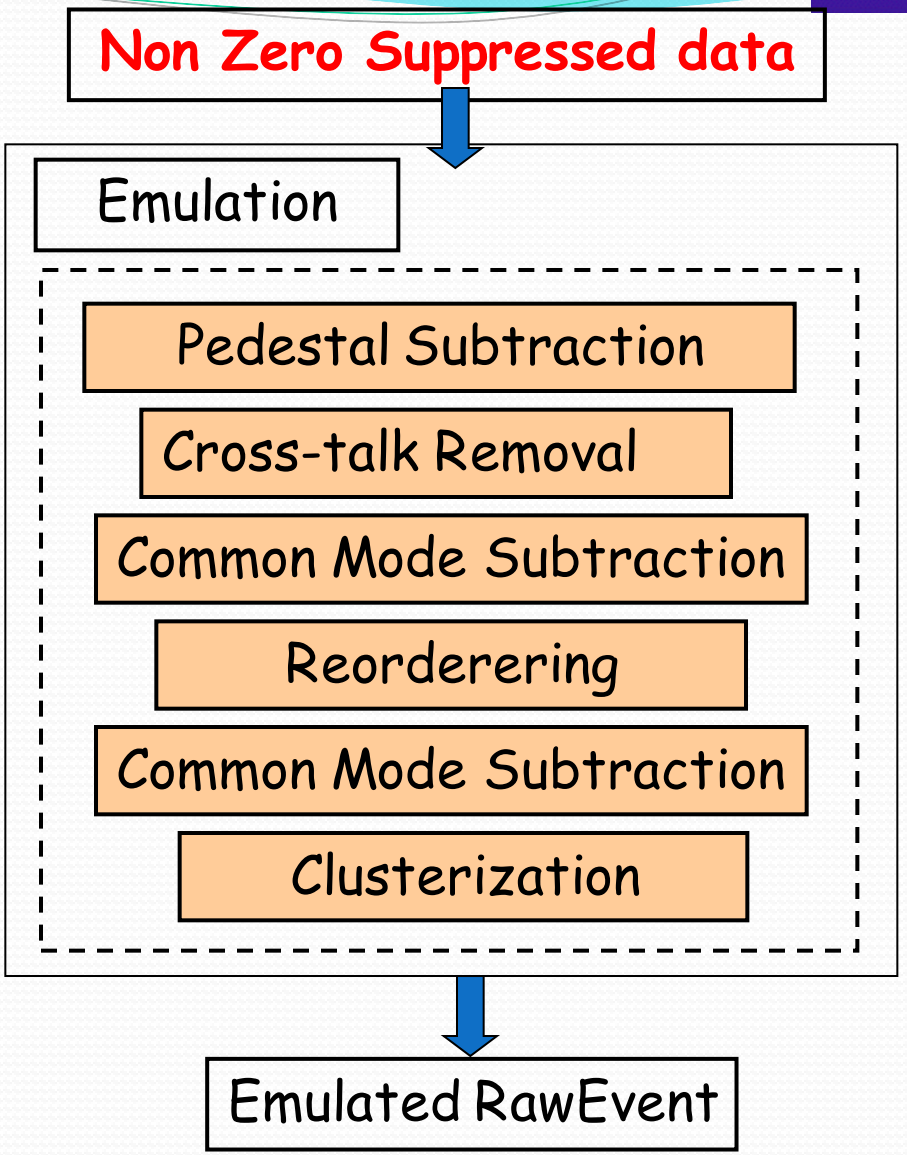
Solution - high level, bit-perfect emulation

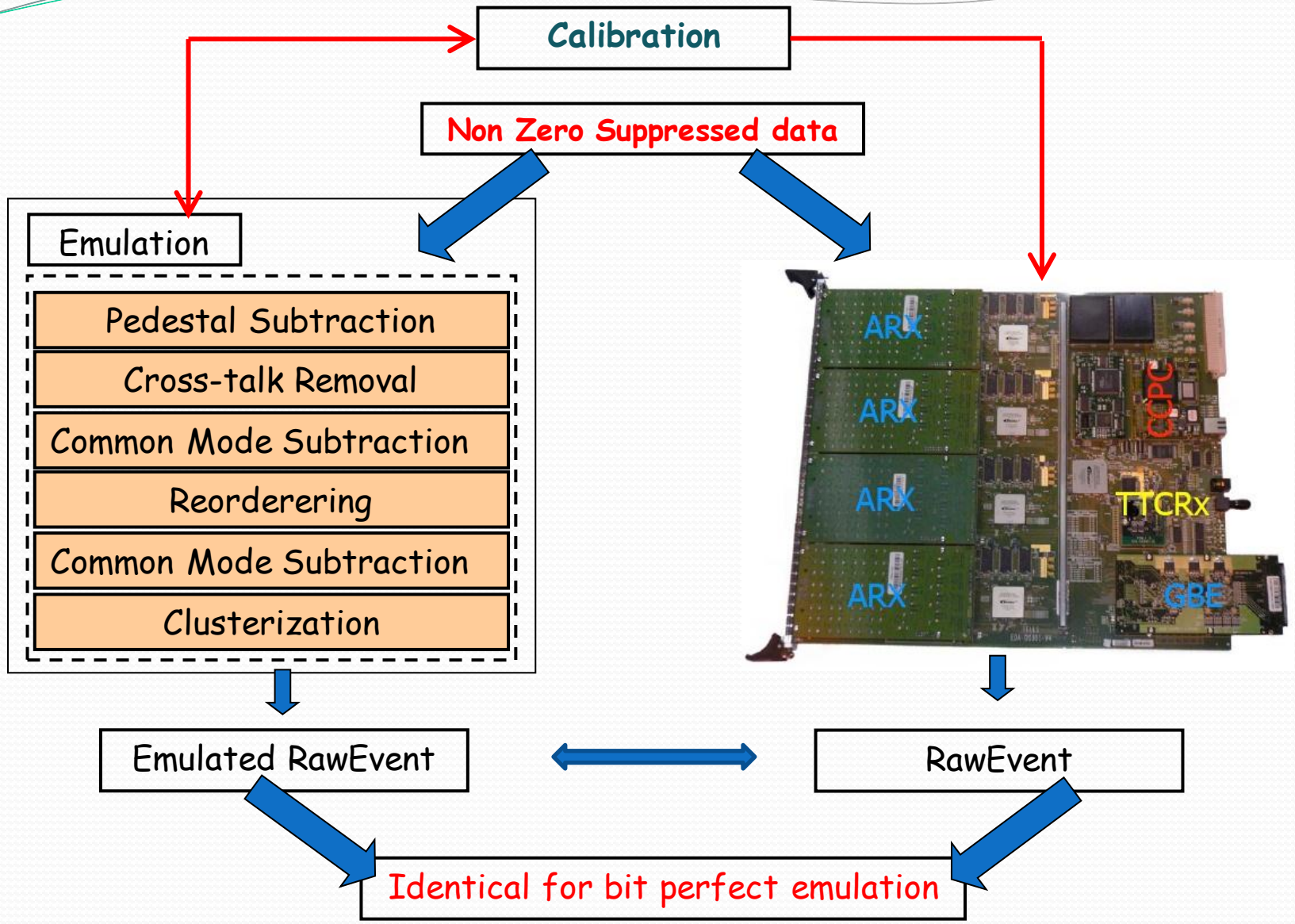
- runs off-line on single CPU
- uses real non-zero suppressed data
- high level model of the VHDL machine code from FPGAs
- calibration and monitoring

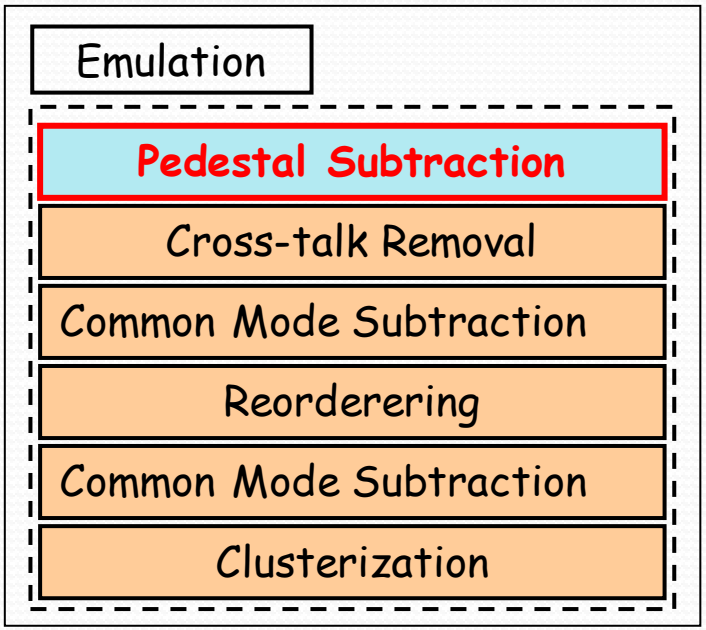
Emulation has the same structure and operates on the same data as the real processing done in FPGAs

Parameters used for readout board fixed in emulation

The full set of parameters that are required for the proper operation of the TELL1 boards amounts to ~ 10^6




Calibration
Non Zero Suppressed data
Emulation
Pedestal Subtraction
Cross-talk Removal
Common Mode Subtraction
Reorderering
Common Mode Subtraction
Clusterization
ARX
ARX
ARX
ARX
CCPC
TTCRx
GBE
Emulated RawEvent
RawEvent
Identical for bit perfect emulation



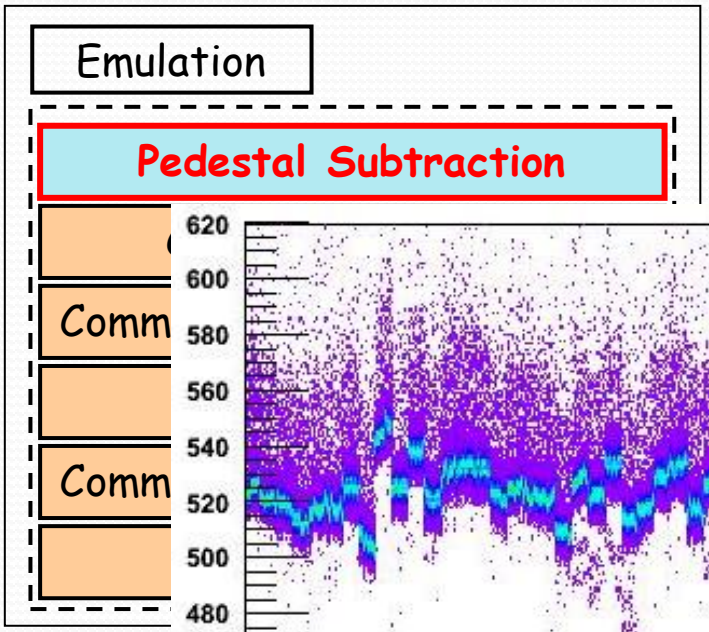
Pedestal following & subtraction

- first algorithm in the sequence
- running average algorithm
- following (training done off-line only)
- pedestals are calculated for each channel
- values are stored in the TELL1 memory

Critical for the quality of the zero-suppressed data

Any problem with pedestals will manifest itself as a change in occupancy

- careful monitoring required



Pedestal following & subtraction

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ıch channel
memory

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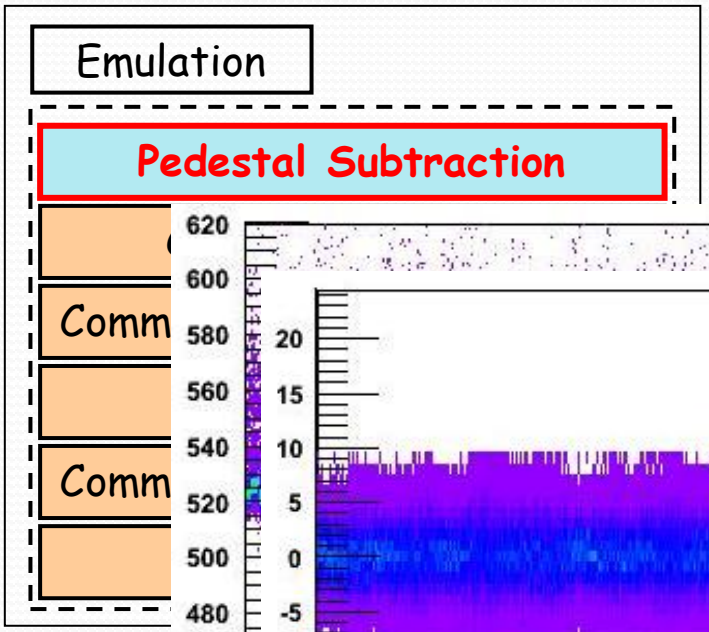

Pedestal following & subtraction

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pressed data

Emulation

Pedestal Subtraction

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Comm

Pedestal following & subtraction

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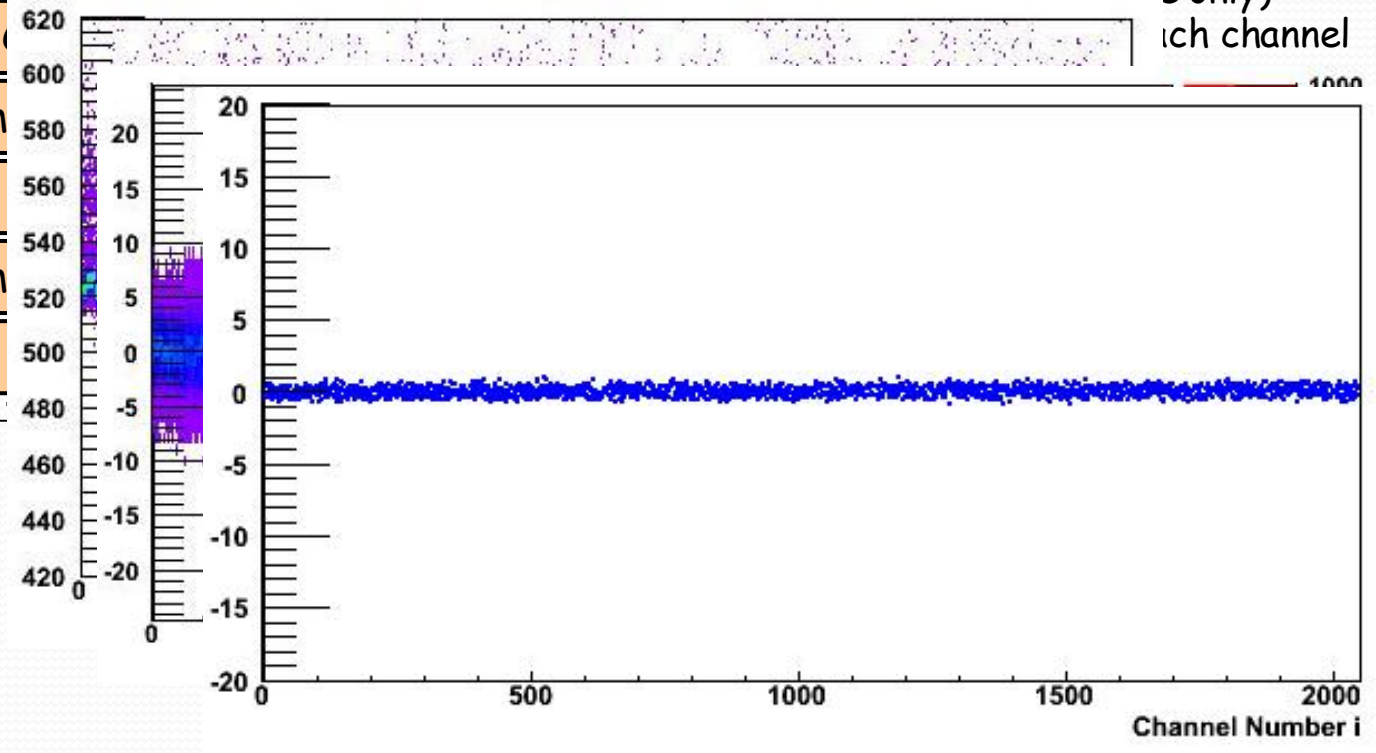
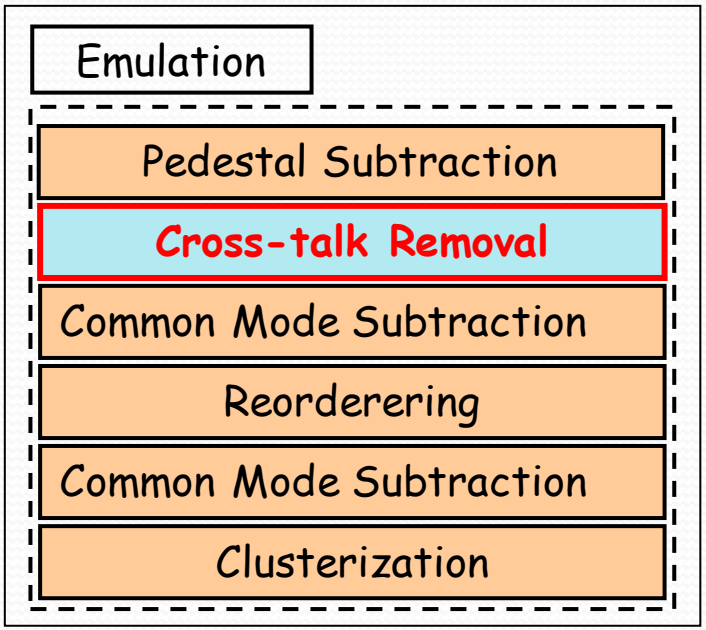




Cross-talk removal

- with such complicated system hard to take into all possible sources

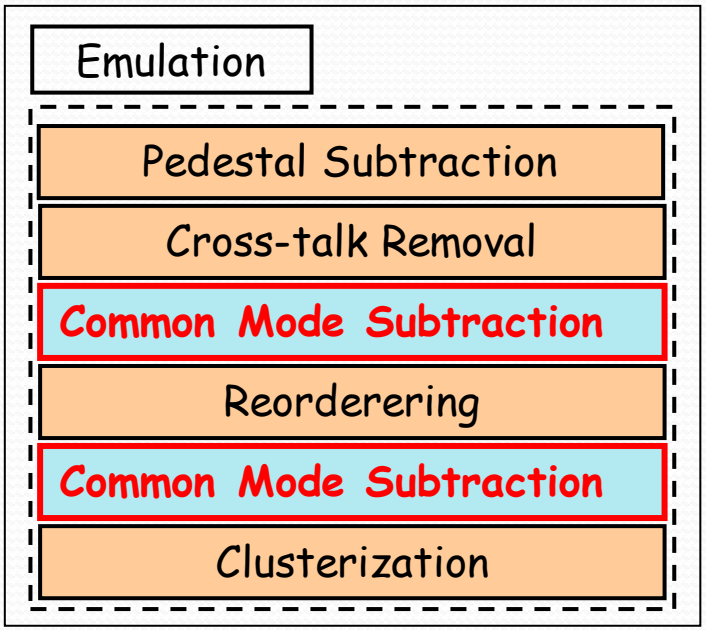
Two kinds are regarded to be dominant

- Beetle Header Cross Talk (front-end chip related)
- cross-talk related to data transfer over the copper cables (~60 meters)

Test beam campaign hinted a possible issues
However the time aligned and properly calibrated system shows minute effect

No correction applied for the 2011 data taking
Monitoring algorithms in place, though!

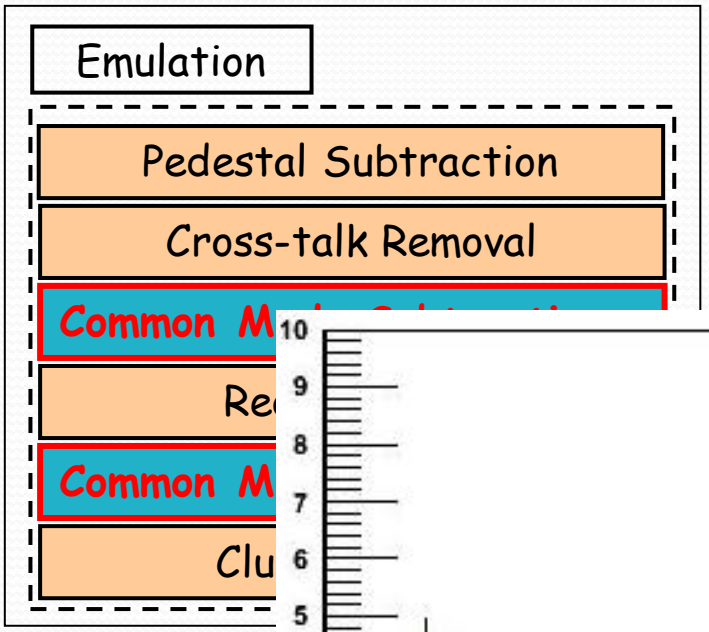
- We surely keep tabs on it!



Common Mode Subtraction

- two stage correction (performed on chip channels /strips)
- uses blocks of 32 chip channels/strips
- first algorithm is Mean Common Mode subtractor
- second Linear Common Mode subtractor
- performance depends strongly on the occupancy
- hit exclusion is of the greatest importance for both algorithms
- tuneable exclusion parameters for both of them are determined during the calibration (per chip)
- wrong tuning can give visible distortion for the signal

Fortunately the common mode is not a major problem for the VELO
Again - detailed monitoring keeps watching the CM



Common Mode Subtraction

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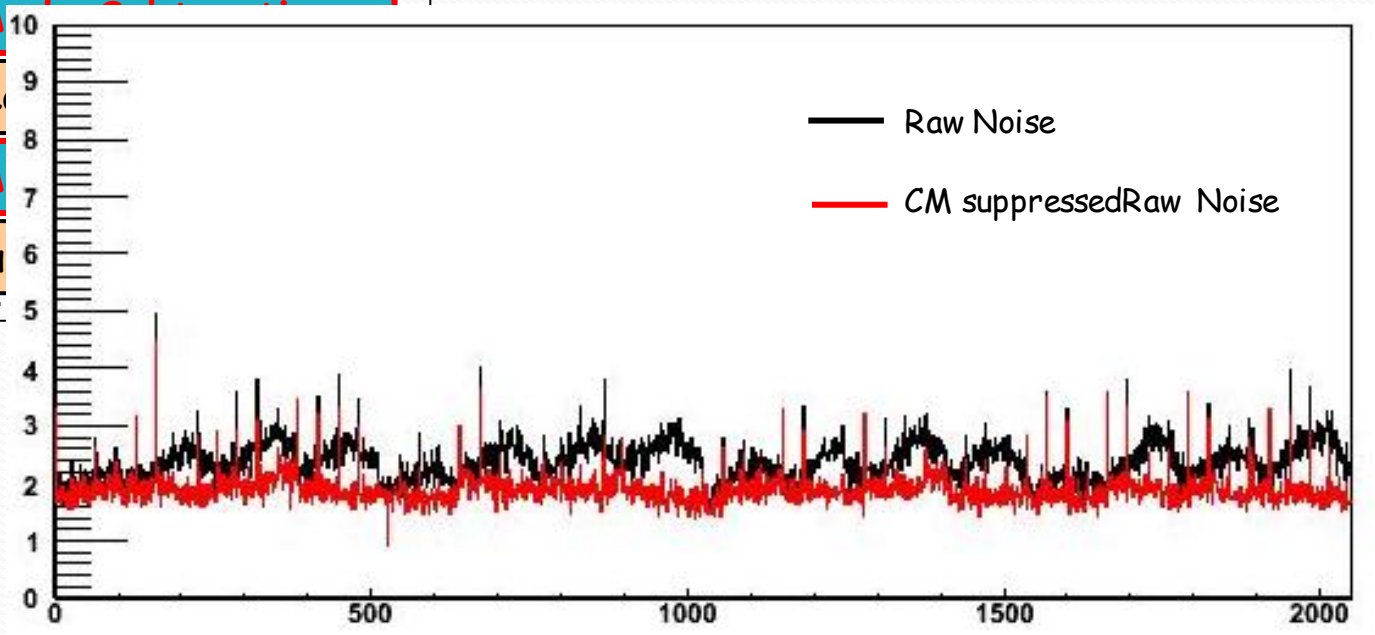

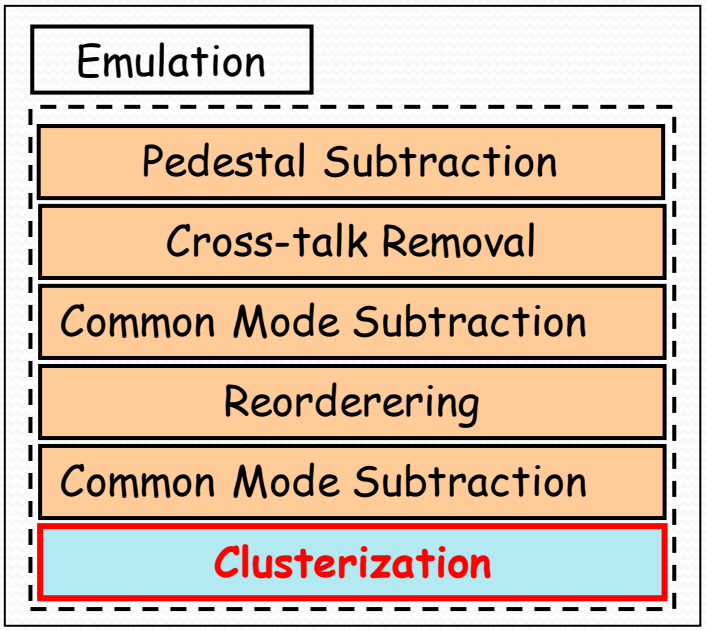

Clusterization

- last in the zero-suppression sequence
- multi stage algorithm (seeding & inclusion) – again uses 32 channel blocks of data
- seeding and inclusion thresholds tuned individually for each channel
- sensitive to the cluster shape
- produces the raw bank of clusters

Each VELO cluster consists of

- main channel (closest to the cluster centre)
- fractional position
- ADC values from channels that contribute to a given cluster

The raw bank constitutes the input for the track reconstruction procedure

Emulation

Pedestal Subtraction

Cross-talk Removal

Common Mod

Reor

Common Mod

Cluste

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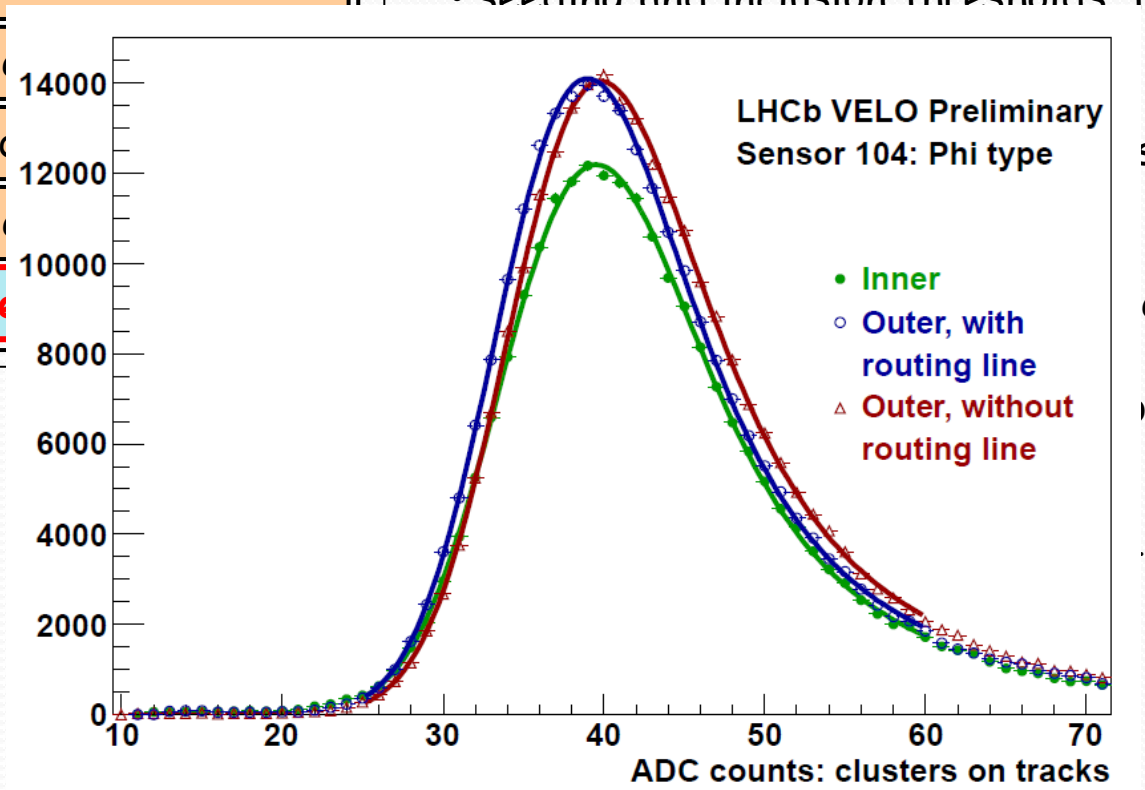

Emulation

Pedestal Subtraction

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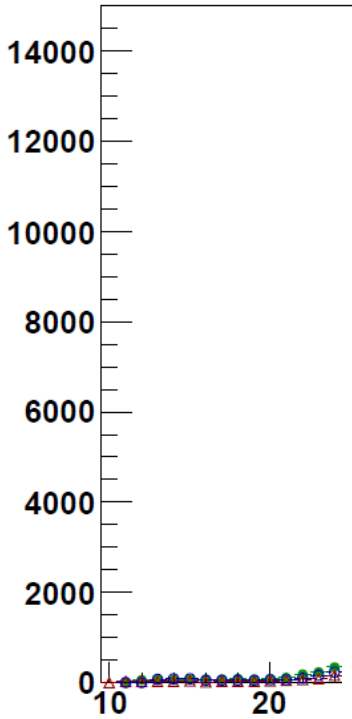

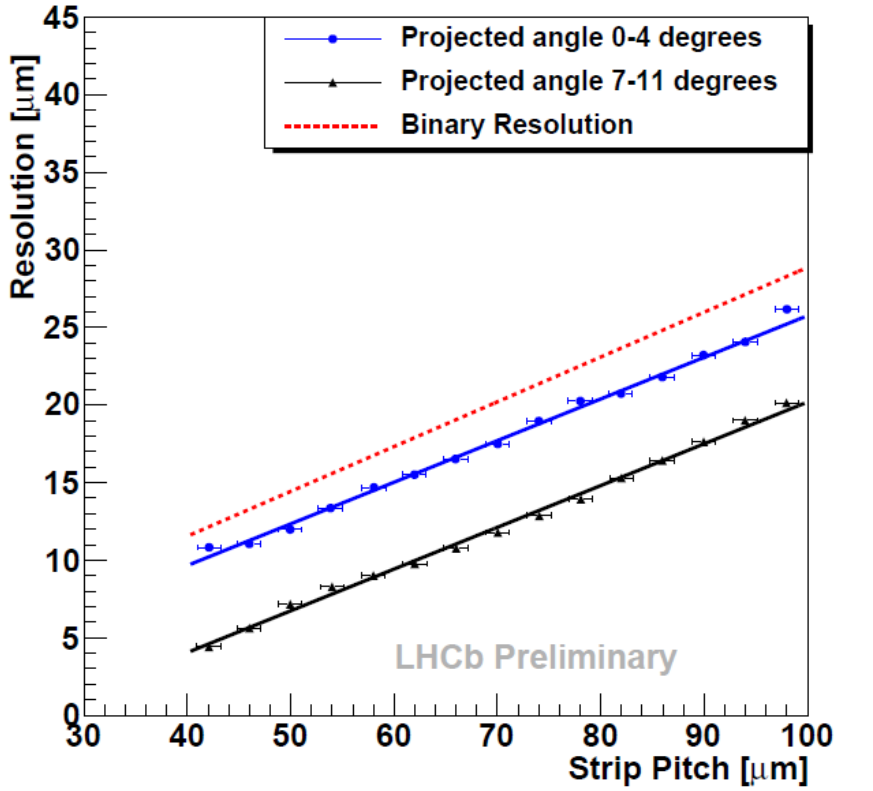

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For the present VELO we have a very strong synergy between the on-line processing (TELL1 based) and off-line processing/monitoring

- we cannot run high-level emulation in real time
- we cannot run TELL1 zero suppression without calibration

Solution

- first we need to perform the calibration run with non-suppressed data
- determine a set of processing parameters
- upload them to the TELL1 memory banks (on-line processing)
- create a SQLite data base (off-line processing)
- run the emulation regularly to monitor the processing algorithms
- monitor the output of the TELL1 boards to check the quality of the calibration (cluster rates, occupancies, landaus, …)

The bit-perfect emulation is essential!

Future vertex locator for upgraded LHCb

Why upgrade (is there something wrong with the current design…?)

Superb performance – but 1 MHz readout is a sever limit

- can collect ~ 1.2 fb^{-1} per year, ~ 5 fb^{-1} for the „phase 1" of the experiment
- this is not enough if we want to move from precision exp to discovery exp
- cannot gain with increased luminosity – trigger yield for hadronic events saturates

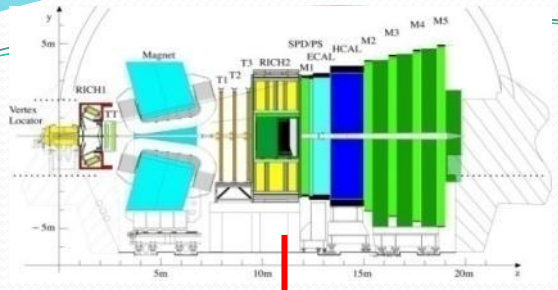
Upgrade plans for LHCb do not depend on the LHC machine

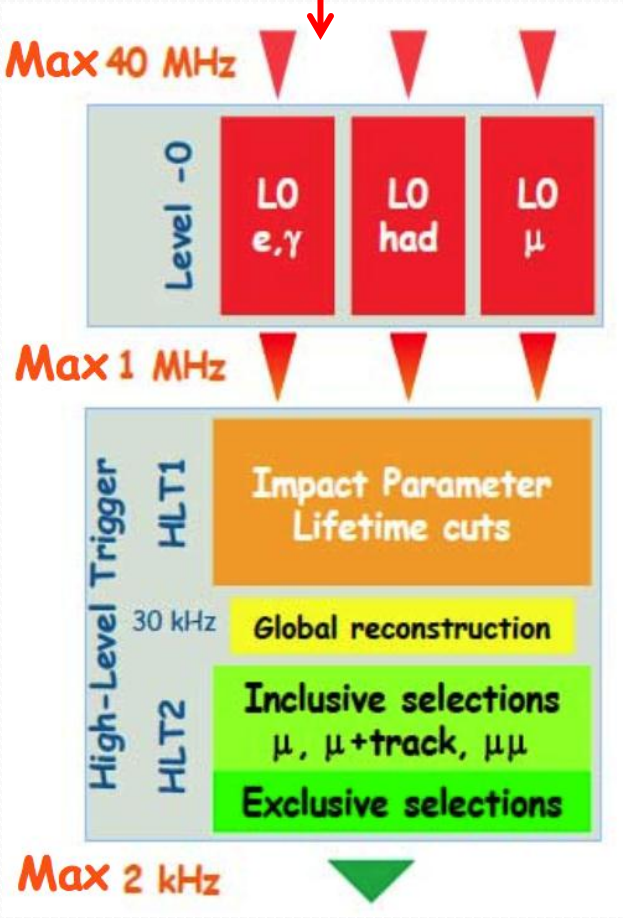
- we use fraction of the luminosity at the moment

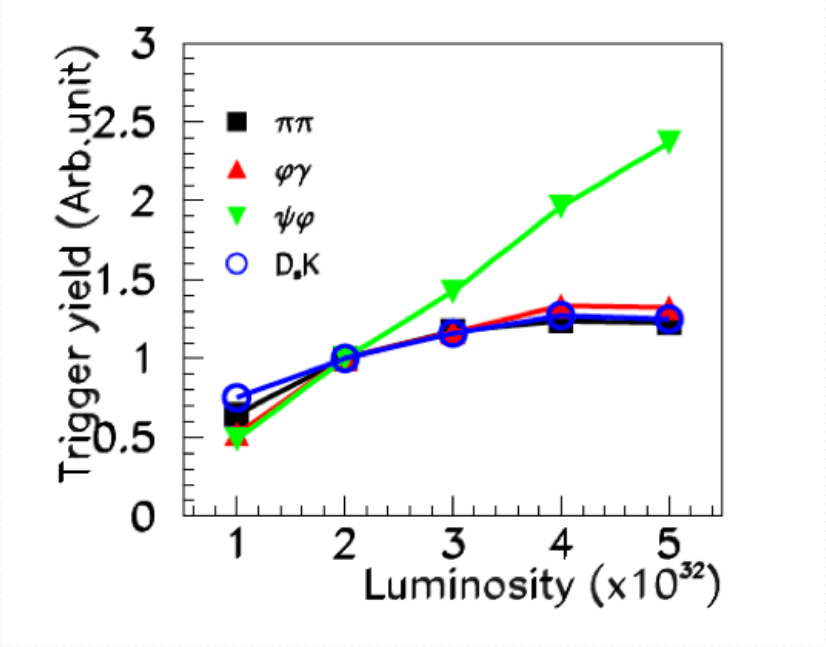
Move to full software trigger

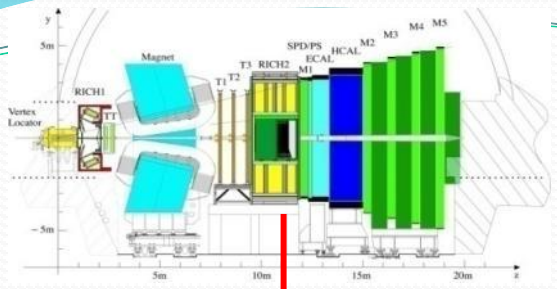
- full event read-out @ 40 MHz
- completely new front-end electronics needed (on-chip zero-suppression)
- redesign DAQ system
- HLT output @ 20 kHz, more than 50 fb^{-1} of data for the „phase 2"
- can gain factor 2 in signal rate for hadronic events
- Expand physics scope to: lepton flavor sector, electroweak physics, exotic searches

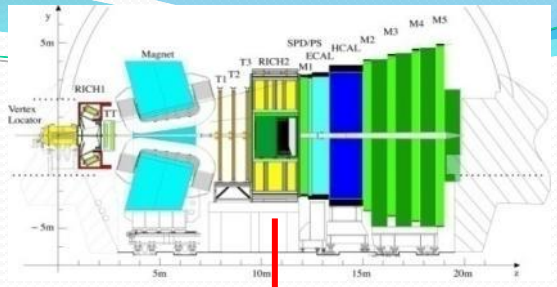
Installation ~ 2017 - 2018

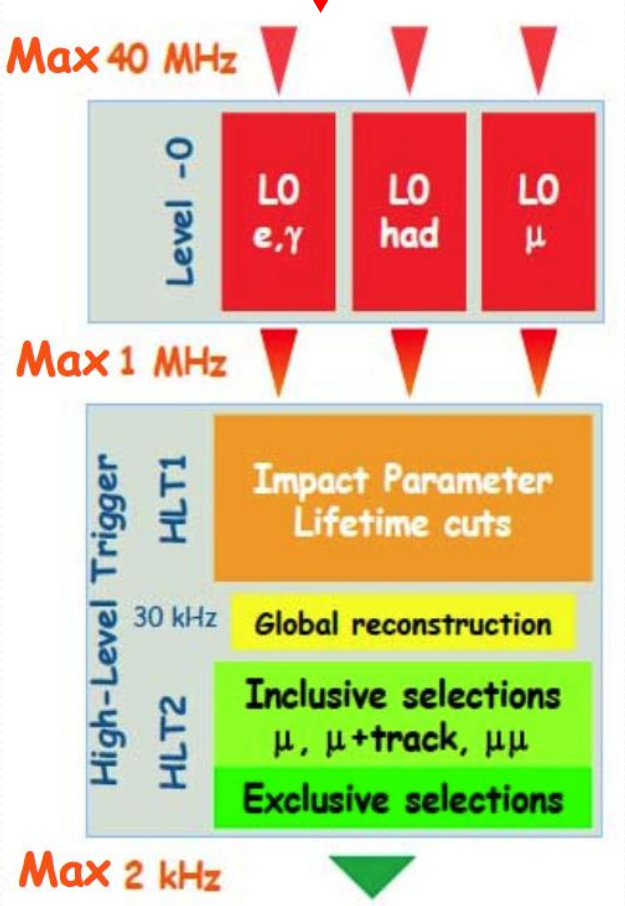

Magnet
RICH1
RICH2
SPD/PS
ECAL
HCAL
M1
M2
M3
M4
M5
T1
T2
T3
TT
Vertex Locator
5m
10m
15m
20m


Max 40 MHz
Level -0
L0 e,γ
L0 had
L0 μ
Max 1 MHz
High-Level Trigger
HLT1
Impact Parameter Lifetime cuts
30 kHz
Global reconstruction
HLT2
Inclusive selections μ, μ+track, μμ
Exclusive selections
Max 2 kHz


Trigger yield (Arb.unit)
Luminosity (x10^32)
ππ
φγ
ψφ
D_sK
0
0.5
1
1.5
2
2.5
3
1
2
3
4
5






Max 40 MHz
Level -0
L0 e,γ
L0 had
L0 μ
Max 1 MHz
High-Level Trigger
HLT1
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30 kHz
Global reconstruction
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Inclusive selections μ, μ+track, μμ
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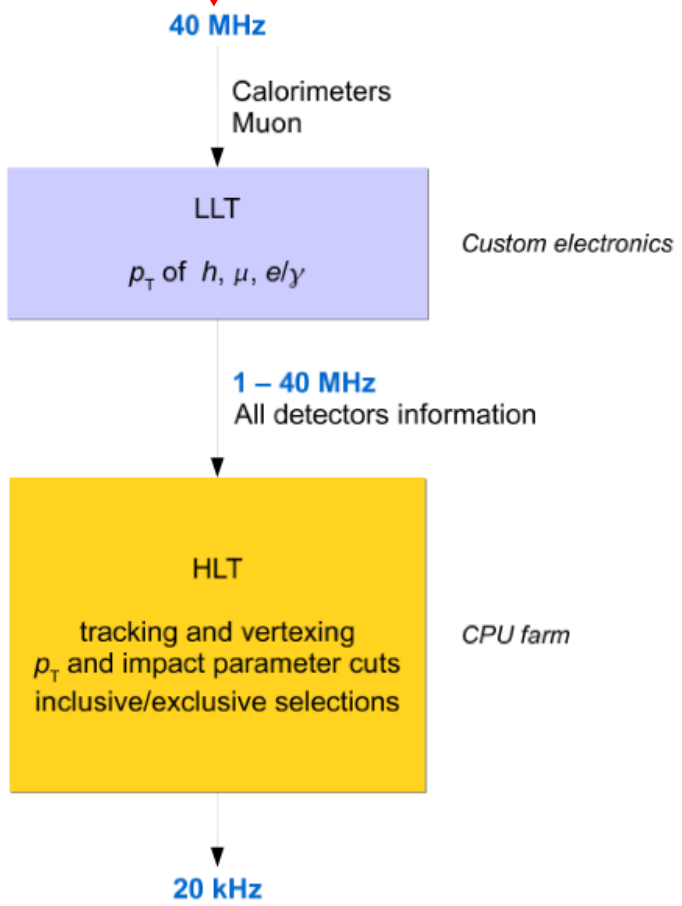
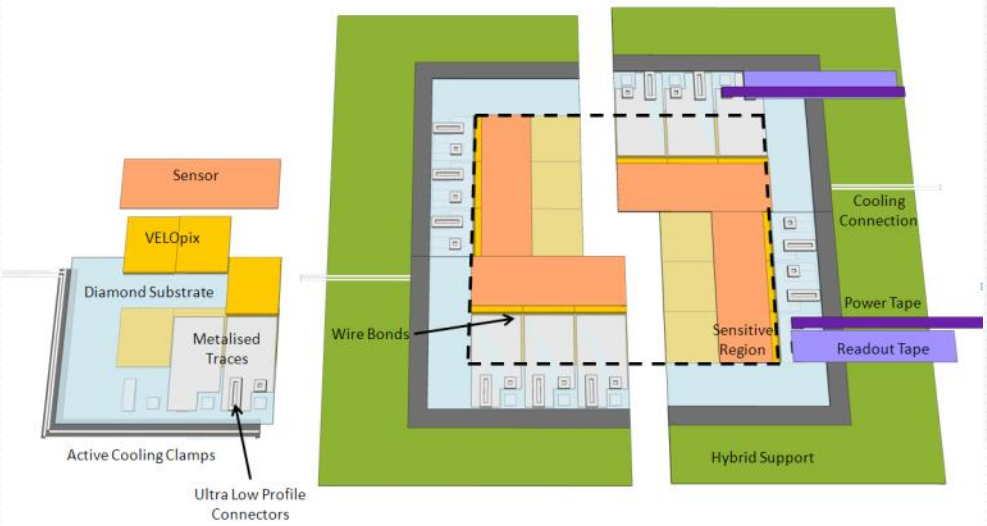
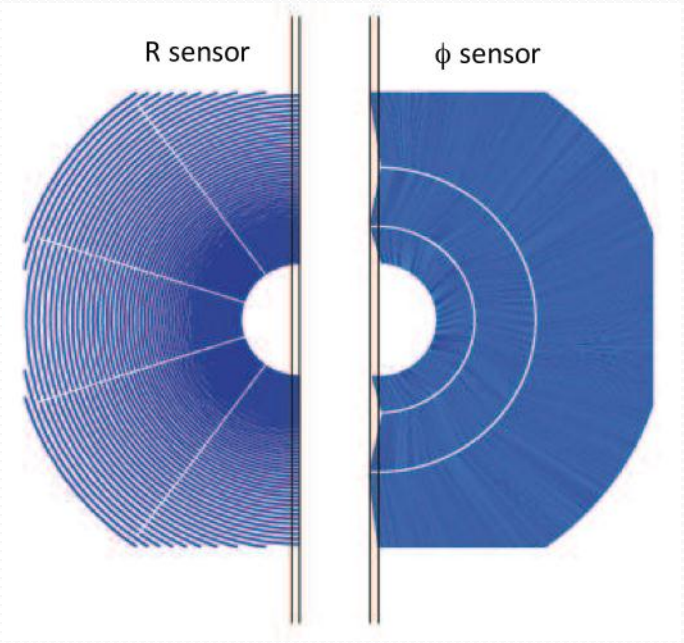
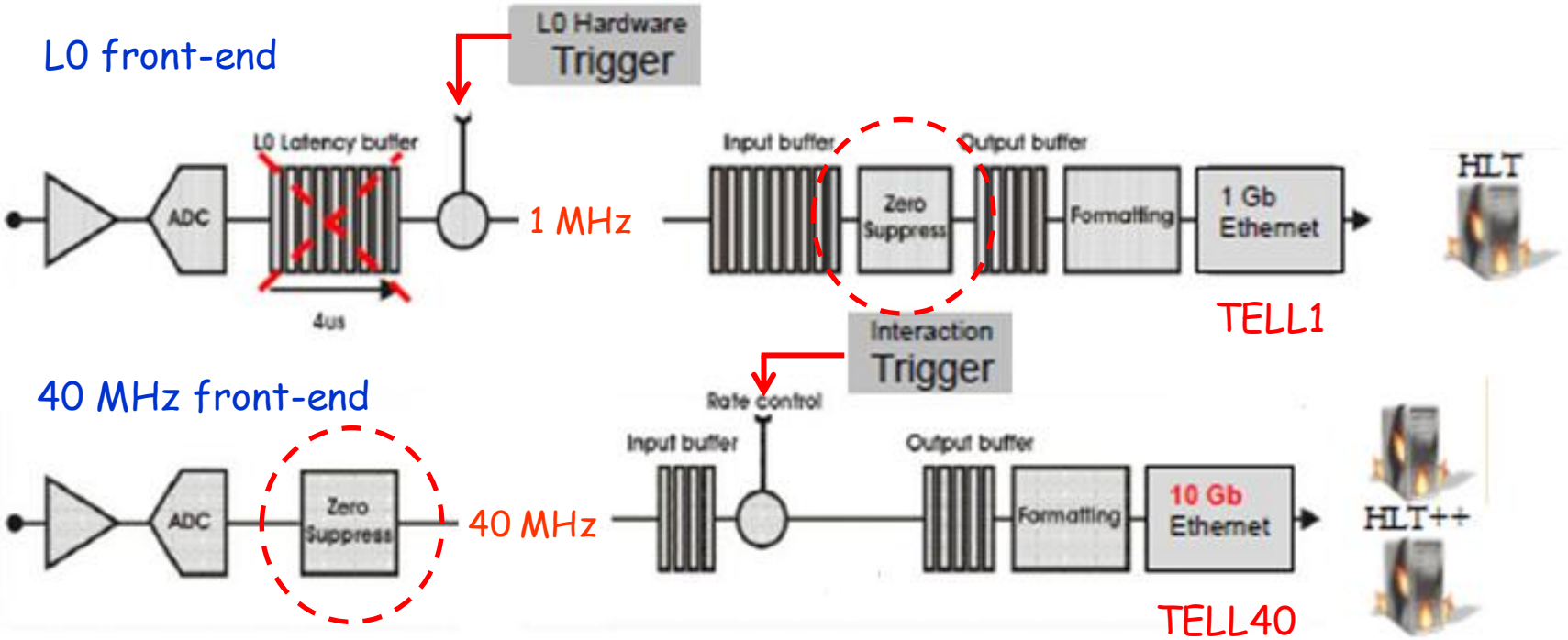

40 MHz
Calorimeters
Muon
LLT
p_T of h, μ, e/γ
Custom electronics
1 – 40 MHz
All detectors information
HLT
tracking and vertexing
p_T and impact parameter cuts
inclusive/exclusive selections
CPU farm
20 kHz



- New Velo @40 MHz readout
  - Pixel detector: VELOPIX based on Timepix3 chip
    - 55 μm x 55 μm pixel size
  - Strip detector
    - New chip

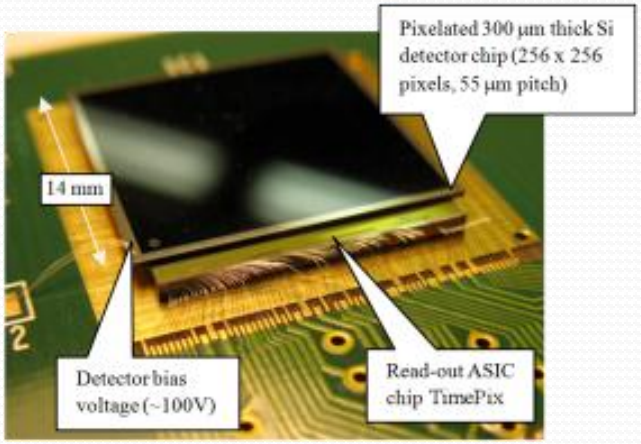
- R&D programme
  - Module structure (X_0)
  - Sensor options
    - Planar Si, Diamond, 3D
  - CO_2 cooling
  - Electronics
  - RF-foil of vacuum box





New front-end chip for the pixel/strip option
New electronic acquisition board – TELL40

Pixel option – VeloPix (based on Timepix3 chip)



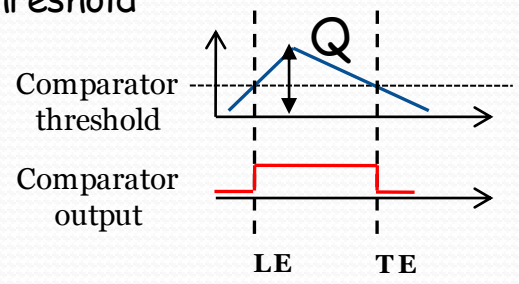
Timepix3 - square 55x55 μm pixels

- 256x256 pixel matrix
- approved project – final submission this summer
- equal spatial resolution in both directions
- IBM 130 nm CMOS process
- great radiation hardness potential ~ 500 Mrad

Velo specific requirements

- large number of channels makes the occupancy tiny but the data rate is huge ~10 Gb/s
- on-chip compression
- continuous dead-timeless operation
- power consumption below 2 W/chip
- 6 bit Time over Threshold (ToT) resolution
- quicker time rise to reduce the timewalk < 25 ns
- bunch identification for each hit

Conversion by time-over-threshold



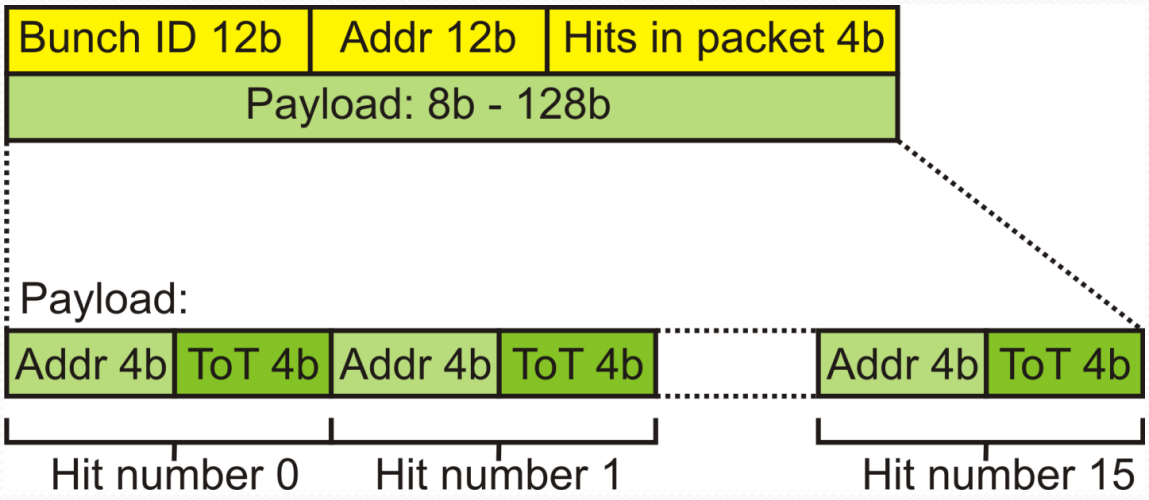
ToT = f(Q)

VeloPix – read-out architecture

- hit detection within super pixel (4x4 pixels) structure
- optimal wrt data compression and sharing the hardware resources
- large data rate reduction (25 %, sharing bunch ID and address)
- all hits detected within 25 ns are sent out in the same packet
- column read-out logic shared between 4 super pixels

VeloPix – output data format

- optimised to reduce the on-chip data rate
- Minimize the TELL40 acquisition board's firmware complexity



Read-out chip for strip option

- completely new design - to keep balanced R&D process for upgraded VELO
- work started last year
- can be shared between other sub detectors

Basic requirements

- IBM 130 nm CMOS technology
- fast shaping time, signal reminder after 1 BX ~ 30%, 2 BX ~ 0% (spill over)
- 6 bit ADC
- on-chip digital processing (zero-suppression)
  - pedestal subtraction
  - CM suppression
  - Clusterization
- integrate 128 or 256 channels, power consumption below 2 W

Time line for the development

- ADC block has been finished and is being submitted now
- analogue part is being simulated, the implementation will commence in summer
- zero-suppression will be first implement (emulated) using FPGAs

New electronic acquisition board TELL40

- 24 GBT serial input streams
- FPGA based (Altera Stratix V/VI)
- Input data
  - Data packets identification (output data format optimisation helps!)
  - Time ordering for VeloPix (packets come in random order)
  - Decoding super pixels to individual pixels (ToT and address)
- Processing
  - Zero-suppression moved to front-end
  - Any complex algorithm will be resource intensive (40 MHz)
  - Clusterization for pixels
  - Interpolated centre position for strips
  - Hits spatial ordering (for patter recognition)
- Output (not VELO specific)
  - Event building and formatting
  - Storage and filtering
  - Ethernet frames building

Considerable work has been done for the pixels – 90% of the firmware is ready
Some of the code should be reusable for strips

Conclusions

- Superb performance of the LHCb experiment in 2010 and 2011
- Large number of new physics results
- Silicon Vertex Locator is a key to this success with best spatial and impact parameter resolution in LHC
- Zero-suppression procedure critical for the high data quality

- Upgrade of the present detector essential for discovery potential of the LHCb
- Two options are being considered – pixels and strips
- New read-out electronics is needed
- VeloPix chip for pixel option based on existing Timepix3 design
- New design for the strip option
- On chip processing necessary to cope with the enormous data rates

Spares

The actual performance of the LHCb detector significantly surpassed the design parameters during 2011 data taking

- typical luminosity during the data taking $3x10^{32}$ (nominal $2x10^{32}$)
- number of reconstructed PV up to 6 per event
- mean number of visible interaction per crossing 1.8 (nominal 0.7)
- average HLT trigger rate 3 kHZ (nominal 2 kHz)

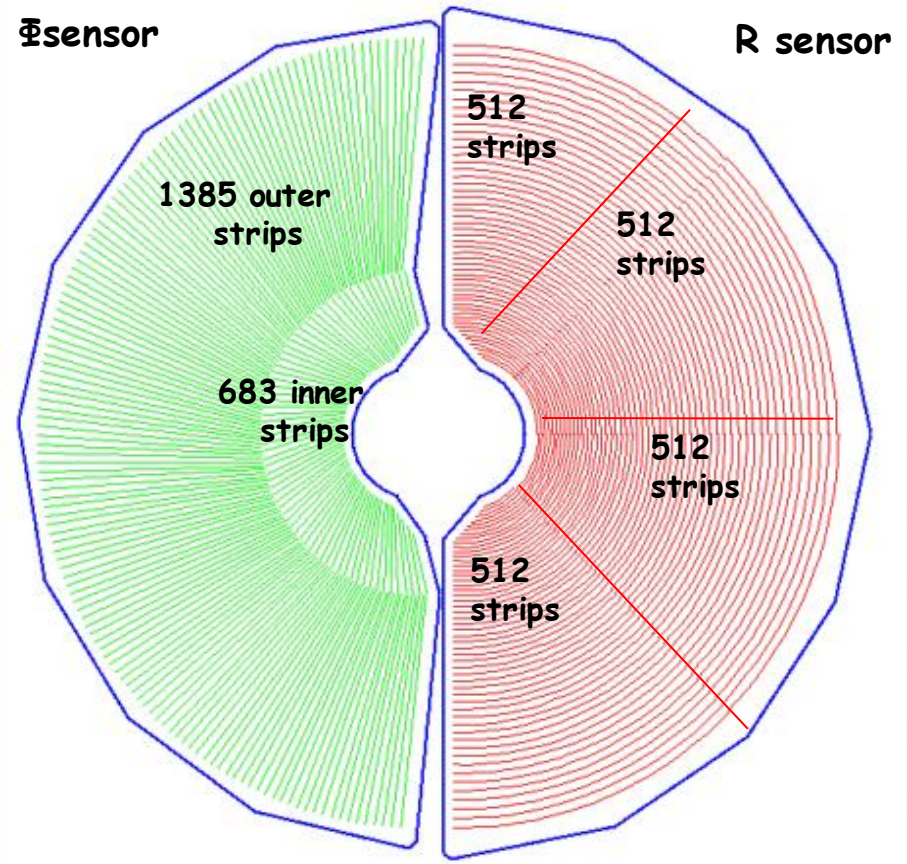
Also the physics expanded significantly beyond the plans

- charm physics (CPV, rare decays, spectroscopy)
- electroweak in forward direaction
- QCD
- lepton flavour violation

1) Measures the azimuthal angle

2) Stereo angle 20o for the inner strips (10o for the outer strips) ⇒ 2 regions

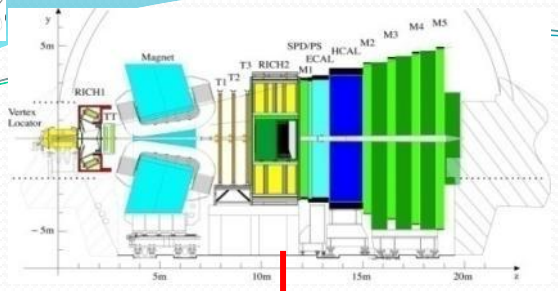
3) Pitch: 36 -97 μm

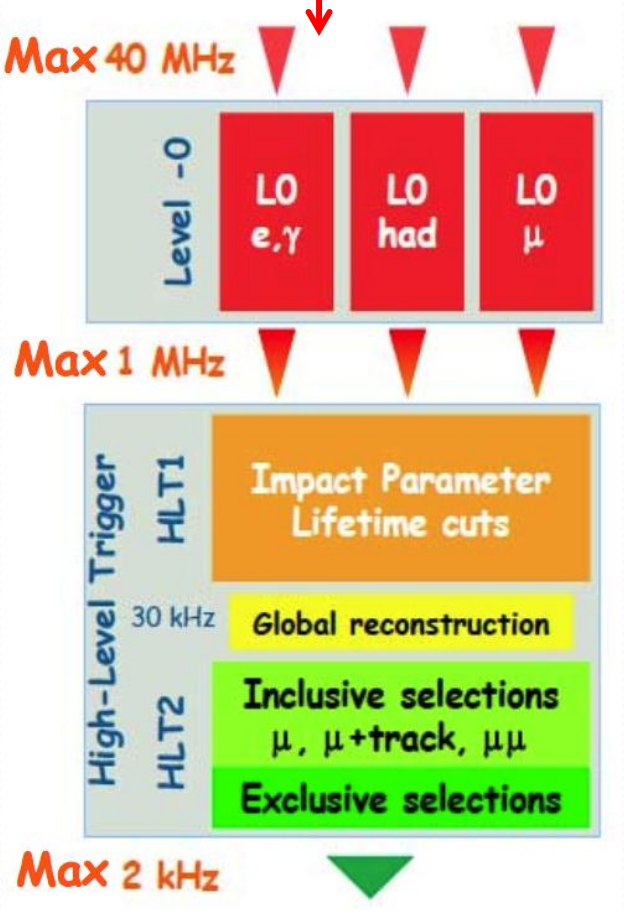


1) Measures the radial distance

2) Divided in quadrants

3) Pitch: 40 -102 μm





The zero-suppression for the VELO is done after the hardware trigger (L0) positive decision

For the current VELO it is done off-detector by the dedicated custom made electronic processing board – TELL1

The output of this board is called raw bank