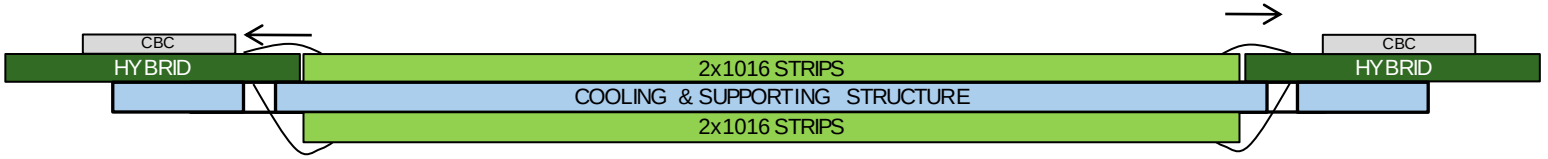
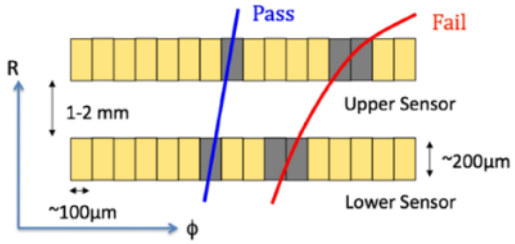
Hybrid circuits and substrate technologies for the CMS tracker upgrade

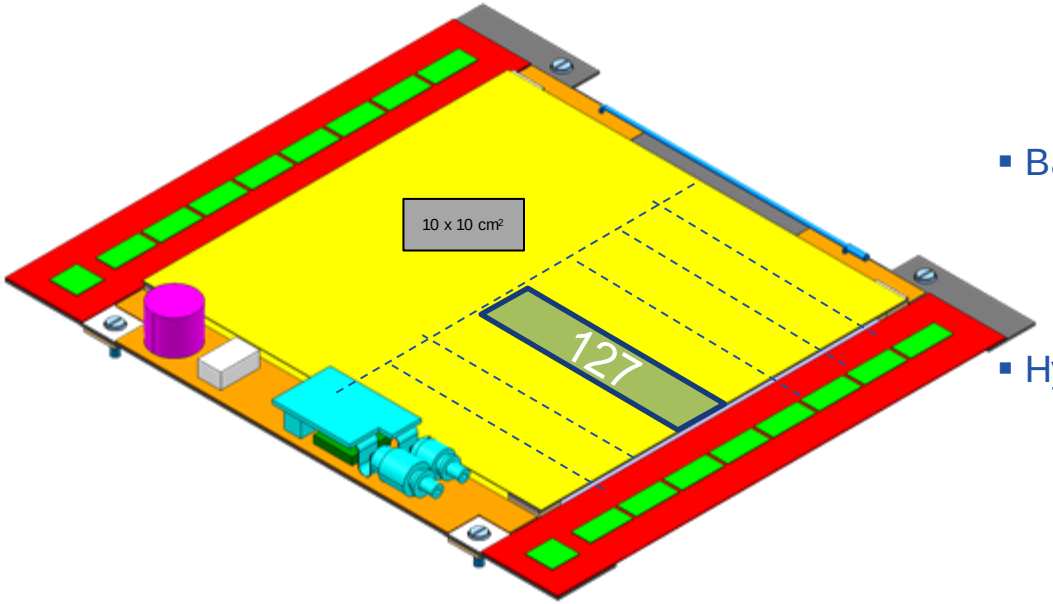
G. Blanchot

- CMS tracker upgrade.
- CMS tracker module types:
  - *2S*
  - *PS*
  - *VPS*
- Technologies for hybrid circuits
  - *Flip chip and wirebonding constraints.*
  - *Rigid substrates.*
  - *Flexible substrates.*
  - *Low cost TSV technology.*
- Ongoing development and conclusions.

- The increased luminosity at HL-LHC yields to new tracking requirements:
  - Higher rate of events.
    - *Increased granularity.*
  - Increased luminosity: 500 fb^{-1} → 3000 fb^{-1}.
    - *Improved radiation hardness for silicon sensors, front-end ASICs, mechanical components and electronic substrates materials.*
  - Reduced mass.
    - *In LHC, tracker mass is mainly contributed by services in the detector volume: power cables, cooling, ...*
    - *FE ASICS made with new technologies to reduce power requirements.*
    - *DCDC converters, Low Power GBT.*
    - *More efficient power delivery will result in less cables, less heat, less cooling → less mass.*
  - Level 1 tracking information.
    - *Low pT tracks rejection.*
    - *Track correlation between closely spaced sensors.*



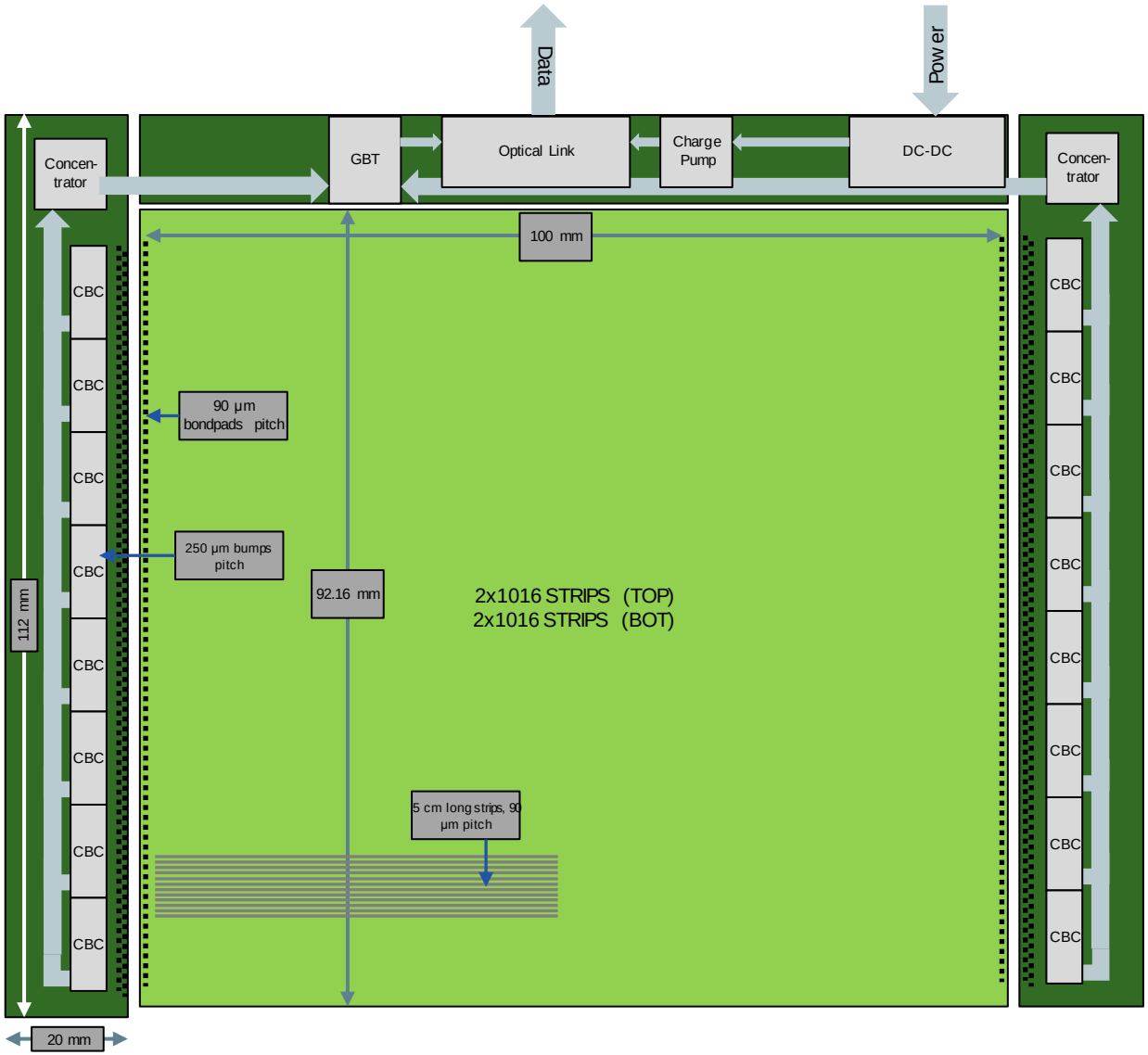


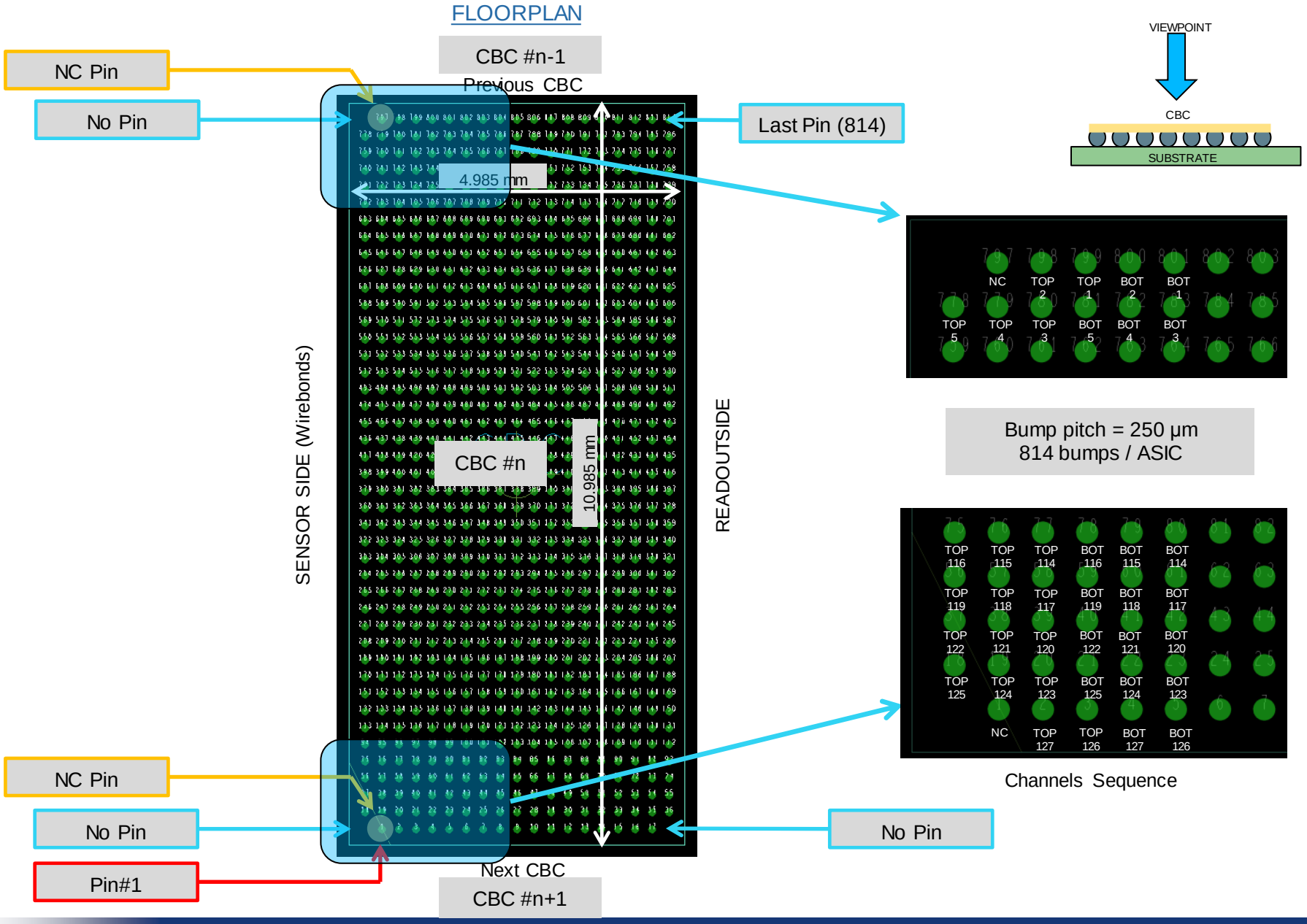


- Double sided strip module
  - Simple topology
    - *Low mass, no Z information.*
    - *Outer areas of tracker.*
  - Low pT rejection.
    - *Top/Bottom correlation create stubs.*
    - *Neighbouring chips interconnection*
  - Based on the CBC2 front-end ASIC.
    - *2*127 inputs per CBC2.*
    - *Flip chip assembly.*
  - Hybrid circuits:
    - *High density substrates to connect the CBC2 to the sensor edges.*
    - *Concentrator ASIC to merge data flows.*
    - *Service substrate to provide input power (DCDC) and data path (LP-GBT).*

2S-Pt Module: Hybrid Topology

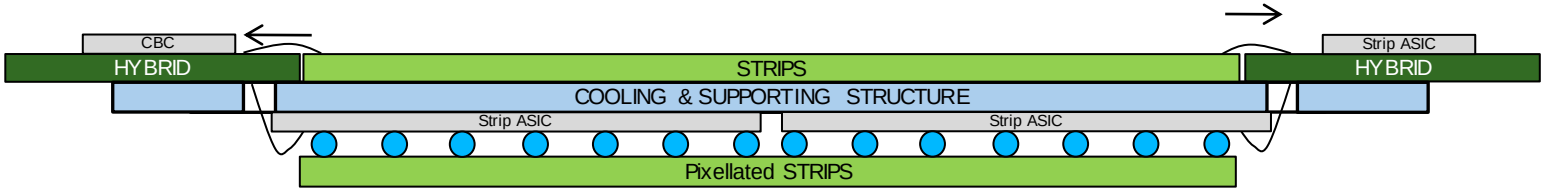
- Front-end circuit assemblies must have the minimum required area
- CBC connection to strips requires high density layout.
- CBC connection to concentrator requires several impedance matched pairs + single ended lines (bus), high density layout required.
- The two CBC sides share a common optical module and power converter.
- Options are:
  - U shaped single hybrid.
  - Frame shaped hybrid.
  - Two HDI hybrids plus one transverse service circuit.
  - This last option poses the problem of interconnecting the HDI substrates with the service circuit *without connectors*.

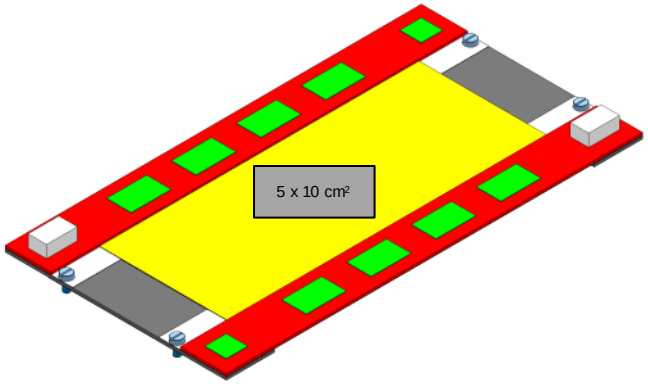


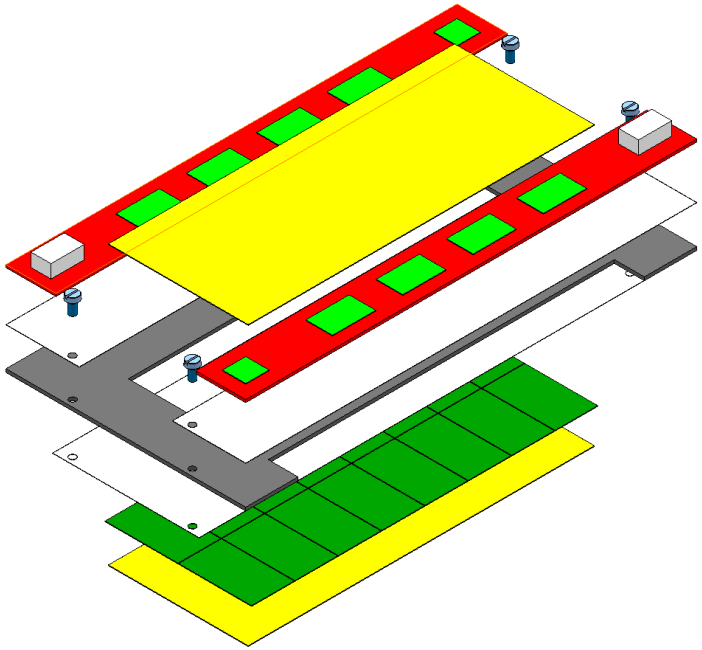

FLOORPLAN
CBC #n-1
Previous CBC
NC Pin
No Pin
Last Pin (814)
4.985 mm
SENSOR SIDE (Wirebonds)
CBC #n
10.985 mm
READOUTSIDE
NC Pin
No Pin
Pin#1
Next CBC
CBC #n+1
No Pin
VIEWPOINT
CBC
SUBSTRATE
NC TOP 2 TOP 1 BOT 2 BOT 1
TOP 5 TOP 4 TOP 3 BOT 5 BOT 4 BOT 3
Bump pitch = 250 µm
814 bumps / ASIC
TOP 116 TOP 115 TOP 114 BOT 116 BOT 115 BOT 114
TOP 119 TOP 118 TOP 117 BOT 119 BOT 118 BOT 117
TOP 122 TOP 121 TOP 120 BOT 122 BOT 121 BOT 120
TOP 125 TOP 124 TOP 123 BOT 125 BOT 124 BOT 123
NC TOP 127 TOP 126 BOT 127 BOT 126
Channels Sequence

Advantages of the C4'd CBC2

- Flip chip ASICs have several advantages compared with their wire bonded counterparts:
  - Having bumps under the ASIC allows getting rid of bond pads at the chip periphery:
    - No dead space required around the chips for wire bonding.
    - Chips can be abutted on all sides on the substrate.
  - Power and signal connections with less inductive parasitics:
    - The current is brought to the ASIC straight through a bump and not through an inductive bond wire.
    - The connection is less resistive too.
    - This is particularly important for the charge pump performance in the CBC2.
  - Wire bonds are sensitive to noise pickup:
    - The CBC2 bump bonding helps reducing the connection length to the sensor, hence reducing the E field coupling on it.
  - The assembled hybrids are fully connected:
    - It enables the testing of hybrids before they are assembled on modules and wired to a sensor.
- All this results in smaller board area, less mass and better performing front-end system.

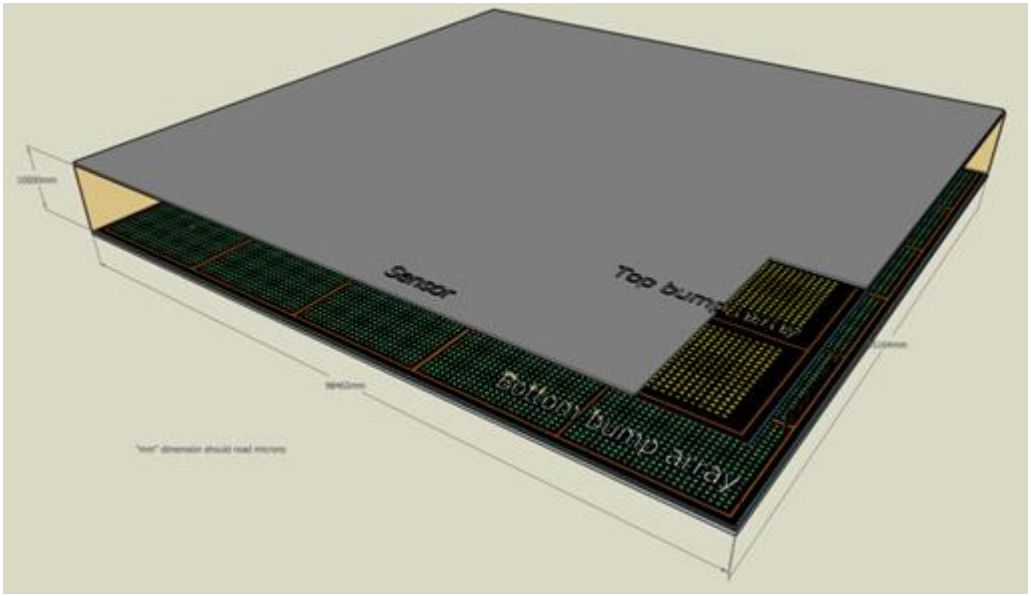


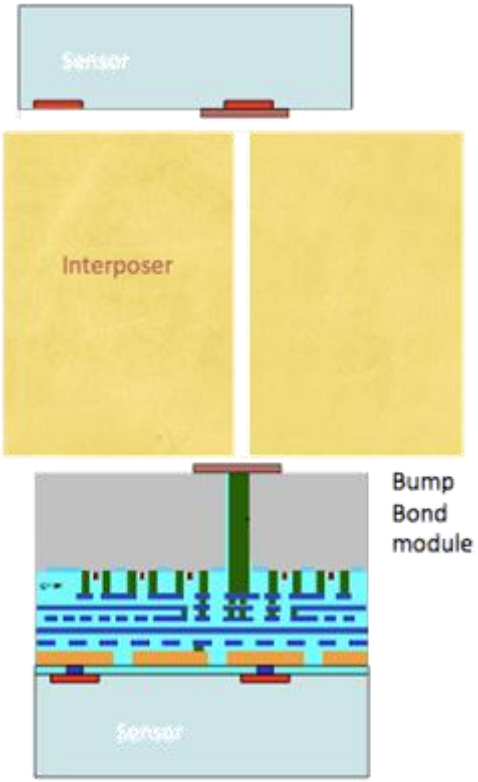




- Strip / Pixellated strip module
  - Pixellated strips
    - *Z information from 1.5 mm long pix. strips.*
    - *Pitch 100 µm.*
  - Low pT rejection.
    - *Pixel/strip correlation create stubs with Z info.*
    - *Correlation made in pixel ASIC.*
  - Requires 2 different ASICs
    - *Strip ASICs (CBC2 subset).*
    - *Pixel ASICs.*
  - Hybrid circuits:
    - *High density substrates to connect together the top strips, the pixel ASICs and the strip ASICs.*
    - *Concentrator ASIC to merge data flows.*
    - *Half width service board that must deliver more power and same GBT link.*

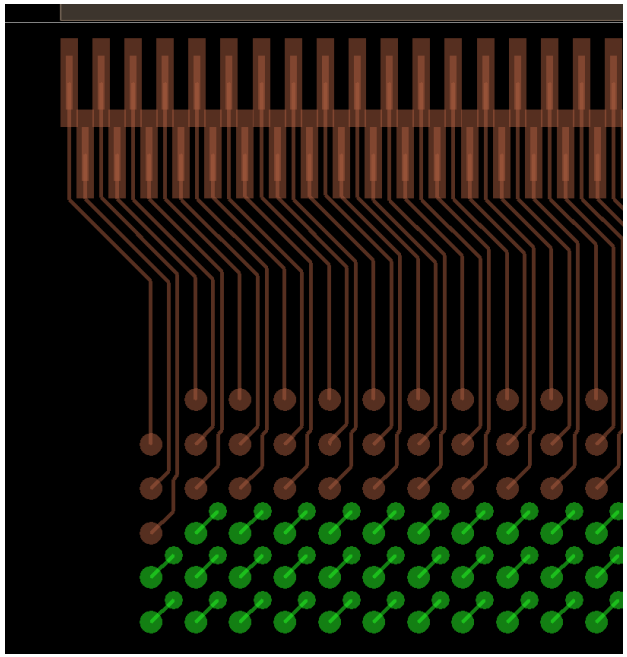
- Substrates technologies addressed here cover 2S-Pt and PS-Pt modules.
  - 3D-Ps module shown here for completeness of module types list.
  - Refer to M. Johnson slides on 3D Tiles.





Flip chip and wirebonding constraints

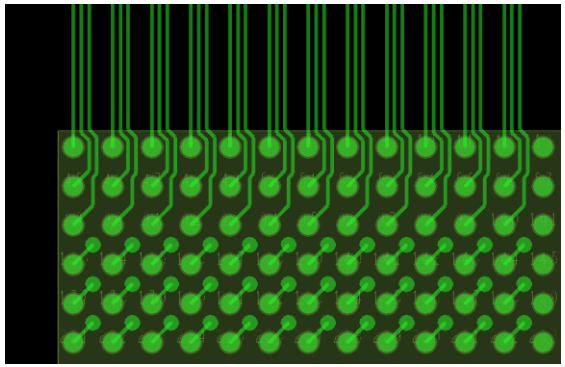
The high density flip chip array imposes the need for high density interconnection substrates.
For example, sensor wirebonding: 25um traces required for straight connection to bond fingers.



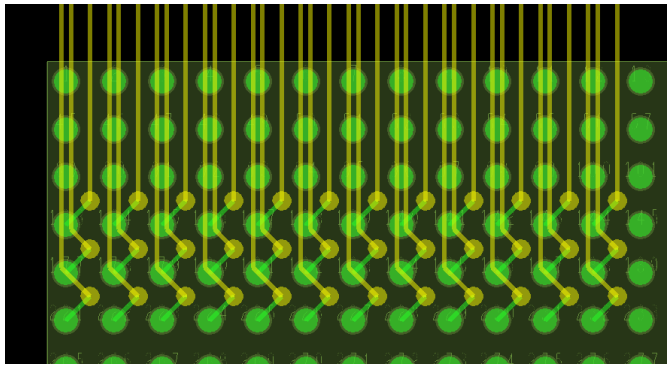
- Top sensor bond fingers can be in-line or staggered
  - In both cases, the wirebond pads are very close of the sensor edge.
  - Traces escape all in same direction without need of vias.
  - Traces can still go through 2 adjacent vias without turn arounds.
- Sensor bond fingers are present at same locations on the bottom side:
  - The connection is possible through the CBC pin escapes via array from the 3 last rows.
  - The 3 top rows are associated to the top side sensor.
  - Microvias, 50 µm drill, 100 µm capture pad are required.

Rigid and flexible substrate technologies are today available with these degree of interconnection densities.

Rows 1, 2, 3: top sensor, straight connection.



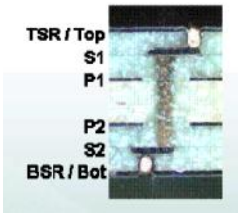
Rows 4, 5, 6: bottom sensor, straight connection through pin escapes.



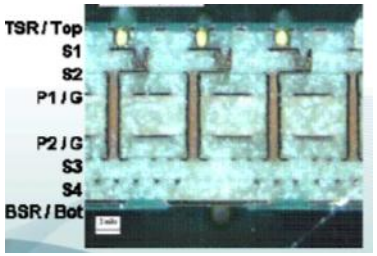
- **Build-up substrates are commonly used for chip packaging.**

  - Core layer provides:
    - Power/Ground planes
    - Rigid core material.
    - Mid density routing and through hole vias.
  - Build-up layers are laminated on top and bottom of core:
    - Very high density interconnections on constrained areas.
    - Microvias to connect build up layers to core external layers.
    - No through hole vias..

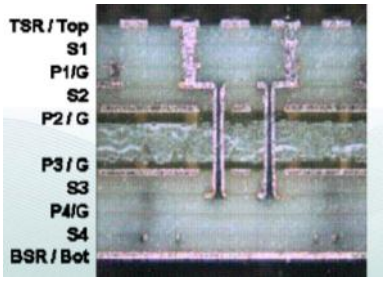
6 layers



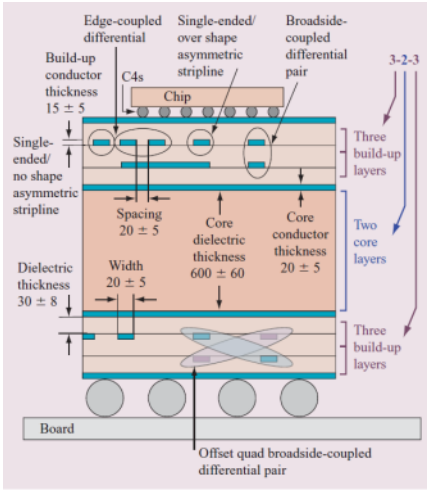
8 layers



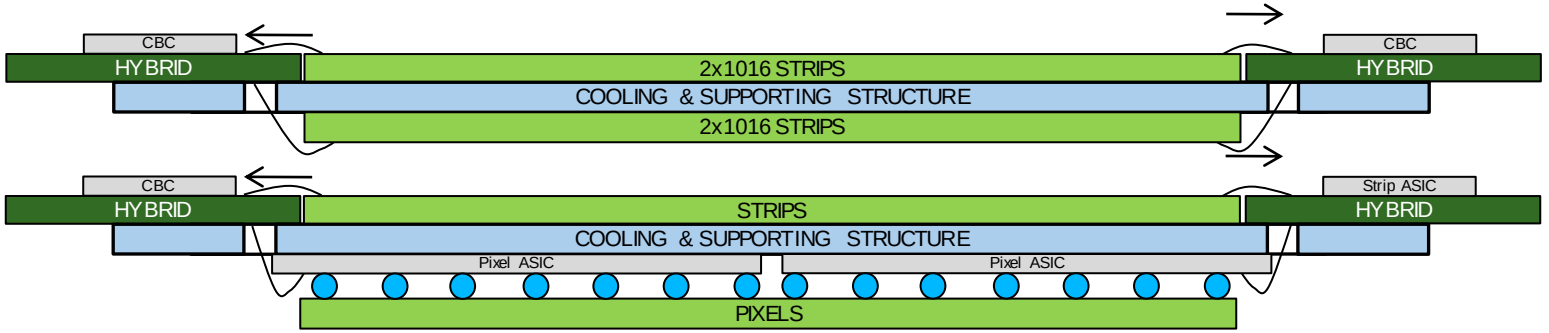
10 layers

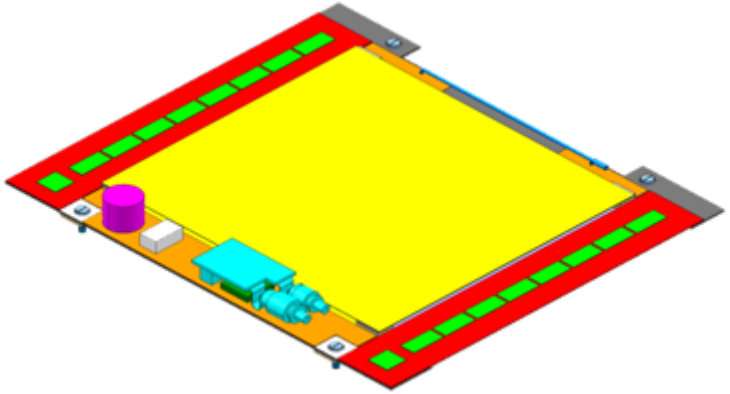


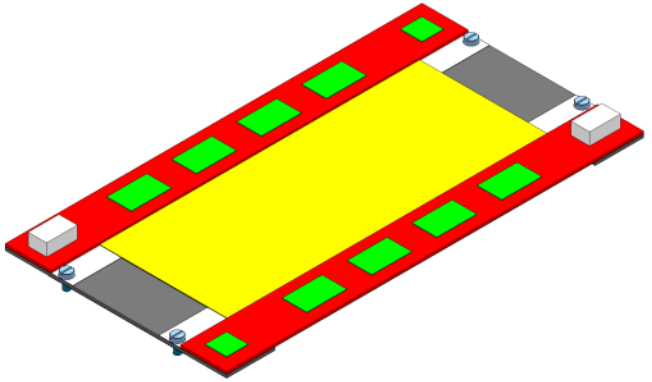
Typical application



Build-up substrates applied to CMS Tracker modules







Rigid, organic build up substrates offer a standard baseline construction for the 2S and PS modules.

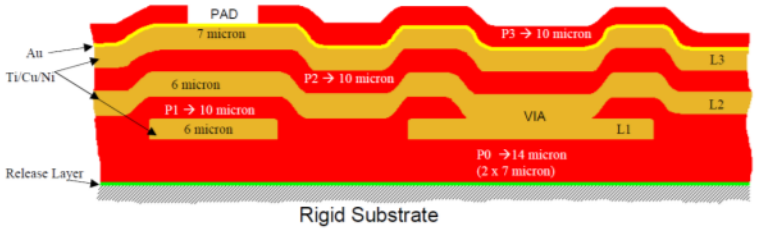
The routability has been confirmed using a 1-4-1 build up structure.

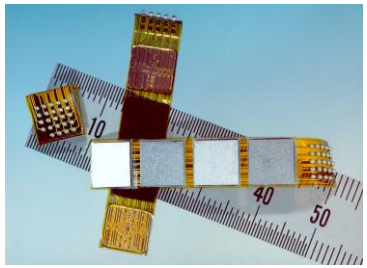
Non negligible mass, but power distribution is adequate to feed the ASICs.

Mechanical integration to be studied: glueing on cooling structure, interconnection with the service board, flatness for wirebonding and bump bonding, wirebonding through groove for bottom sensor.

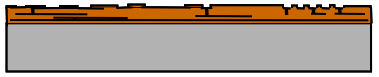
Flexible polyimide is a quickly emerging technology.

- Thin film flex technology made of spinned liquid polyimide on square panels.
  - Very high density layouts: Tracks w/s = 20 µm, microvias = 30 µm.
  - Silicon matching CTE = 3 ppm/K.
  - Very low mass: Cu thickness < 7 µm, film thickness ≈ 10 µm.
  - However: 4 layers maximum, no copper on base layer, limited power delivery capabilities.

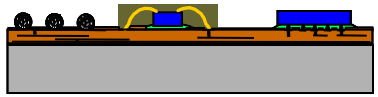




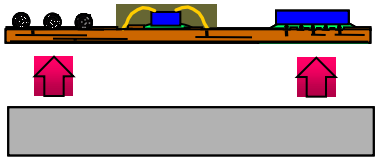
Fabrication of Multilayer Structure on Rigid Carrier Substrate

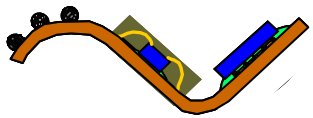


Assembling, Bonding, Protection , Test



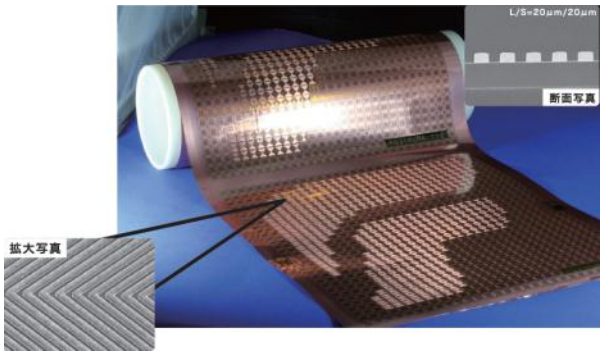
Separation of Multilayer from Rigid Substrate Reuse of Carrier





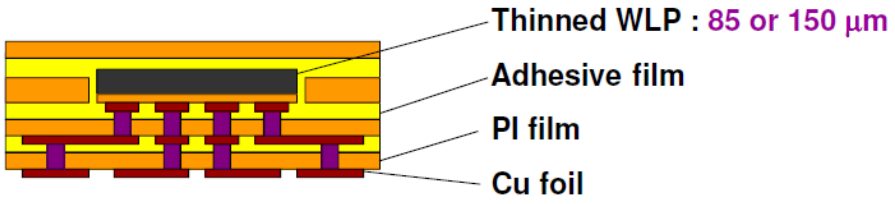
- **Packaging industry is adopting this technology for large volume and integration.**

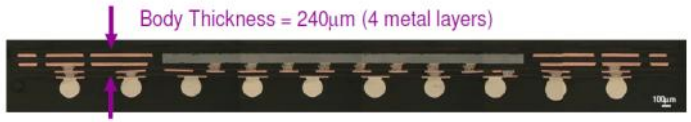
- Several suppliers are today available for panelized flex films.
  - They all provide very high density, small microvias, thin foils on limited number of layers.
  - Flip chip compatible, wirebonding compatibility to be evaluated.
- Trend is now to use this technique for:
  - Roll to roll lamination of flex circuits for very large volume productions.
  - Embedding of dies into multilayer system in package overmolded structures.



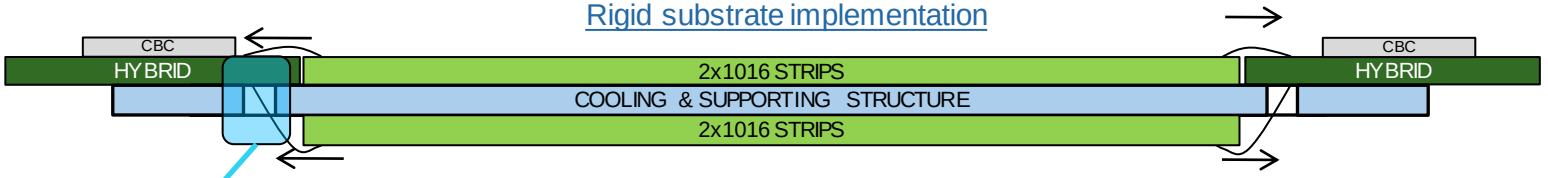
IMAPS MINAPAD Forum
Grenoble, April 2012.

Ultra slim package due to the thinned WLP die and multilayer flex based structure.

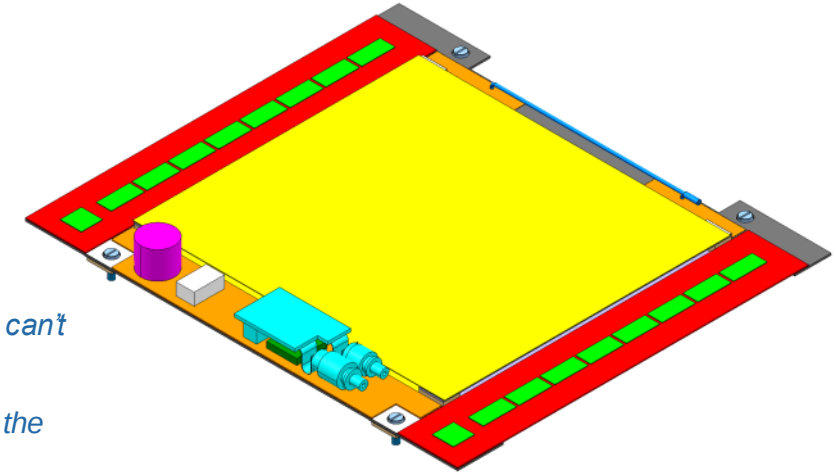




Rigid substrate implementation



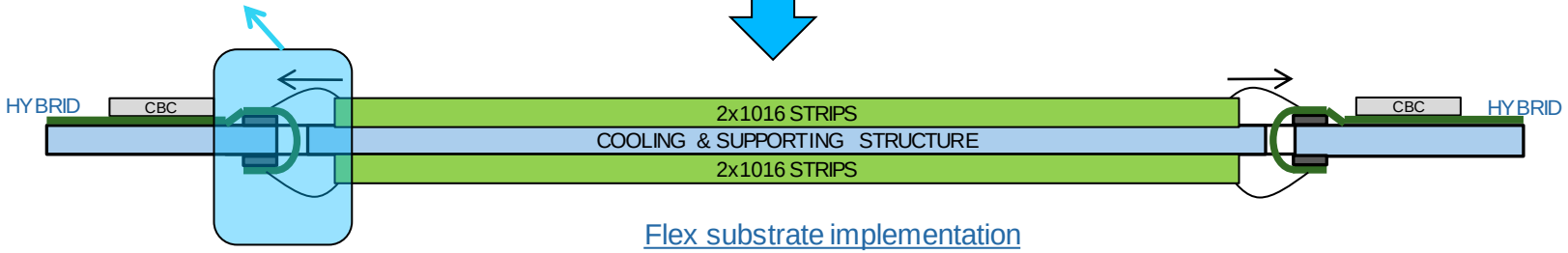
Bottom layer wirebonded through a slot window in the carbon fiber frame.



Flex foil provides pads only on top layer: can't bond to the bottom side.

Bond pads reinforcement on the base of the flex, under the bond pads.

Folding the flex in the slot window of the frame.

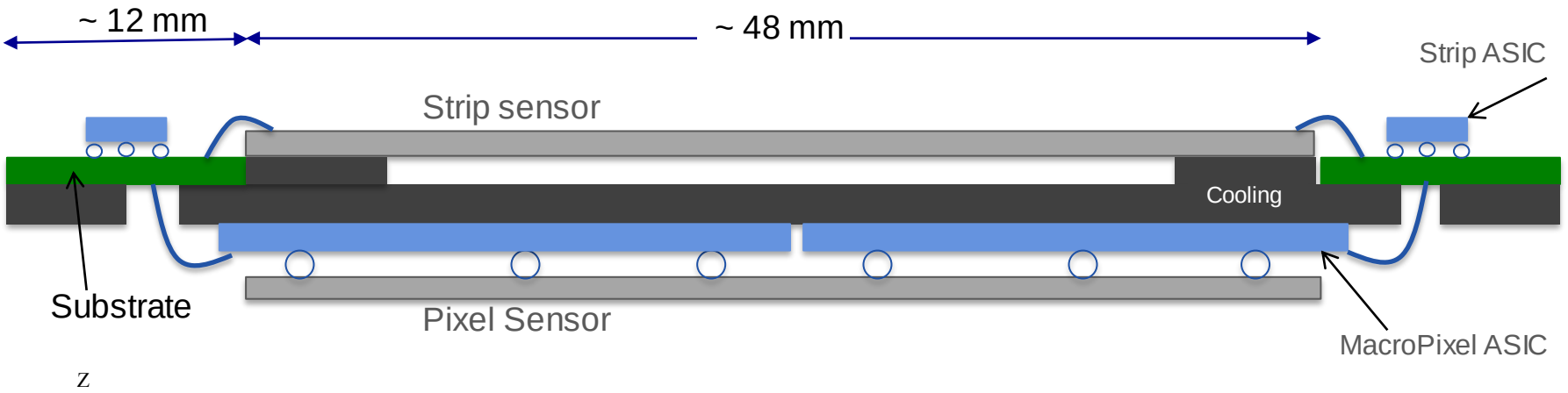


Flex substrate implementation

TSV option for PS-Pt modules

Wirebonds through window.

Power distribution through Silicon



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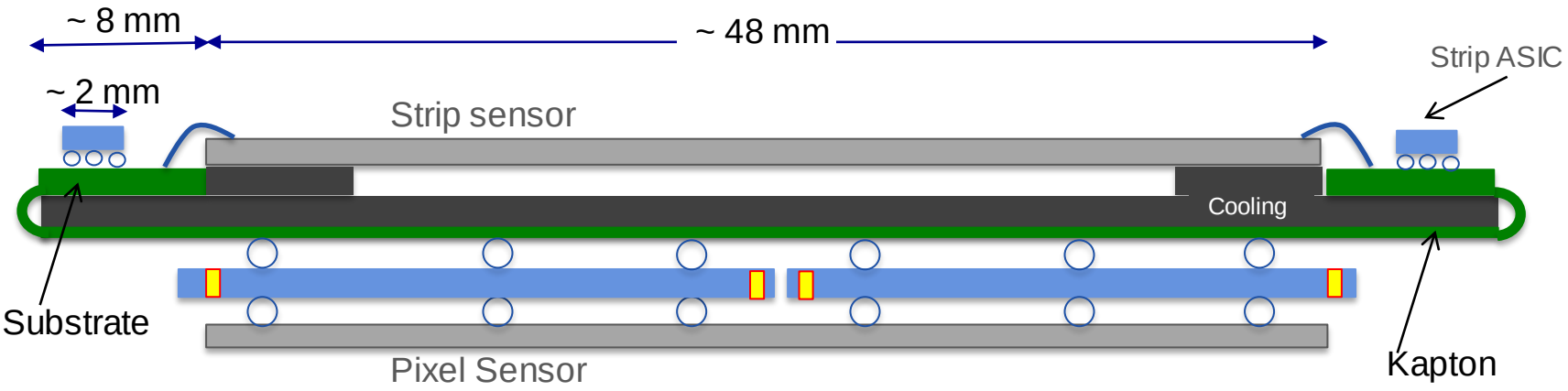
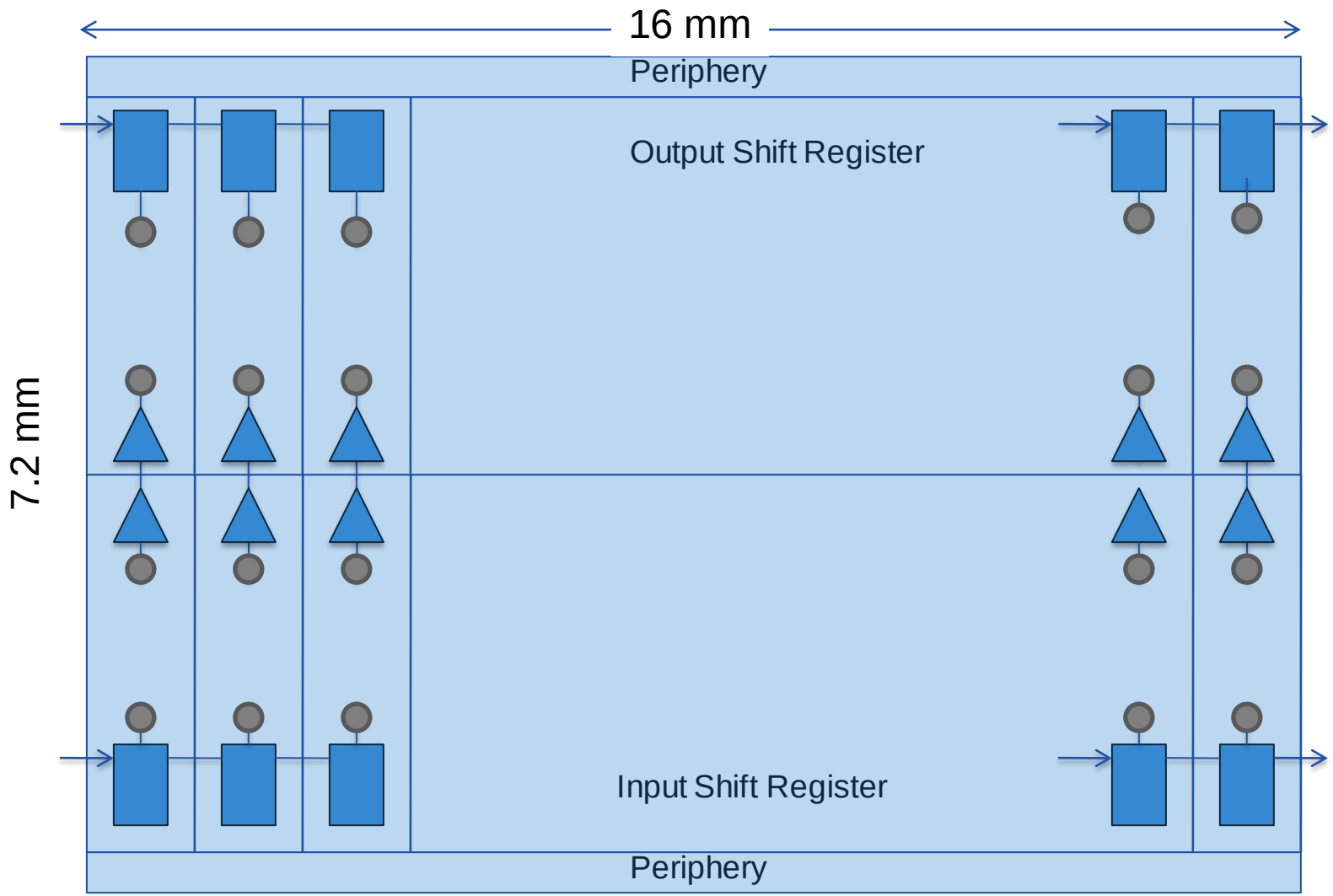


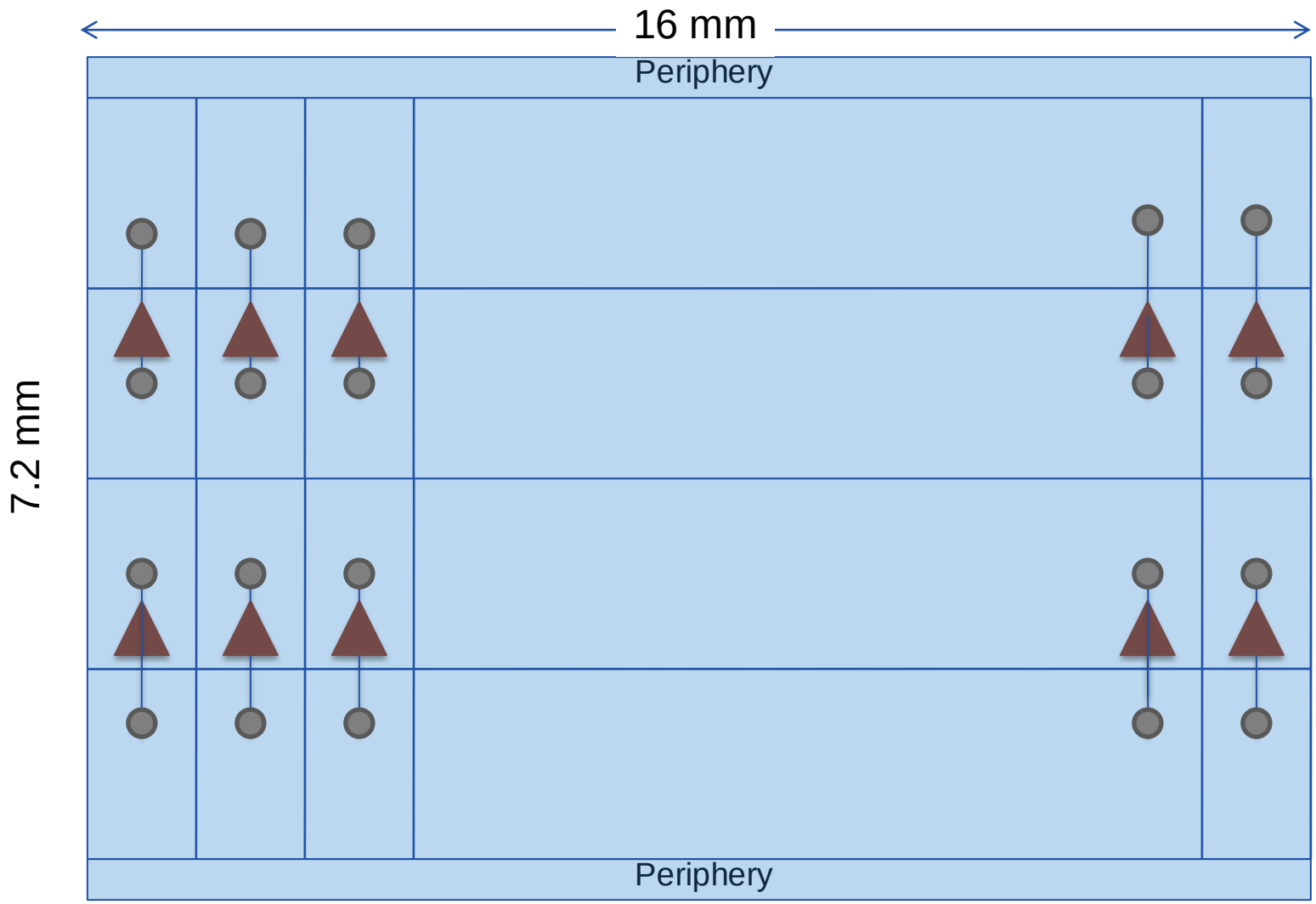
Single piece flex substrate.

TSVs for better power delivery inside the dies.

Wirebonds top side only



ASIC emulator: Lower layer chip



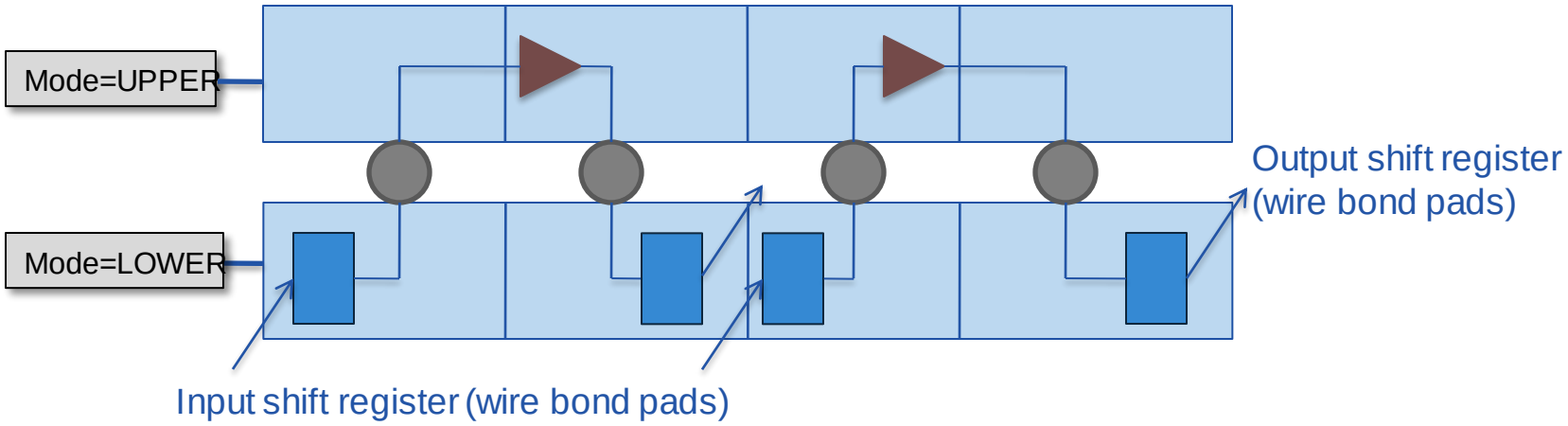
Sensor emulator: Upper layer chip

Slice: see next slide

Test patterns are shifted into the input shift register.

The patterns flows between the 2 chips, through the bumps.

The pattern is read out from the next output shift register at the end of the chain.

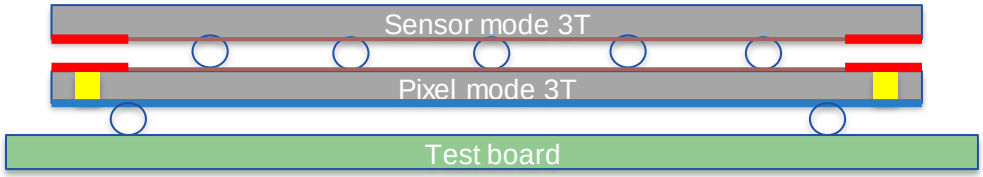


Upper layer chip

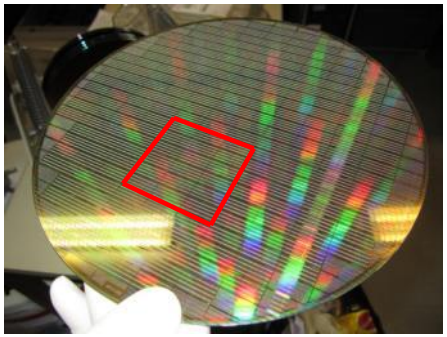
Lower layer chip

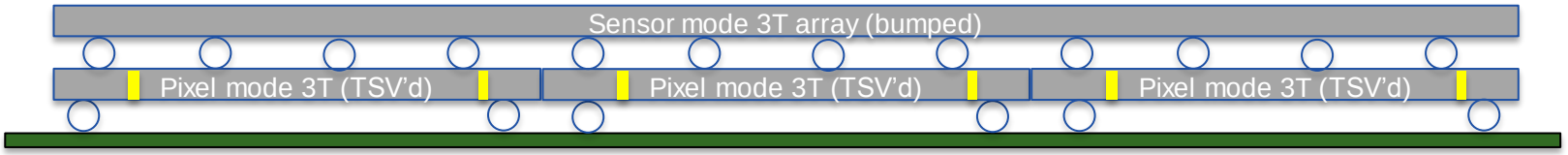
3T: 3D integration demonstrator for PS-Pt

- Etching of TSVs
  - Low cost, 75 µm diameter, 100 µm pitch TSVs.
  - Wafers bumped, with TSVs.
- Testing of a standalone 3T stack
  - Bump bond 3T chips together.
  - Design standalone test board for bump bonded stack.
  - Test standalone stack.
  - Expected: end summer 2012.



- Testing of 3T array structure
  - Dice an array of 3 × 6 bumped chips in one piece.
  - Bump bond TSV'd chips with the sensor array, abuted on alll sides..
  - Design array test board.
  - Testing.
  - Expected: end 2012.





- **The CMS Tracker modules requires high density hybrids:**
  - Rigid substrates offer a baseline solution.
  - Flexible polyimide substrates brings new integration options to reduce size and mass.
  - Both solutions achieve the required density of routing.
  - A prototype is currently in development for a 6 layers rigid build up substrate for the 2S-Pt modules.
- **The TSV technology is being explored for better integration of PS-Pt modules**
  - Large TSVs in pixel ASICs would allow better integration of the pixel ASICs.
  - Low cost TSVs are being evaluated on the 3T demonstrator ASIC.
  - Results expected on this front by end 2012.
- **The flexible polyimide is quickly being adopted by the packaging industry.**
  - Embedding of dies and passives into laminated structures could bring new perspectives for the design of hybrid circuits for trackers.