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# A fast digital readout architecture for vertically integrated pixel sensors

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A digital architecture for fast sparsified readout has been developed for the implementation of wide 3D pixel sensors. The Italian VIPIX collaboration is realizing two prototypes exploiting the Tezzaron-Chartered vertical integration process in order to build a 12k-pixel 3D deep n-well MAPS sensor, and a 3D 4k-pixel front-end chip, with 50 um pitch, for a fully depleted silicon sensor. In both cases the digital and analog circuits are implemented on dedicated tiers in order to reduce the digital noise induction and enhance the digital logic at pixel level. The dense in-pixel logic allows for innovative sparsified hit extraction techniques, in order to reduce the pixel occupancy. The readout logic we propose can face an input hit rate of the order of 100MHz/cm2 and allows a time resolution of 100 ns, in addition it can be configured to work in data-driven or triggered mode.
The technology process is a Chartered CMOS 130 nm, this feature size presents an intrinsic radiation tolerance and allow the use of foundry's standard cells. The architecture has been deeply investigated in terms of efficiency on a wide span of input parameters (hit rate, time resolution, trigger latency etc.) thanks to a parameterized VHDL synthesizable model, that has been designed to match even larger matrices of pixels. The model was stimulated within a complex test bench environment that included a Monte Carlo generator for the hit extraction, a simulation monitor and a C++ framework for the efficiency analysis and error detection. The flexibility of the code allow to easily tailor the architecture and of the test bench on different matrix dimensions: we observed this scalable architecture working properly even with bigger matrices, of the order of 50k pixels.
The paper presents the readout efficiency versus a variety of parameters as the clock rate, the pixel hit-rate and
the time-stamp resolution. The overall project leads to design a high-density thin vertex detector with an on-chip
sparsified digital readout system, for particle tracking, aimed at matching the requirements of future high-energy physics
experiments like SuperB.

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