Contribution ID: **48** Type: **not specified**

Asynchronous readout architectures for Tracker Front-End ASICs

Friday, 4 May 2012 12:00 (30 minutes)

We preset a design of a front end ASIC that combines a level 1 trigger and normal event readout. It uses asynchronous logic through out the design to reduce both power consumption and noise sensitivity. The only clock used is the 40 MHz LHC clock. A test chip based on this design is planned to be submitted in July of this year.

Summary

The use of architectures based on asynchronous logic represents an innovative approach in the readout of Front-End circuits for Silicon Trackers. These architectures have several key advantages with respect to traditional synchronous architectures. First, when there is no data most of the circuitry remains inactive with a significant saving in power. Second, there is no need for a high frequency clock which reduces potential noise sources. Finally, the digital circuits operate over a much wider frequency range than clocked ones and therefore the power spectrum will not be concentrated in a restricted set of frequency values. This will reduce noise and make shielding easier.

An architecture based on asynchronous "mousetrap"pipelines has been developed for a possible upgrade of the CMS Silicon Tracker. This design supports a level 1 trigger as well as conventional silicon readout. We describe in detail the behavior and the timing performance of this readout architecture as well as the methods used to minimize the effect of noise and single event upsets

This architecture has been mapped into a Standard Cell library for the IBM CMOS 130nm technology. A custom approach in the placement and routing of the Standard Cells has been chosen in order to optimize and equalize delays along the asynchronous pipelines. A test ASIC is currently under development and it will be submitted for fabrication this summer. The only clock on-chip is the 40 MHz clock used to synchronize data acquisition with the LHC bunch crossings rate. All data transmission within and between ASICs is via asynchronous logic. Data is converted to synchronous logic at the connection to the optical transceivers (GBT). The test ASIC and a possible module architecture based on it will be described in detail.

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Session Classification: On-module electronic circuits (3D and conventional), intra-module and off-detector communication

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