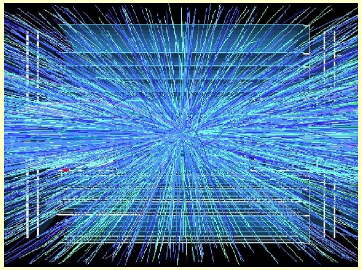
WIT2012 Workshop on Intelligent Trackers



A Self Seeded First Level Track Trigger for ATLAS

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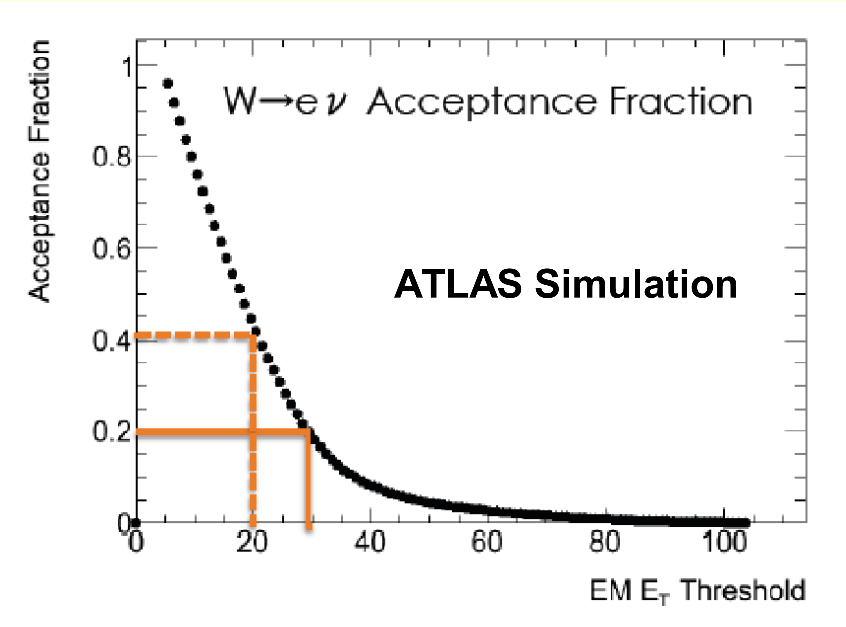
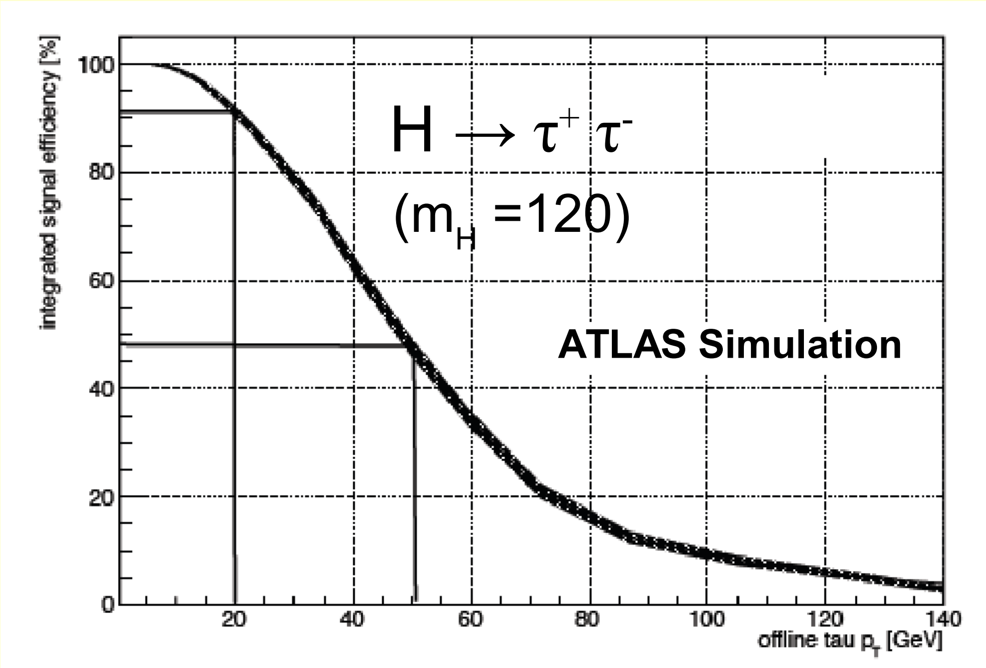
Motivation

- Today, no clear picture about full spectrum of physics analysis at Phase II (L=5·10^{34} cm^{-2} s^{-1} , Year>2022)
- Need to design a robust and flexible L1 Trigger system that can cope with the unexpected, i.e. with enough redundancy
- Many of the scenarios we can think of today involve objects at (or near) the **electroweak scale**

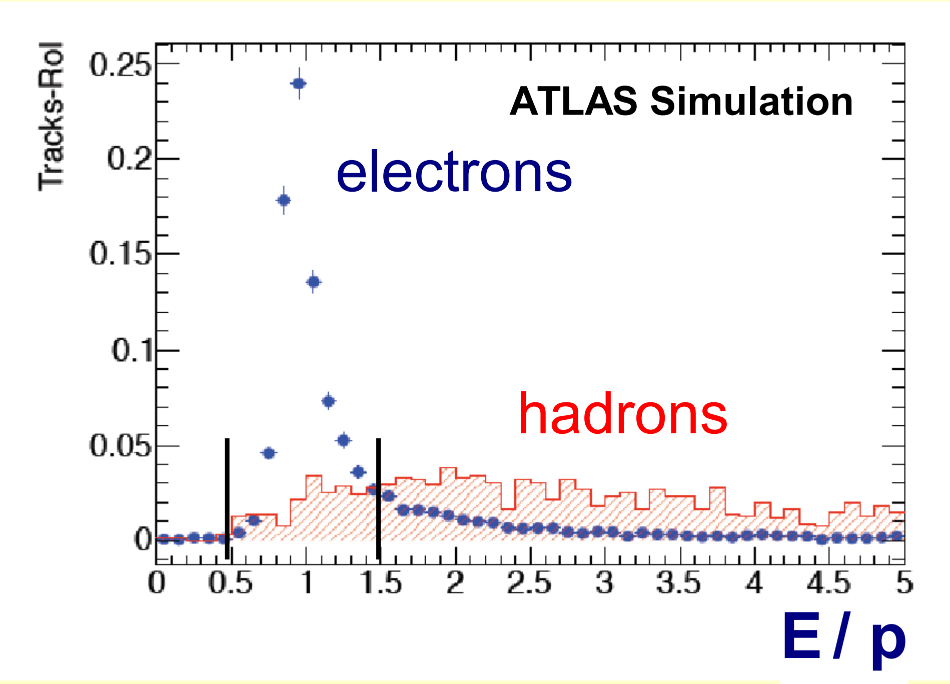


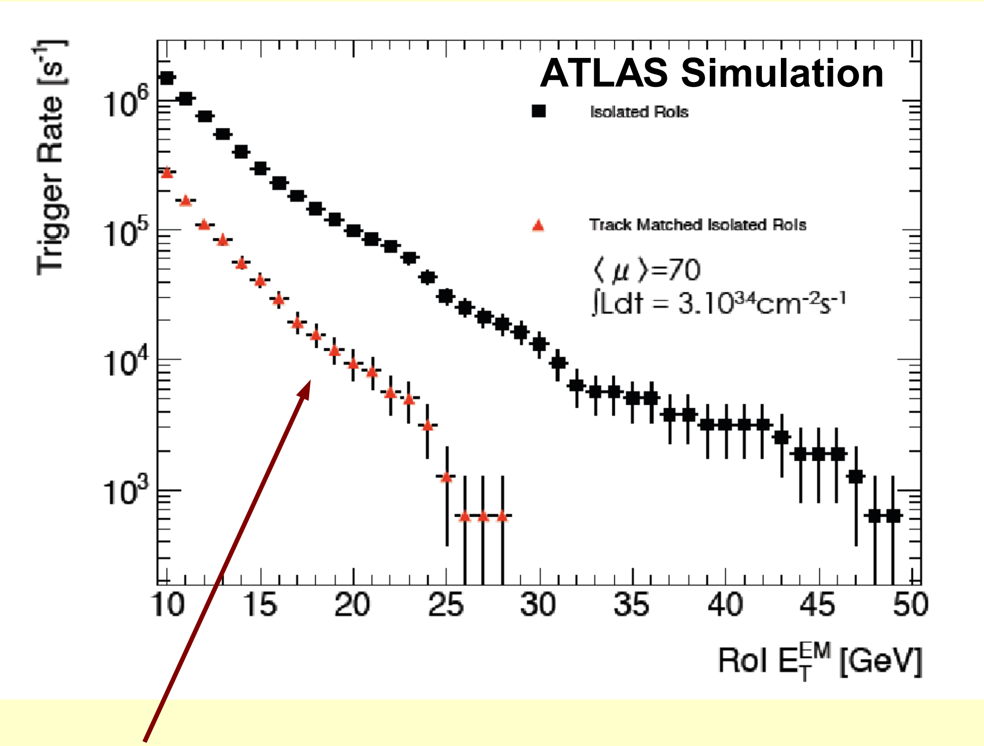


First studies show that track matching at L1 allow for **~20 GeV** object triggers (**e,μ, τ**)

Rate Reduction using Track Cluster Match

Using track-cluster matching in **E / p**, a rate reduction of up to a factor **~10** can be achieved





Challenges of L1 Track Trigger

Challenges

O(10^7) channels in strip detectors

O(10^8) channels in pixel detectors

O(5000) central tracks per collision at LHC phase II

O(10) Tbit/s data in tracker central region

Simplifications → Data Reduction

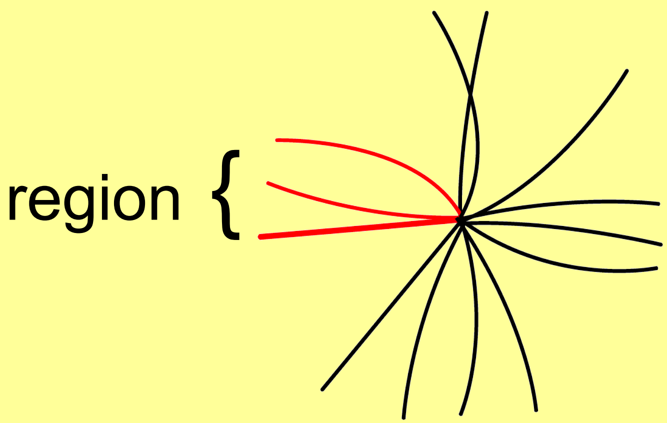
- **only (selected layers of) strip detectors**
- **reduce data rate by:**
  - **regional filtering → Region of Interest Track Trigger**
  - **kinematical filtering → Self Seeded Track Trigger**

Trigger Bandwidth Solutions

two baseline concepts for L1 Track Trigger in ATLAS:

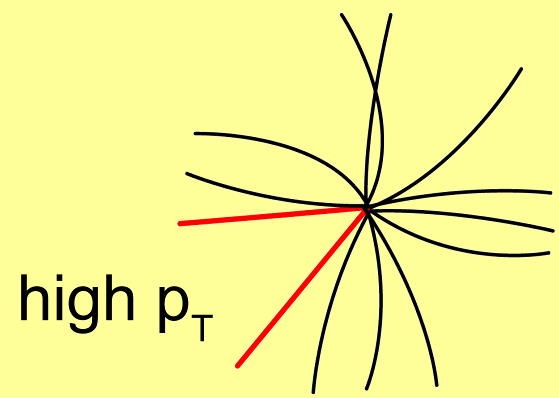
"Region of Interest"

- spatial cluster filter
- external trigger information (calo, muon, ...)
- new level L0 trigger required
- all tracks in regions



"Self Seeded Track Trigger"

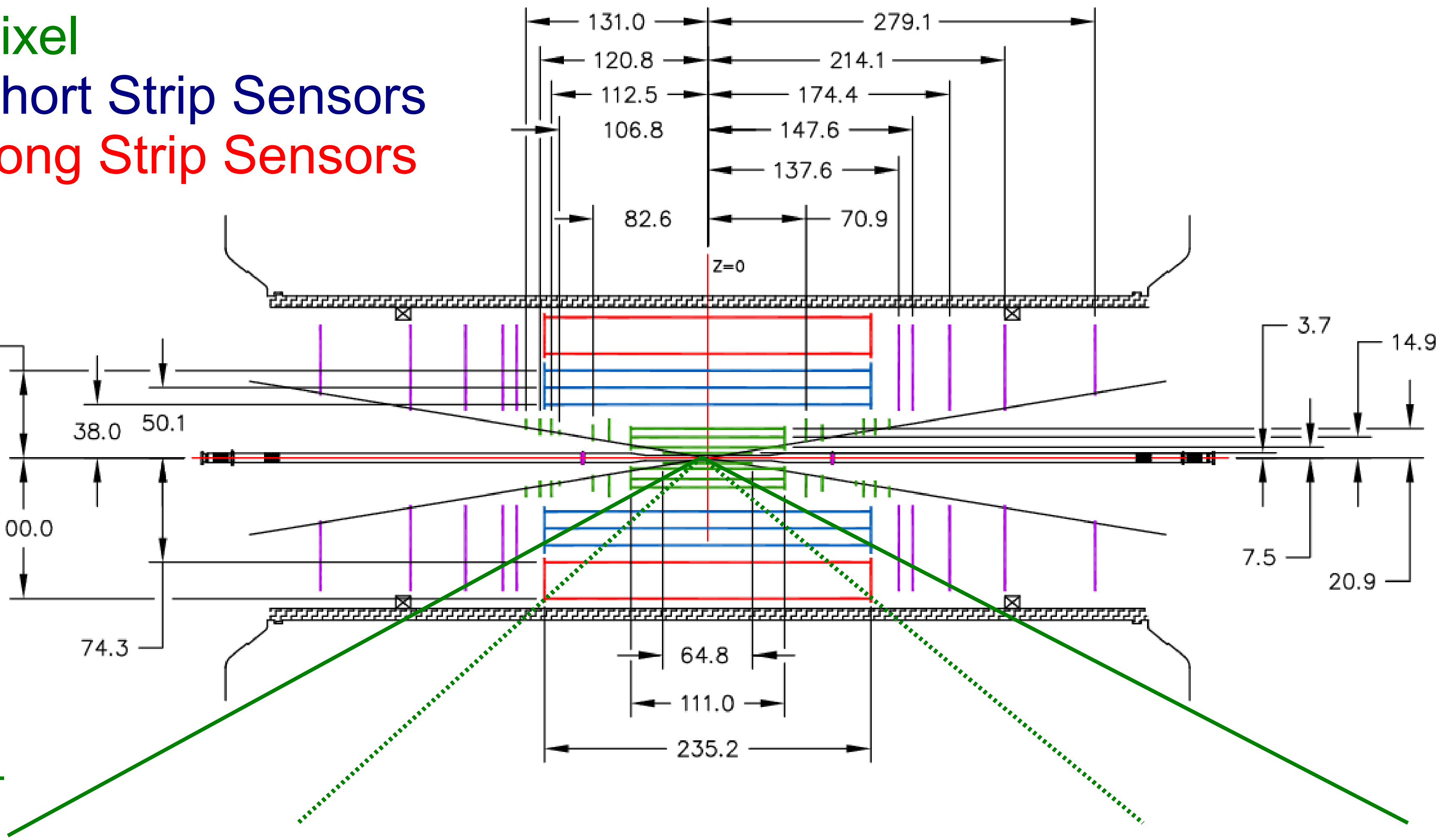
- momentum filter of clusters
- cluster size + local coincidence
- special HW design required
- all high p_T tracks



Double Frontend Buffer → talk D.Wardrope

Utopia Geometry

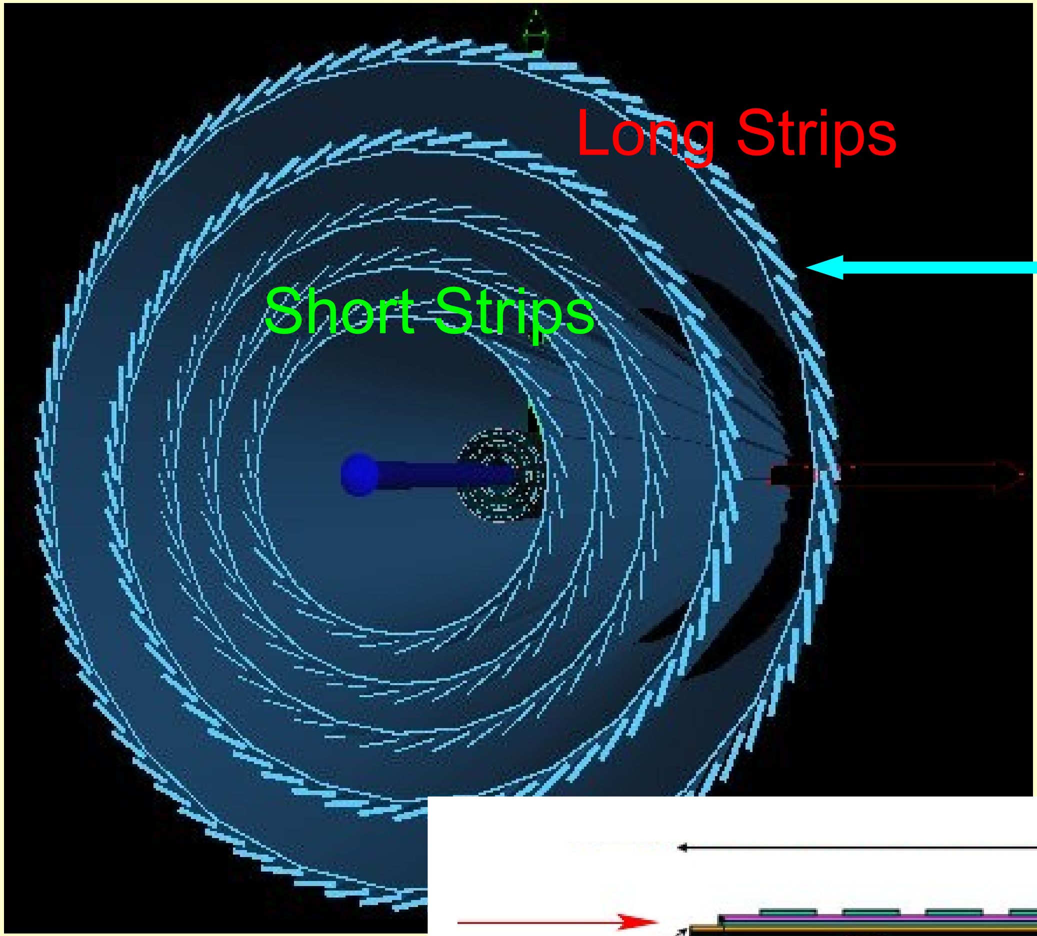
- Pixel
- Short Strip Sensors
- Long Strip Sensors



eta=1.4

studies only for central region

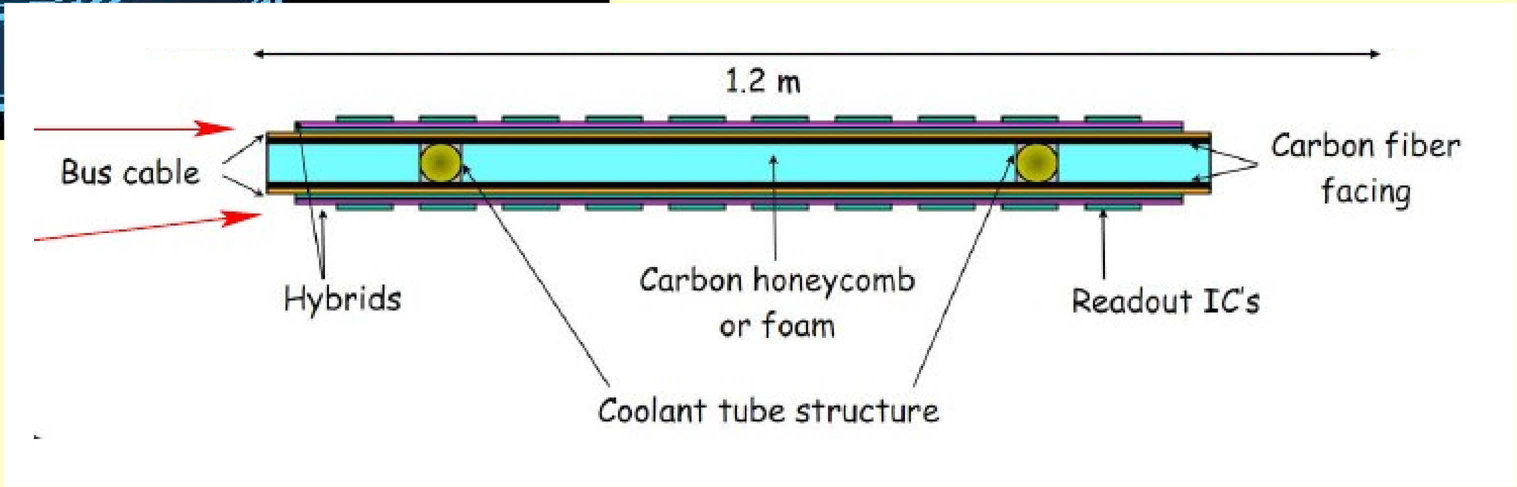
ATLAS Utopia Strip Layer Design for Phase II



<u>Double strip layers</u>

- gap 7.35 mm
- tilted by 10 (16) degrees
- 80 µm pitch
- stereo angle (standard)

→ no stereo angle for track trigger

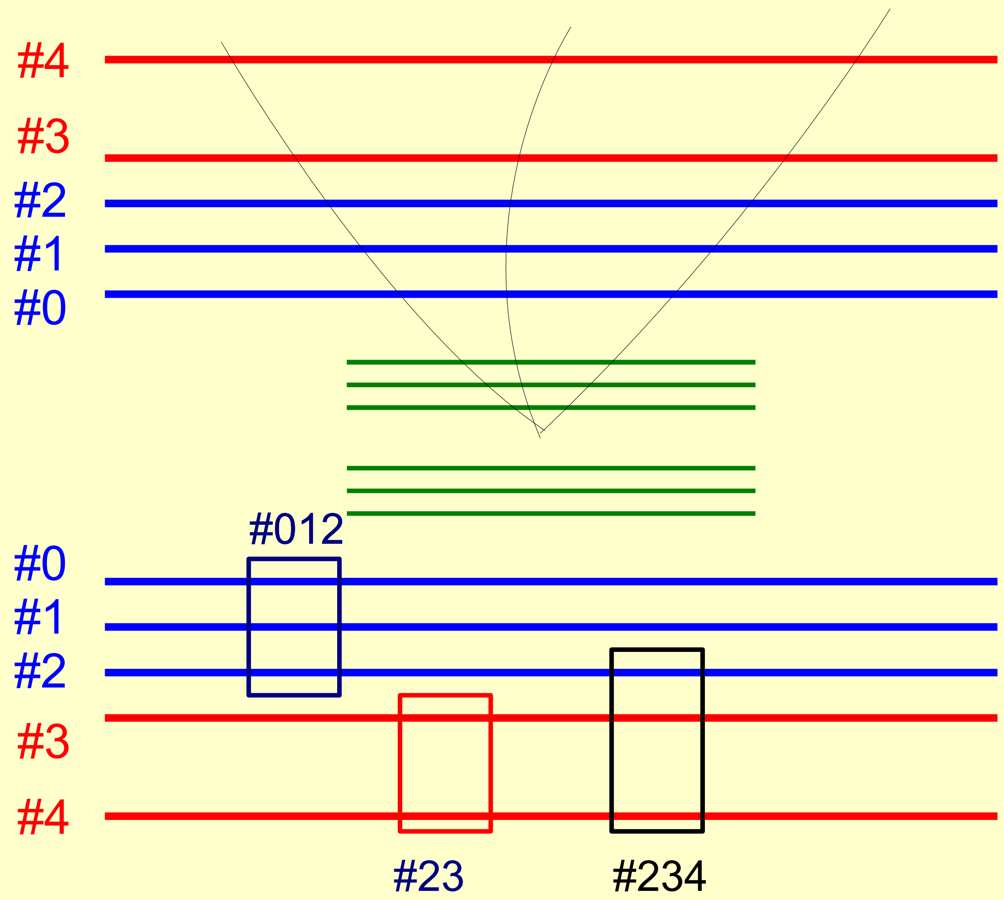


Pixel + Strip Sensor Layers

Long Strips (*Δz=10cm*)

Short Strips (*Δz=2.5cm*)

Pixel (not used)



Layer combinations studied for track trigger:

- #0, #1, #2 (only short strips)
- #3, #4 (only long strips)
- #2, #3, #4 (mixed, outer layers)

Questions addressed

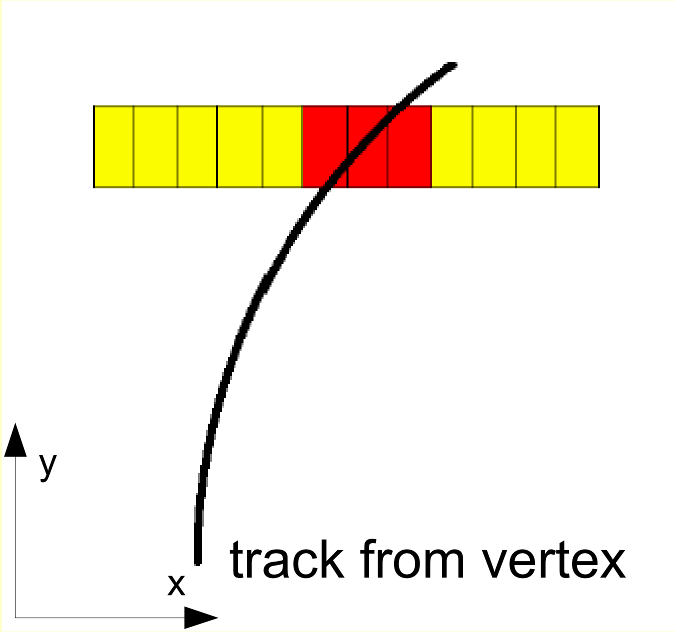
- **Study of high p_T local filter algorithms (Frontend)**
  - cluster size filter algorithm
  - "offset method"
- **How many silicon double layers for trigger (2,3,4,...)?**
- **Best layer combinations?**
  - study combinations "012", "34", "234"
- **Performance:**
  - data reduction versus p_T-threshold
  - data reduction versus track finding efficiency

  - Most results taken from diploma thesis of **Arno John**, Heidelberg

Cluster Size Filter

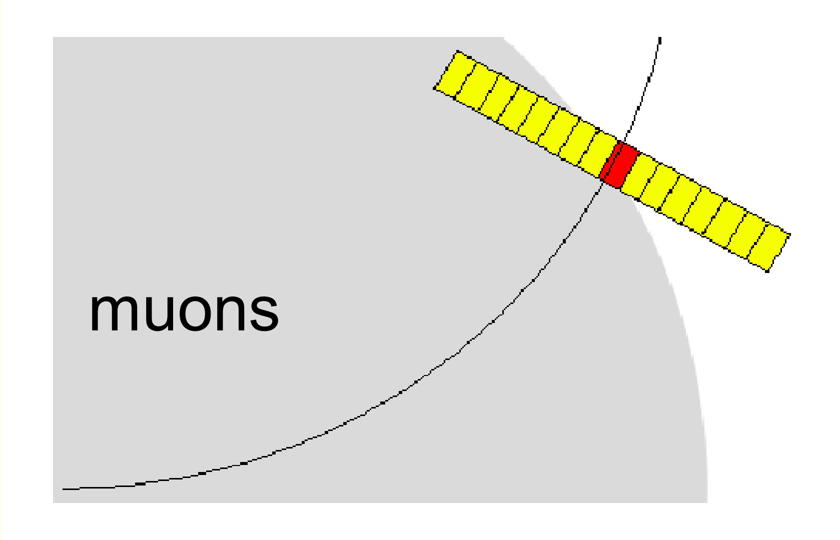
Due to the rectangular strip geometry several strips collect charge if low momentum tracks are bent in the magnetic field

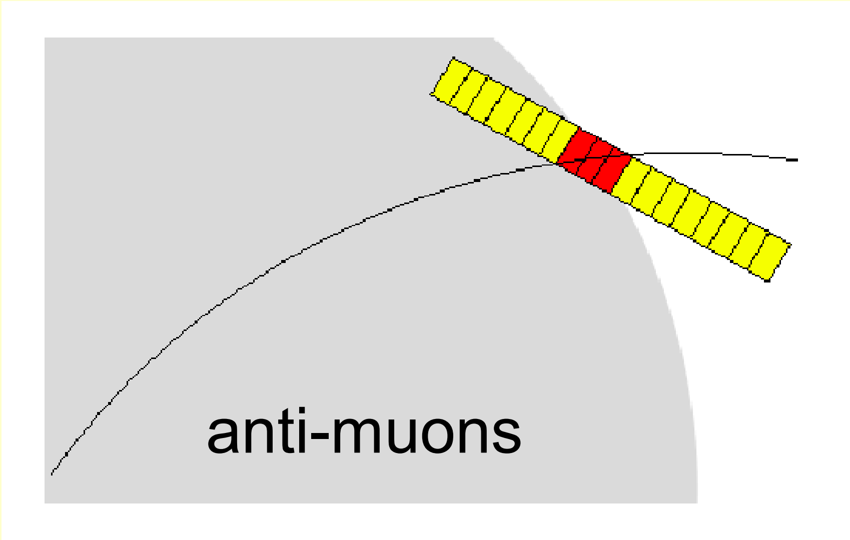
"cluster size method"

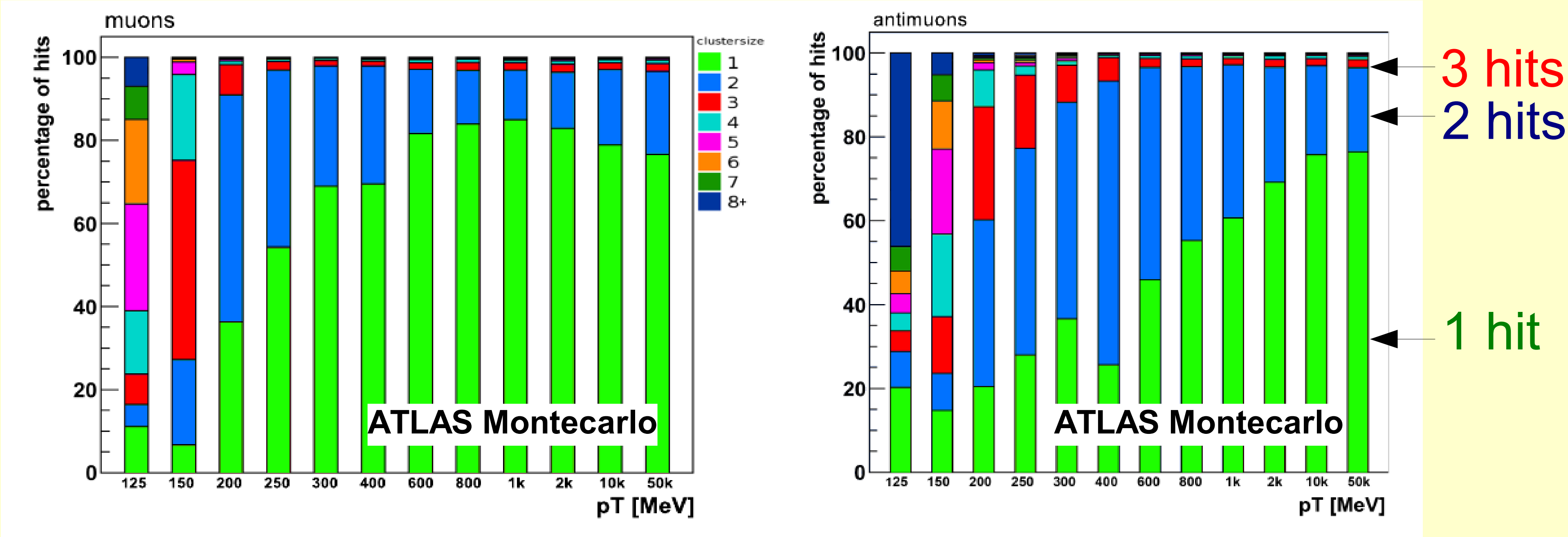


Complication: strip layers are tilted (10 degrees)

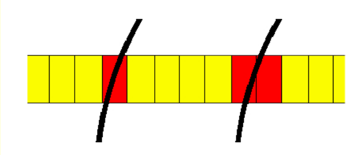
Results Cluster Method (layer #0)





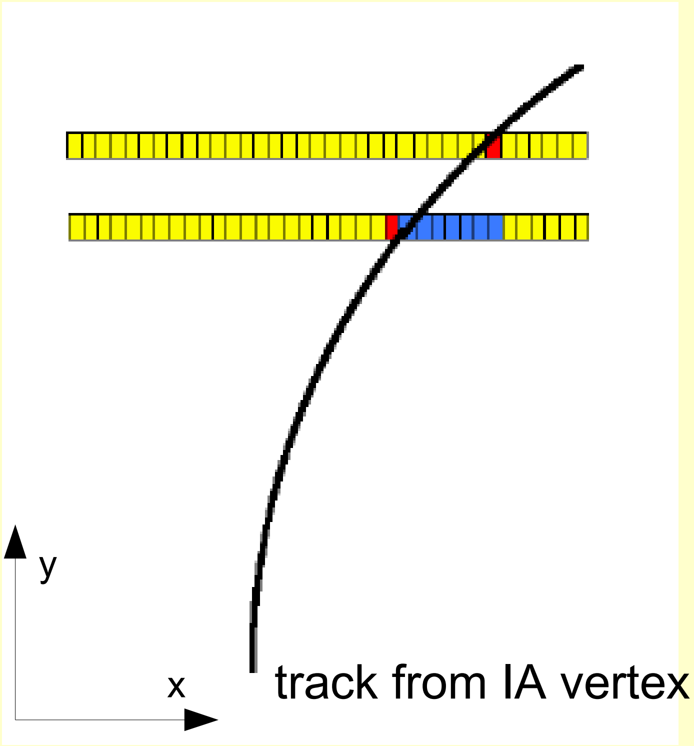


keep clusters with 1 or 2 hits



Coincidence “Offset” Method

“offset method”



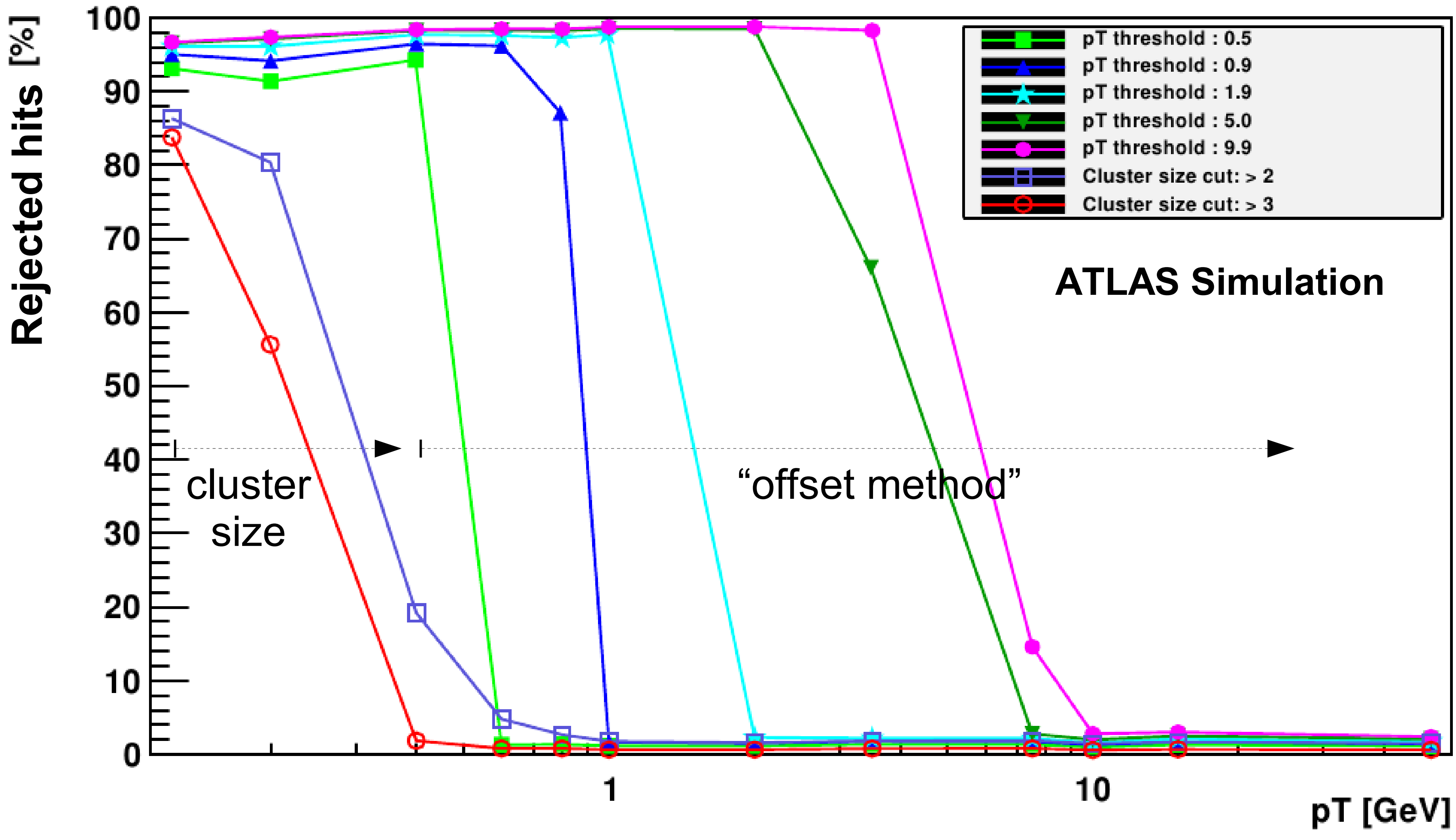
rejection of low momentum hit pairs

Two steps:

- find coincidence
- measure distance (“offset”) between hits

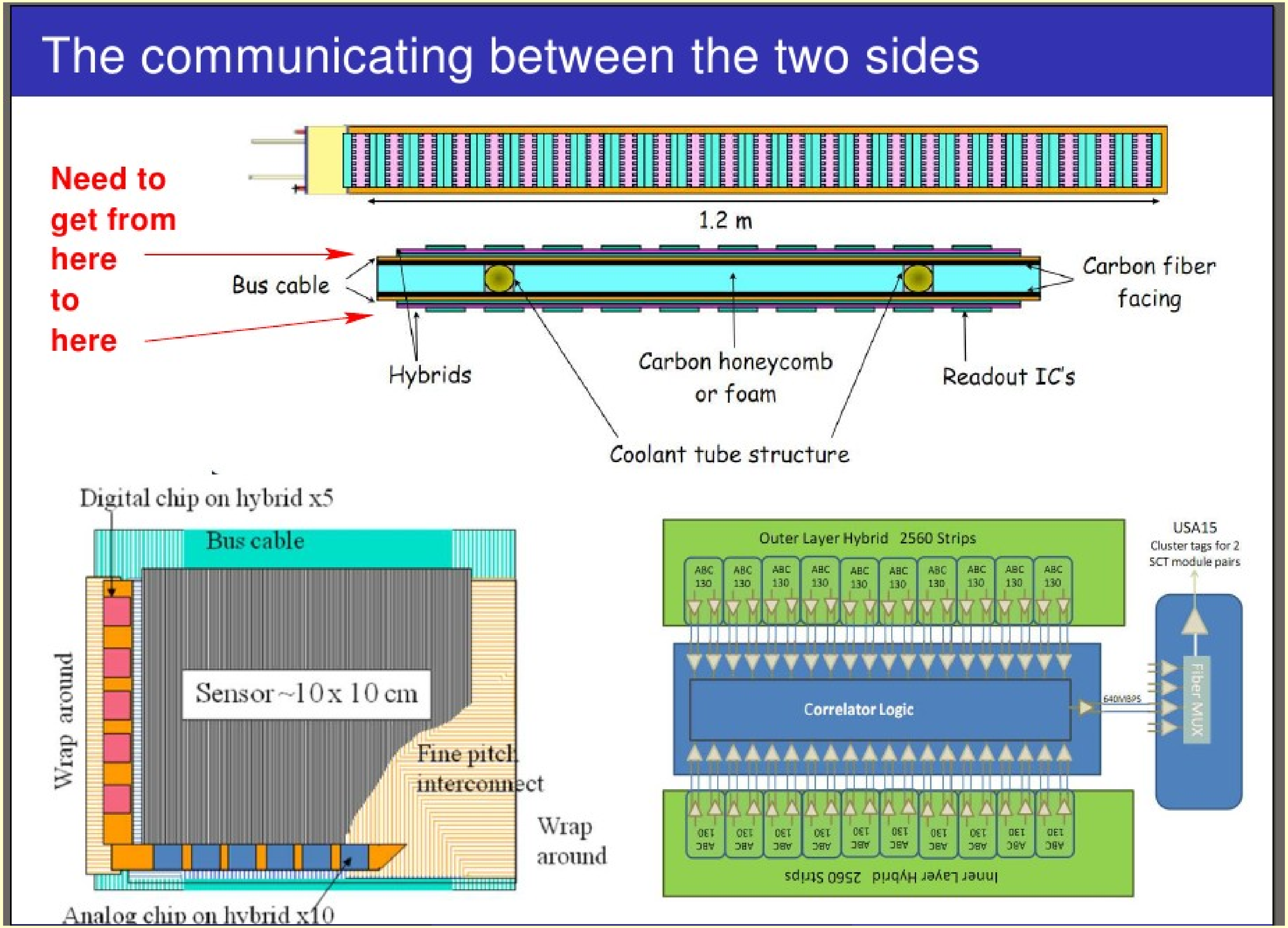
- **can be combined in a single step by defining acceptance windows**
- **special treatment of sensor edges (cross module communication + “edge recovery”)**

Muon Momentum Selectivity (layer #0)



Good momentum discrimination!

Possible Hardware Realisation



Fast Clustering Block → M.Newcomer

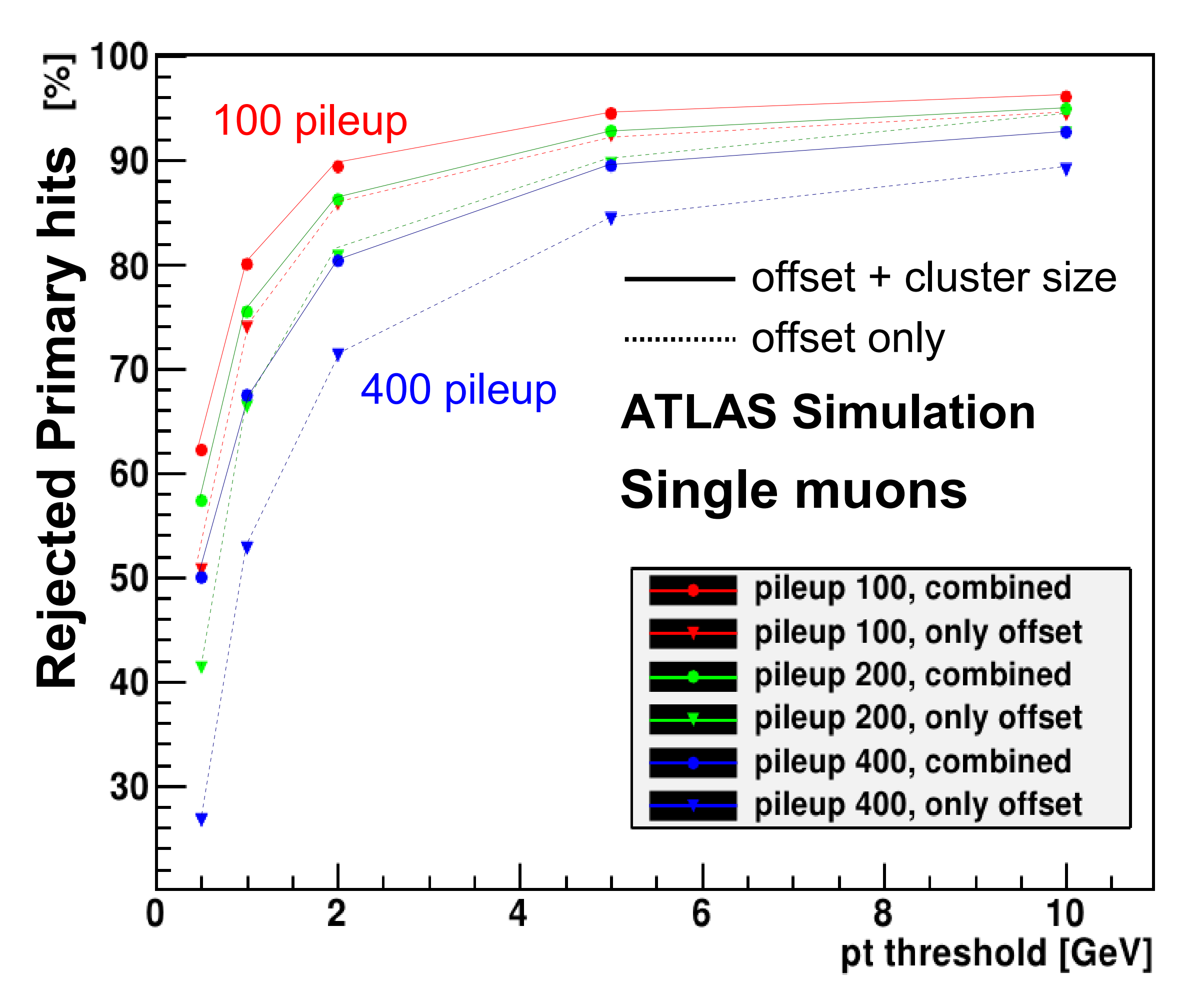
Simulation

- **GEANT4: ATLAS modified Utopia layout**
- **Strip Sensors**
  - tilt angle 10 degrees
  - no stereo angle
- **Minimum Bias Events (PYTHIA) with 50, 100, 200, 400 events**
- **Signal tracks:**
  - high p_T muons implanted in Minimum Bias events
- **Chi^2 fit simulates track trigger processor (varied Chi^2 cut)**
  - **trigger rate calculation**
- **Matching with truth information**
  - **efficiency calculation**
  - **purity calculation**

Rejection as Function of p_T Threshold

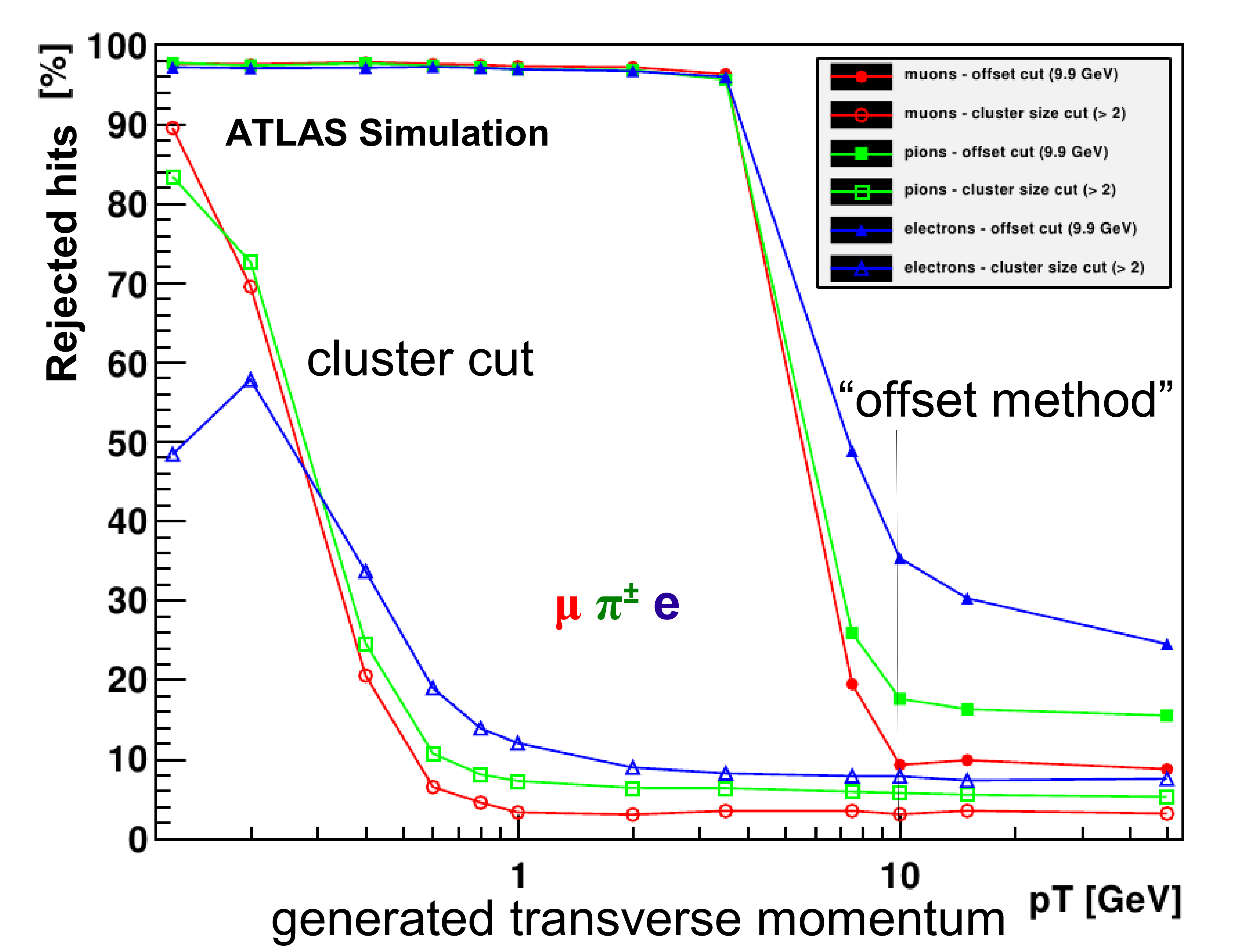
Rejection
of Primary Hits

Minimum Bias
Events



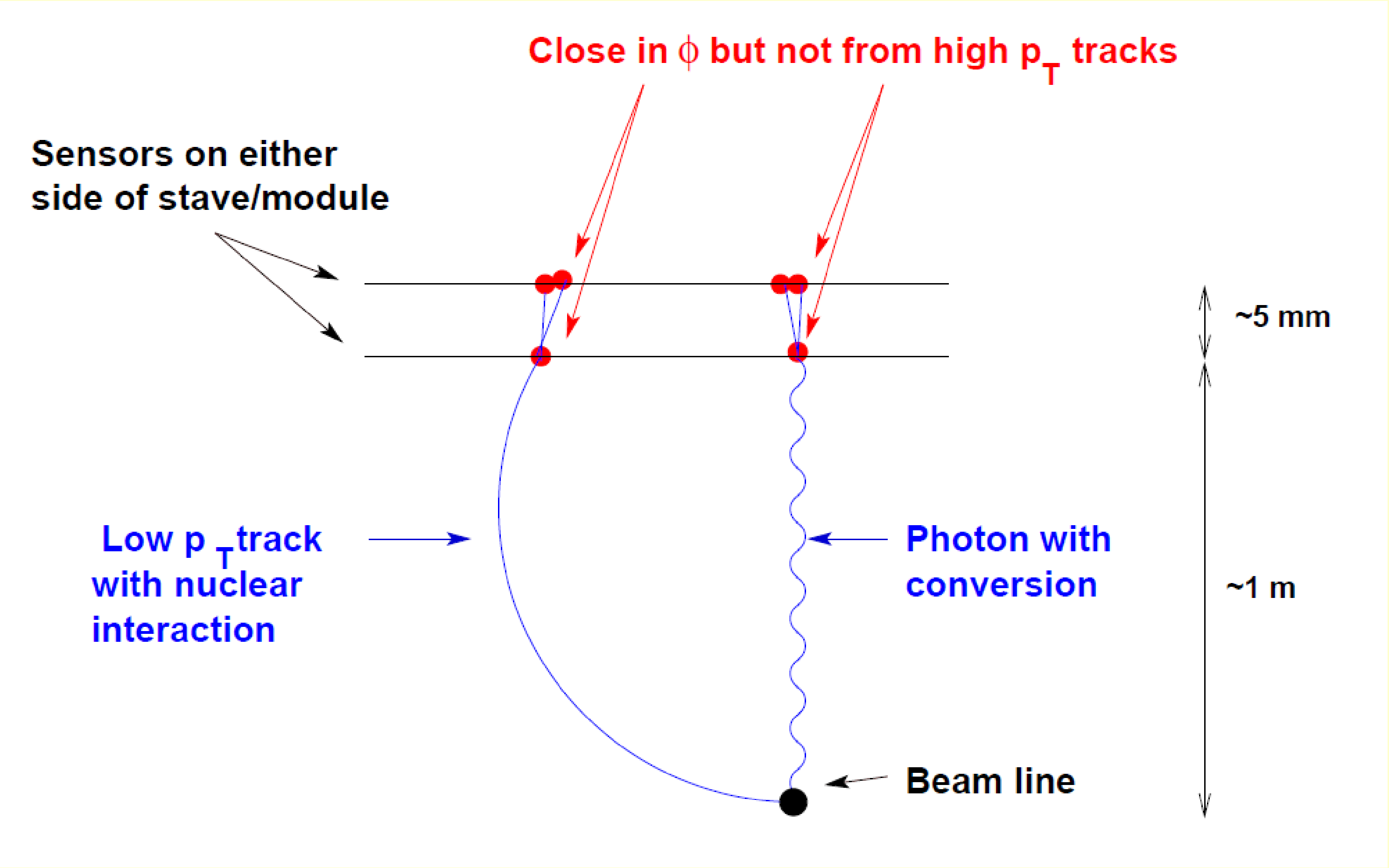
- **most tracks (at low p_T) are rejected already with a low p_T threshold**
- **rejection power higher if cluster size and offset cut are combined**
- **rejection power <u>affected by high pileup</u>**

e, μ, $\pi^{\pm}$ Rejection (single particle)



hit reduction also above p_T threshold due to secondary IA

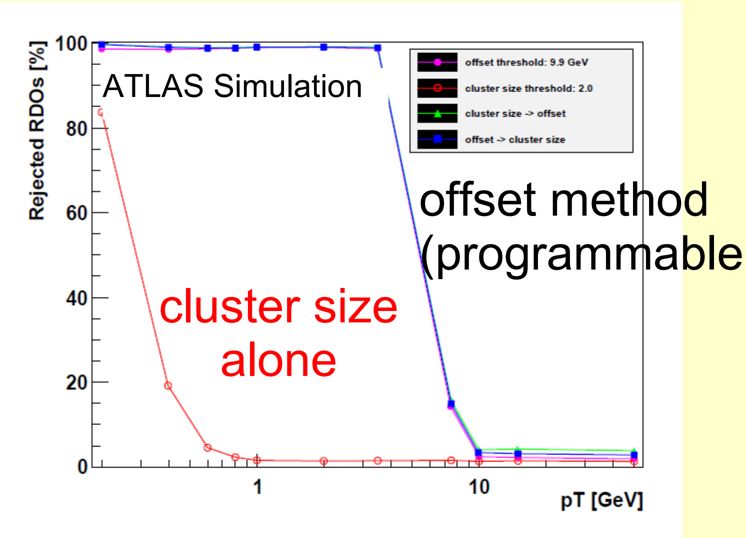
Secondary Interactions



Source of (low momentum) background

Performance of Detector Filters

- pileup 100 minimum bias (Pythia)
- p_T>10 GeV (offset)



offset cut only

	# hits (layer)	27-153 degrees # hits (SS 3 accept.)	40-140 degrees # hits (LS 2 accept.)
SS 1:	6.4%	4.3%	2.8%
SS 2:	5.5%	4.7%	2.9%
SS 3:	5.1%	5.1%	3.4%
LS 1:	8.0%	8.0%	6.2%
LS 2:	6.5%	6.5%	6.5%

Reduction factors of: 15-30 on short strip layers

~15 on long strip layers

Performance of Detector Filters

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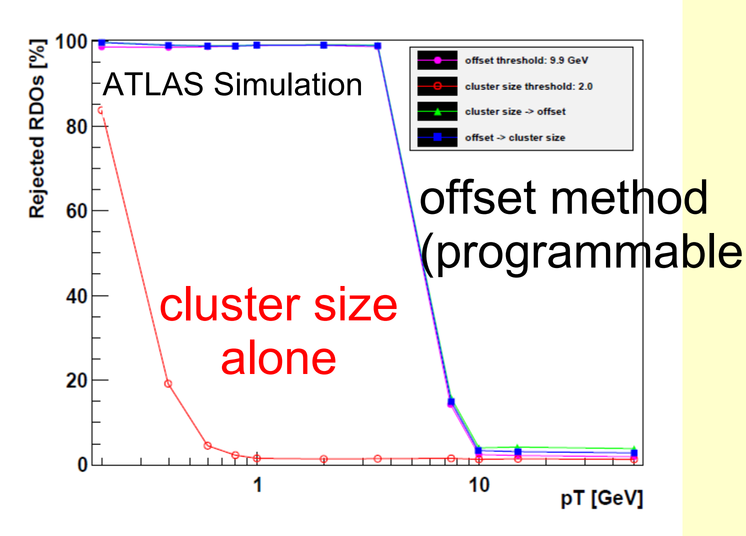
- p_T>10 GeV (offset)



cluster+offset cut

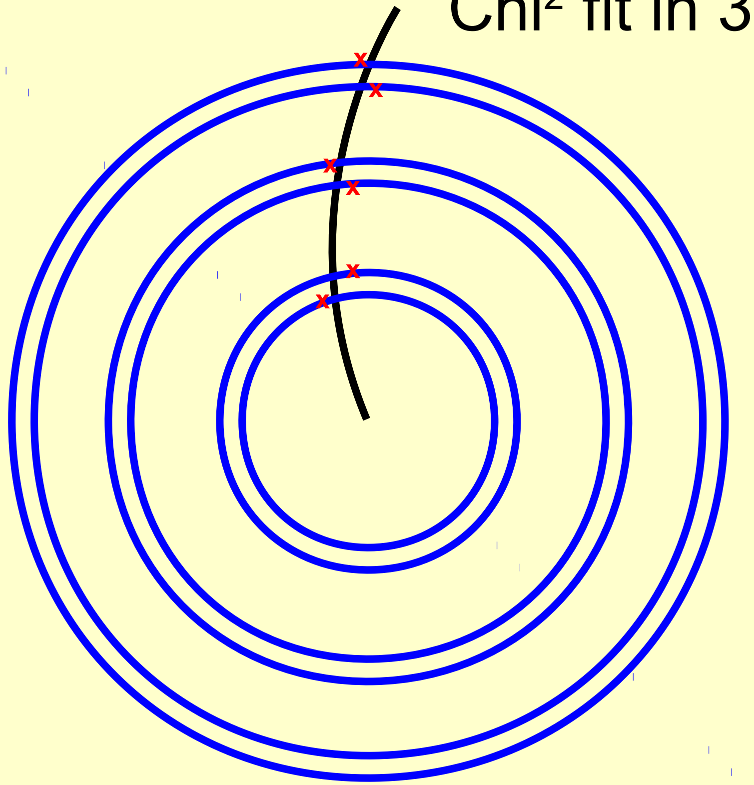
	# hits (layer)	# hits (SS 3 accept.) 27-153 degrees	# hits (LS 2 accept.) 40-140 degrees
SS 1:	4.0%	3.7%	1.7%
SS 2:	3.4%	2.9%	1.8%
SS 3:	3.2%	3.2%	2.1%
LS 1:	4.5%	4.5%	3.5%
LS 2:	4.0%	4.0%	4.0%

Reduction factors of: 25-50 on short strip layers

~25 on long strip layers

Simulation of Full Track Trigger

- **Local hit filtering (cluster size + offset method)**
- **Link hits in all used layers (no redundancy)**



Hardware Implementation:

number of patterns O(10^{10})

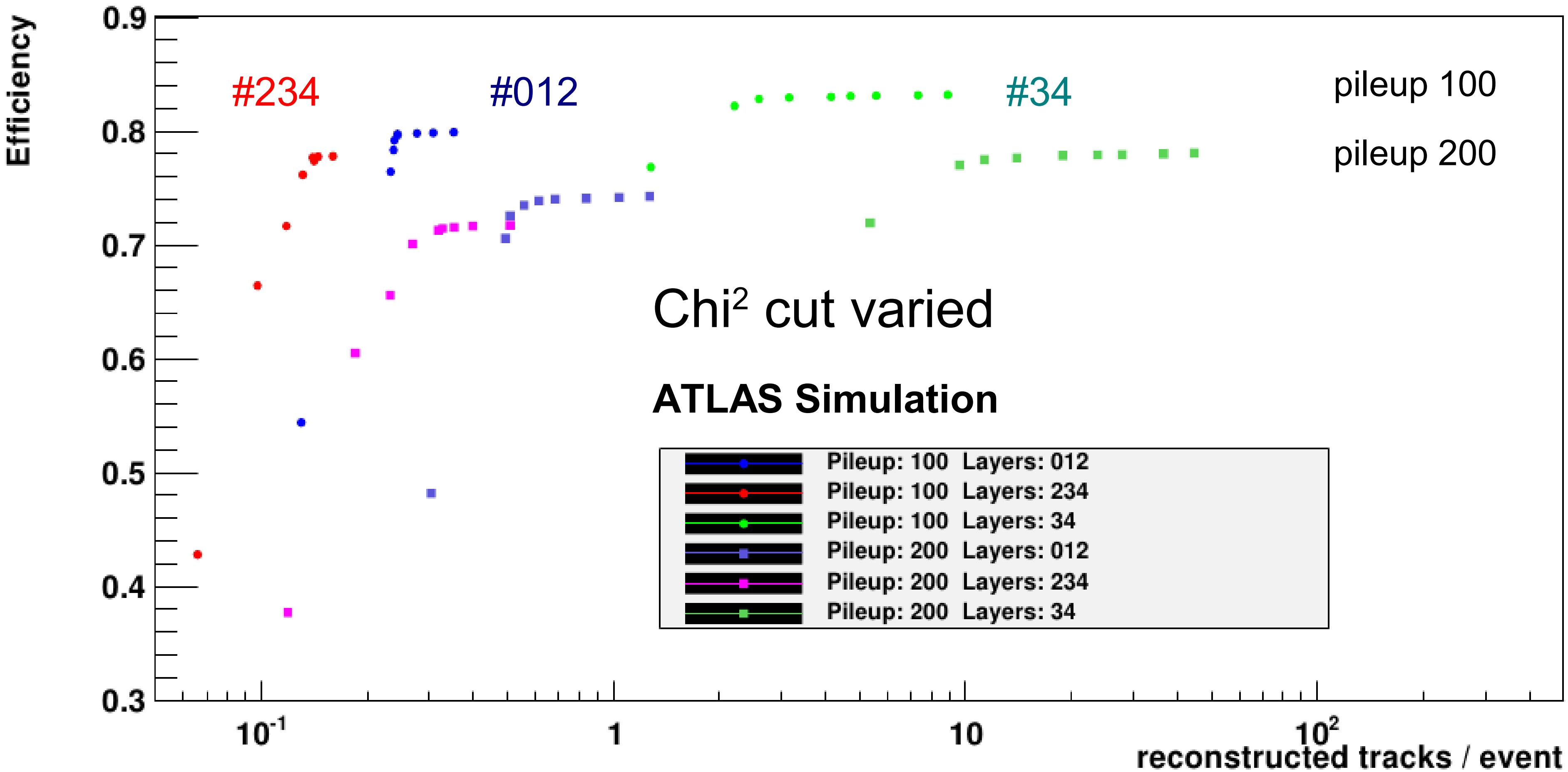
→ talk S.Schmitt (WIT2010

fast lookups using next generation of associative memory chips → more talks today

Track Efficiency vs Track Rate

cluster size
+
offset cut $p_T > 10$ GeV

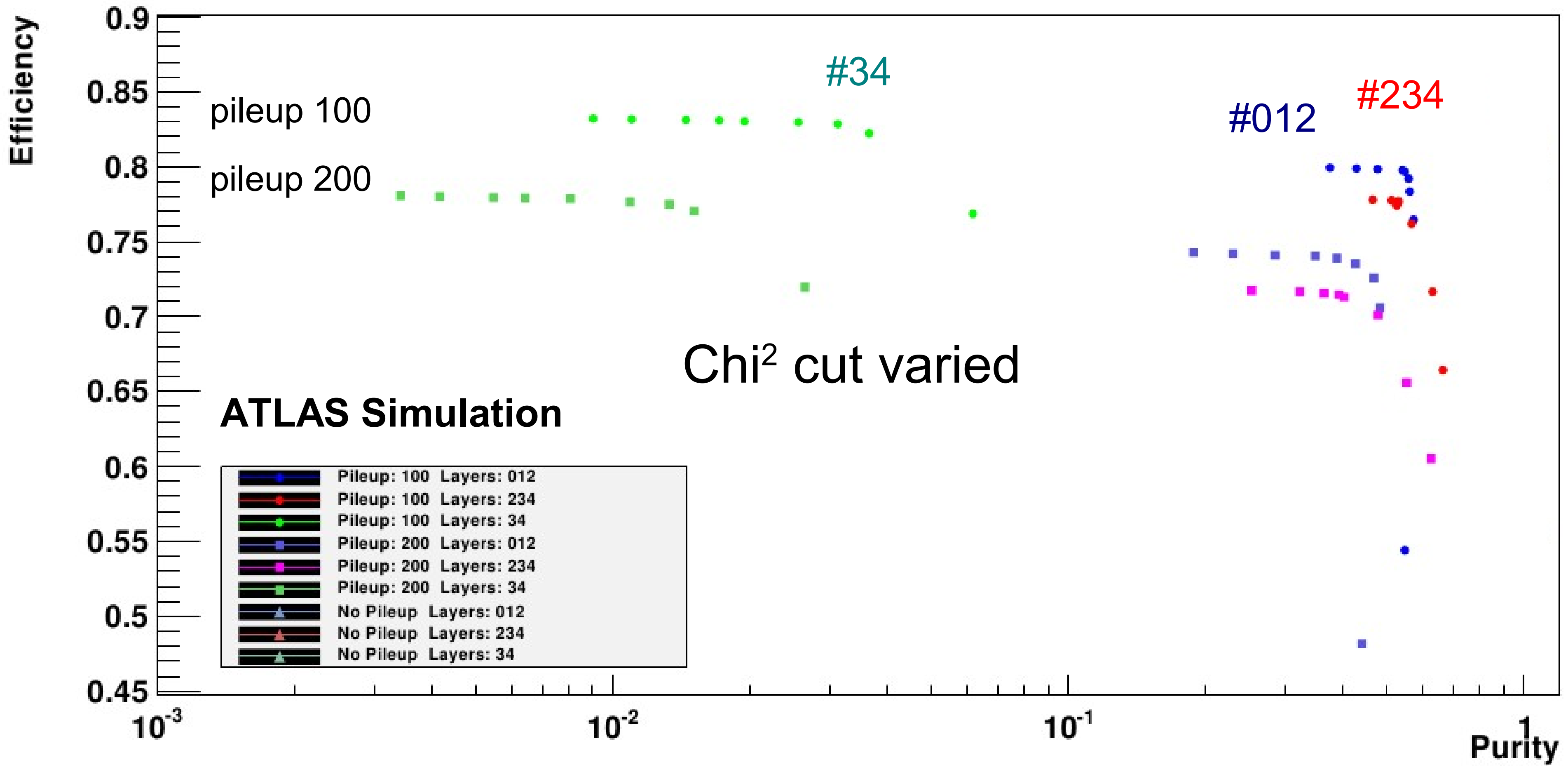
→ 3 double layers give sufficiently low rate



Track Efficiency vs Purity

cluster size
+
offset cut p_T>10 GeV

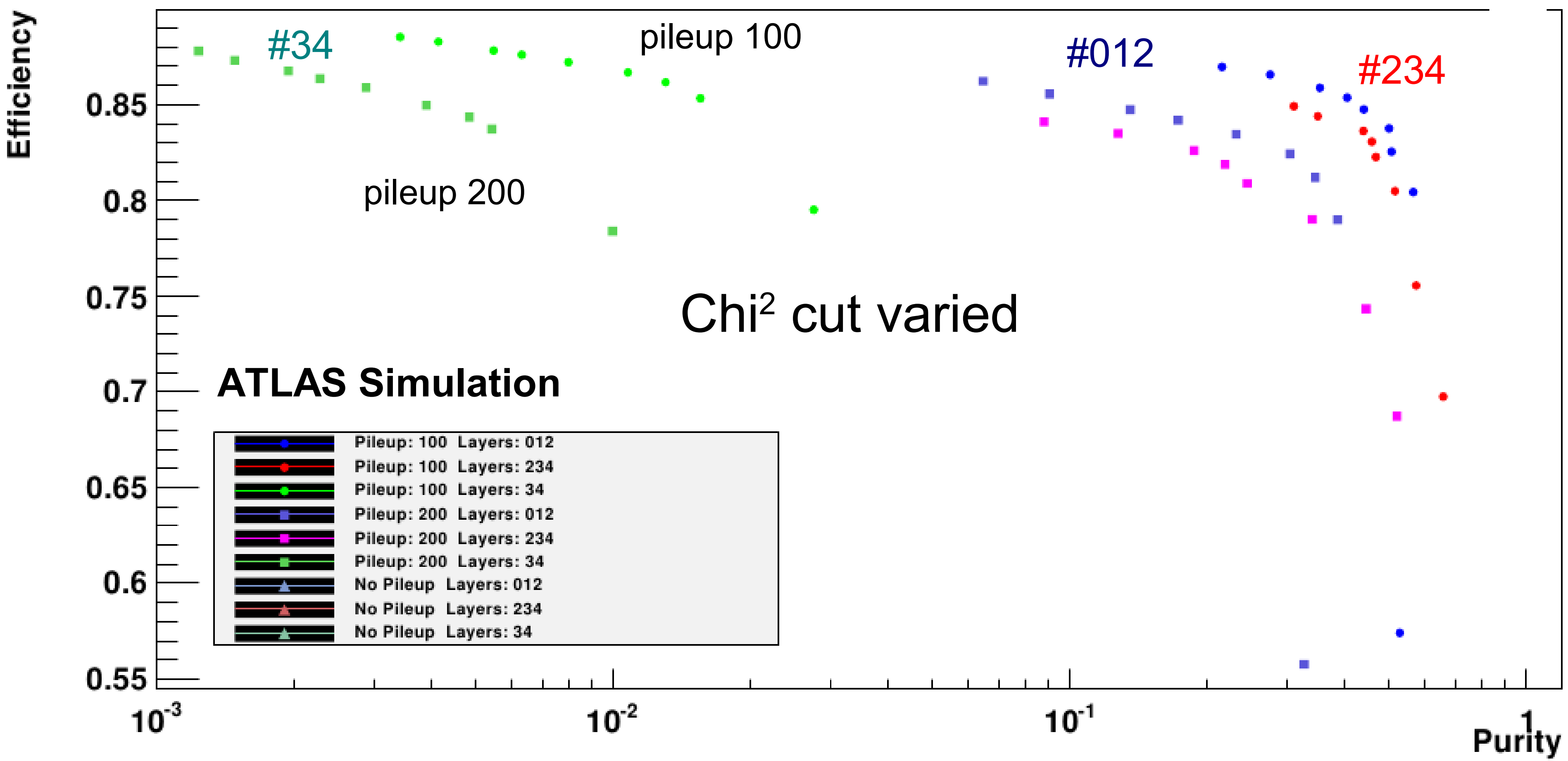
3 double layers good purity



Track Efficiency vs Purity

only offset cut

p_T>10 GeV → higher efficiency w/o cluster size cut



Parameter Studies

Choose chi^2 cut which maximises product: *efficiency^2 * purity*

cluster size cut and pileup 200

ATLAS Simulation		with cluster size cut			
p_t threshold	layer set	efficiency	purity	rate	χ^2-cut
10.0	0/1/2	0.726	0.468	0.507	12.0
	2/3/4	0.656	0.551	0.231	12.0
	3/4	0.720	0.026	5.349	6.0
15.0	0/1/2	0.743	0.309	0.097	10.0
	2/3/4	0.640	0.750	0.029	10.0
	3/4	0.746	0.006	3.312	6.0

For p_T threshold of 15 GeV rates of “only” 0.1 tracks/event

Analysis of Efficiency Losses

Set #012 (short strips)

single hit efficiency ~98% in six layers → ~12% loss
cluster size cut ~1% per layer → ~6% loss
inefficiency of offset method ~0.4% → ~1.2% loss
inefficiency track fit → >1% loss

filtering algorithms affected by high pileup by **up to 5%**

Analysis of Efficiency Losses

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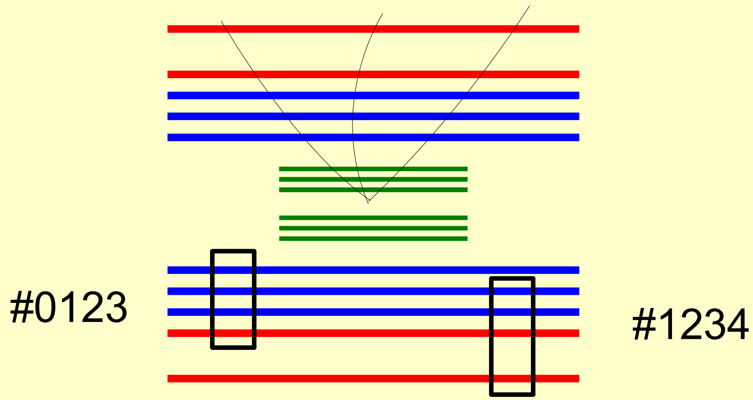
filtering algorithms affected by high pileup by **up to 5%**

Higher efficiency >95% possible be adding **more redundancy**:

- e.g. requiring 2x3 hits out of **four double layers**



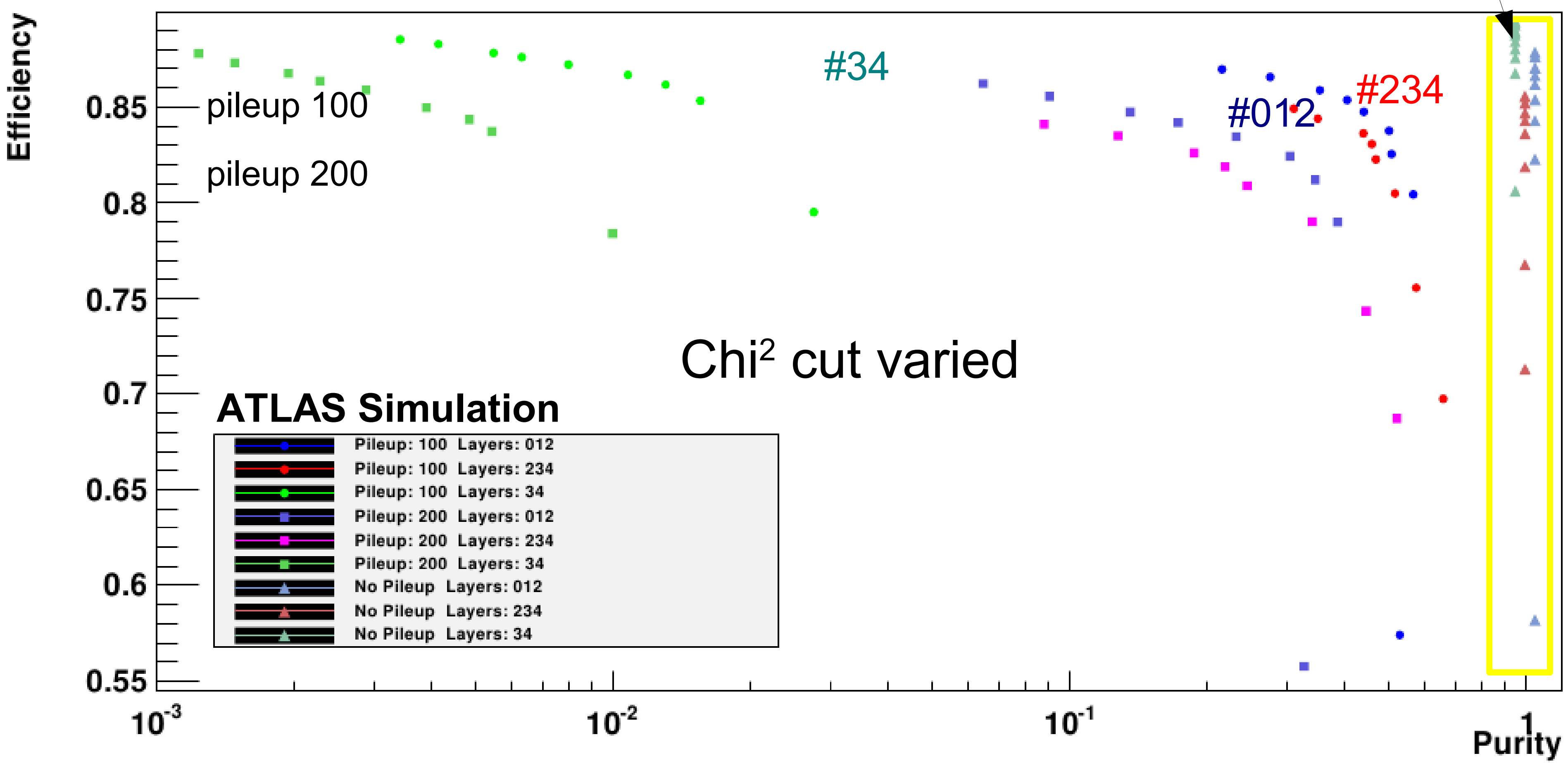
- **four layers would reduce purity**
- **more studies required**

Track Efficiency vs Purity

offset cut only

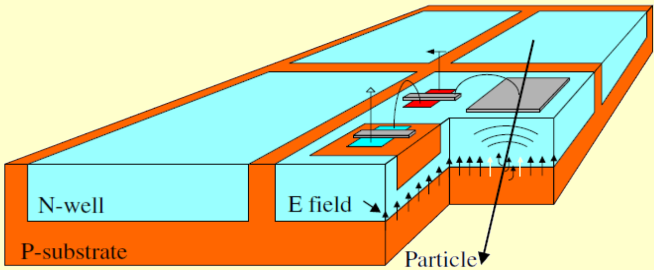
p_T>10 GeV

pileup=1 corresponding to pixel/"strixel"



Alternative: CMOS Pixel Sensors

- Main track trigger challenge is the data rate
- Reduce data rate by going from **strips** to thin (50 μm) **pixels** (50 x 50 μm^2)
  - number of hits per layer does not increase
  - **more information** for similar amount of material
  - lower occupancy → **fewer layers** (in total) required



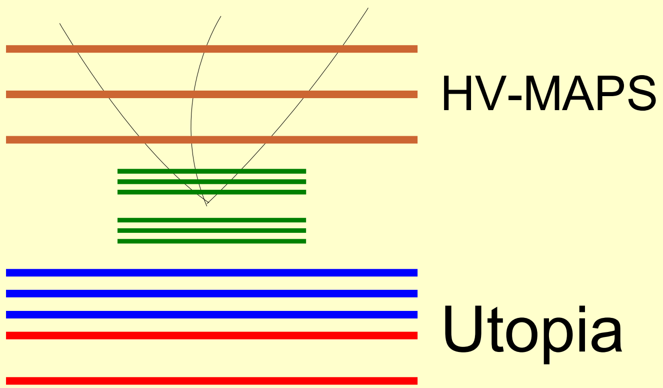
→ HV-MAPS technology by Ivan Peric
→ Mu3e experiment (poster), D.Wiedner

furthermore:

- **3D correlator** (in CMOS sensor?) instead of 2D → filtering is more powerful
- **z-vertexing** ($\sigma = 5$ mrad) possible for hit doublets (for 5 mm gap)
  - further reduction of data rate

What is good for the trigger can be beneficial also for the offline reconstruction

- **HV-MAPS should be studied seriously**



Summary

- **Studied design of a Self-Seeded First Level Track Trigger for ATLAS Utopia design**
- **Local filtering algorithms: cluster size and coincidence**
- **Results:**
  - **at least 3 double layers for reasonable purity and trigger rate**
  - **design with more redundancy (4 double layers) would improve track efficiency**
  - **Self Seeded Track Trigger possible with "minor" design changes of the Utopia design (no stereo angle, frontend electronics)**
- **Alternative designs using pixels (HV-MAPS) ?**

Extra Slide

Two comments motivated by discussions during this workshop

1. **Proposed L0/L1 readout scheme and First Level Track Trigger ("Self Seeded") are not exclusive**
2. **Self Seeded Track Trigger can add redundancy to First Level Trigger**

e.g. alternative L1 Muon trigger: