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Status of Work on Vertically Integrated Circuits

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Commencing work on the 3D-integrated circuits in the High Energy Physics (HEP) community, which coincided with the appearance at the same time of first commercial 3D-IC design kits, whetted the appetite of the community and raised confidence in the rapid rollout of 3D-IC technology, which undoubtedly introduces a new quality to integrated readout system for the detectors. The Fermilab team was in this group of a few, who spearheaded the development of 3D integrated circuits for detector's readout. At the first place a proprietary fully-depleted CMOS SOI process by MIT-LL and the via-last based wafer bonding technology was used. Commercial bulk CMOS wafers with front-end-of-line integrated micrometers-size through silicon vias (TSVs) and the Tezzaron wafer bonding technology was used at the later time. The early Fermilab work led to the formation of an international consortium, grouping major research centers, for the development of vertically integrated circuits. The consortium submitted the first multi project wafer (MPW) run to Tezzaron with over 25 different designs in 2009. The run unfortunately has been suffering from multiple problems causing an overall delay to such an extent that no diced 3D parts could be delivered to the participants until the drafting of this abstract. Despite of this downbeat of the apparent picture of the state of the first HEP MPW run, it is received as the source of learning experiences, about 3D-IC processing technology and its crucial ingredients, like requirements for the surface flatness and surface treatment, alignment, gas atmosphere, etc. Due to the use up of initial stocks of wafers for failed attempts of bonding, it was necessary to start an additional lot of wafers at the foundry. By having the conditions of the bonding process fine-tuned, it is expected that the wafers will eventually be bonded successfully, resulting in distribution of chips for testing. The review of consecutive steps undertaken with Tezzaron, illustrated by their results, will be provided at the presentation. In the autumn of last year, a group of professional brokers (MOSIS/CMP/CMC) decided to open an access to the Tezzaron/GlobalFoundries 3D-IC process through the MOSIS MPW scheme. The decision drew deeply from the knowledge acquired in the completion of the 3D-IC MPW run by Fermilab and nonetheless existing positive experience of full processing of another MPW run (parallel to the HEP one) by Tezzaron. New high density circuit bonding techniques, wafer thinning, and submicrometer size TSVs allowing connection to top and bottom sides of an IC provide new opportunities for the detector designer. These opportunities will be presented by looking at various 3D designs that have been completed for the MPW run or are being planned for exploration.

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