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Radiation tolerant IP-cores for the control and readout of Front-End electronics in future Silicon detectors

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The FF-LYNX protocol represents an innovative and flexible solution for the distribution of Timing, Trigger and Control (TTC) signals and the data readout in future detectors for the High Energy Physics. Transmitter (TX) and Receiver (RX) interfaces to serial electrical links implementing the FF-LYNX protocol with different speed options (160Mbps, 320Mbps, 640Mbps) have been developed. They are available as VHDL cores for integration in commercial FPGA devices and as Standard-Cell based cores, designed and developed in the IBM CMOS 130nm technology. Architecture and behavior of the interfaces and results of test and characterization of the prototypes embedded in the test ASICs fabricated in 2011 will be presented.

Radiation tolerant FIFOs have been developed as input and output buffers in TX and RX interfaces. They are available as stand-alone IP-cores and can be used in Front-End ASICs or other circuits where radiation tolerant data buffers are required. Architecture and behavior of these FIFO blocks will be described as well as results of irradiation tests performed on the their prototypes.

Results of tests performed with FF-LYNX Encoder and Decoder directly coupled with the GBT Transmitter and Receiver in an FPGA proof-of-concept demonstrator of optical links handled by GBT transceivers and running data encoded with the FF-LYNX protocol will be presented as well as the architecture and the behavior of the Data Concentrator Module, a VHDL core that merges input data transmitted from multiple sources through “low-speed”serial links into one (or more) “high-speed”output serial links.

Finally future plans, mainly focused on the development of interfaces with improved speed and power performances and including custom Serializer and Deserializer modules will be presented.

Summary

The FF-LYNX protocol developed by INFN-Pisa, University of Pisa, Department of Information Technology, and UCSB, Physics Department, represents an innovative and flexible solution for the distribution of Timing, Trigger and Control (TTC) signals and the data readout in future detectors for the High Energy Physics. It provides different speed options (“4x”, “8x”, “16x”) and robustness of critical information (triggers, frame headers and frame descriptors) against errors due to noise and radiation, It allows to share the same physical channel between time critical and fixed latency information, as triggers or “trigger’data, and information with lower priority and unbounded latency, as “raw”data or “slow”controls.

The protocol has been extensively validated through functional simulations and tests in FPGA based emulators. Transmitter (TX) and Receiver (RX) interfaces to “double-wire”(clock and data on separate lines) serial electrical links have been developed in the three speed options as VHDL cores, available for integration in commercial FPGA devices, and as Standard-Cell based cores, designed in the IBM CMOS 130nm technology. A test circuit with prototypes of the interfaces has been fabricated in 2011.

A full set of TX and RX interfaces implementing a new version of the FF-LYNX protocol with a DC-balanced “8b/10b like”channel encoding that provides compatibility with optical links and standard Clock Recovery Devices (CRD) and, therefore, with “single-wire”links (clock and data encoded onto one line) has been also developed. Prototypes of the interfaces in the “8x”speed option have been designed as Standard-Cell based cores and integrated in a second test circuit.

The behavior and the performance of the TX and RX interfaces in both versions will be shortly described and the results of the test and the characterization (also under irradiation) of their prototypes embedded in the test ASICs will be presented.

FIFOs implementing error detection and correction and scrubbing have been developed as input and output buffers in TX and RX interfaces. These modules can be used as stand-alone IP-cores in Front-End ASICs or other circuits where radiation tolerant data buffers are required. The architecture and the behavior of these FIFO blocks will be shortly described as well as results of irradiation tests performed on the FIFO prototypes.

FF-LYNX Encoder and Decoder have been directly coupled with the GBT Transmitter and Receiver in an FPGA (Xilinx Virtex 6) and a proof-of-concept demonstrator of optical links handled by GBT transceivers and running data encoded with the FF-LYNX protocol has been developed and validated. Results of the tests performed in the demonstrator will be presented.

We have also very recently developed and validated the Data Concentrator Module (DCM), a digital module that merges input data transmitted from multiple sources through "low-speed"serial links into one (or more) "high-speed"output serial links. This IP-core could play a key role in concentrating and buffering data from different Front-End ASIC in future detector modules before transmission to optical transceivers. Both DCM architecture and behavior will be described.

Future plans will be finally shortly described. They mainly foresee the development as IP-cores of TX and RX interfaces compatible with "single-wire"serial links with improved speed (up to 800 Mbps) and power performance and tolerance to Single Event Transient effects. This will require the development of custom Serializer and Deserializer devices and of a radiation tolerant CRD. The submission of a test circuit including prototypes of these devices is foreseen before the end of 2012.

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