Use of Associative Memories for L1 triggering in LHC environment.

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WIT2012 Workshop on Intelligent Tracker

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Outline

- Importance of **tracking** for **Level-1** trigger
- Track reconstruction -> **pattern matching** -> **Associative Memory** (AM)
- **Existing** HW and FW for L2 and L1 trigger
- **New** version of AM system under design
- Conclusion

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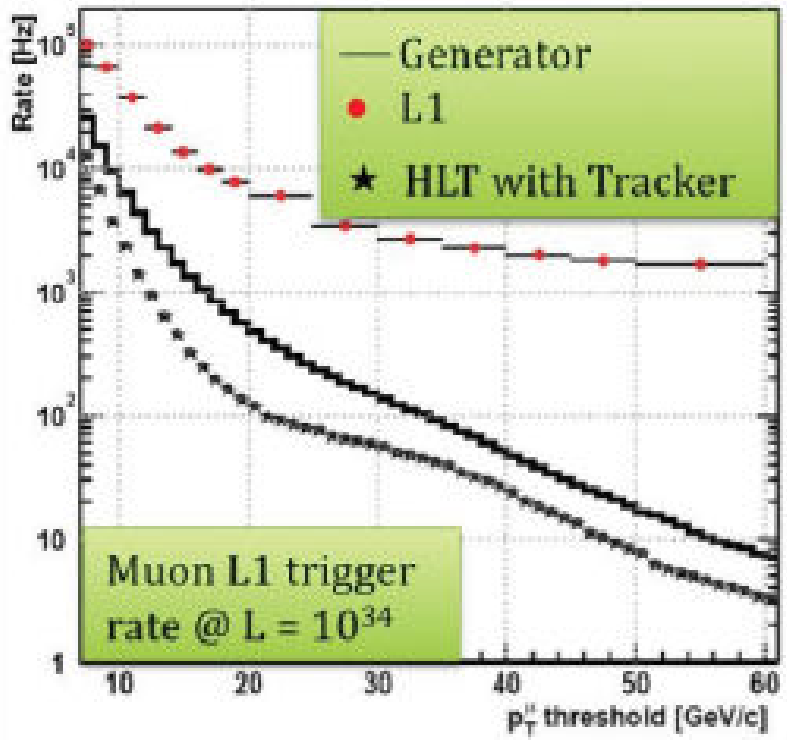
Importance of **tracking** for **Level-1** trigger

The increase of the LHC luminosity well above its original design figure requires a substantial upgrade of the CMS tracking system

• The biggest challenge stems however from the requirement to maintain the first level trigger rate at its current value of 100 kHz.

• This requires the use of tracker data in the Level-1 (L1) trigger, and consequently a completely new tracker concept.

• Tracker data could be used to improve the muon pT resolution, to facilitate electron matching, for the application of isolation criteria, and for primary vertex identification



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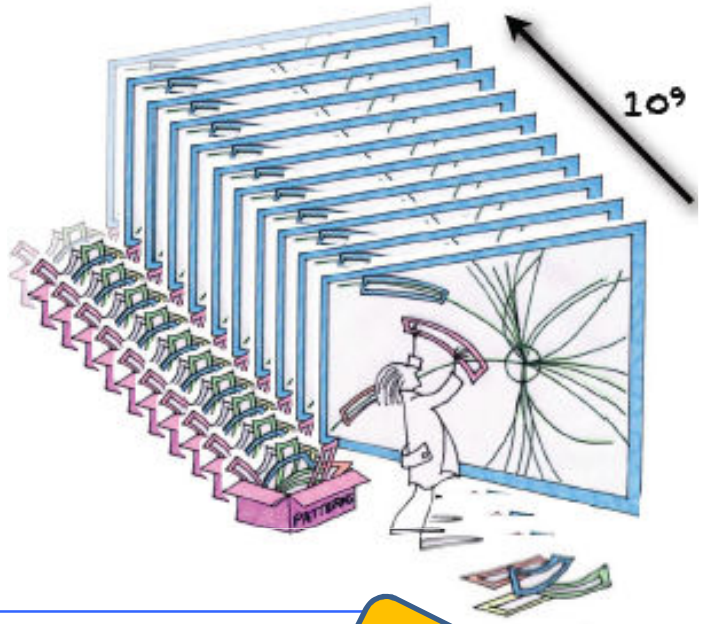
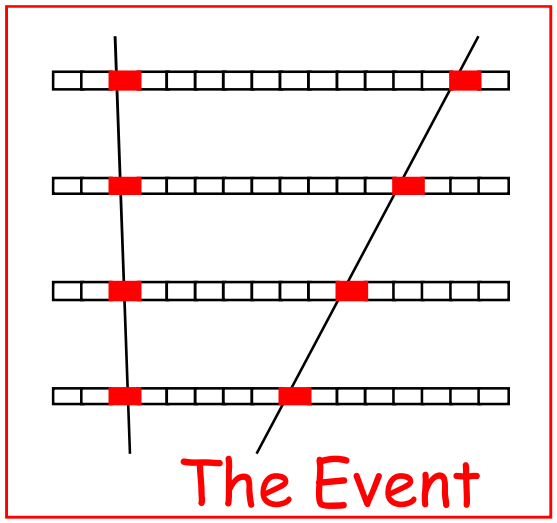
Track reconstruction and pattern matching

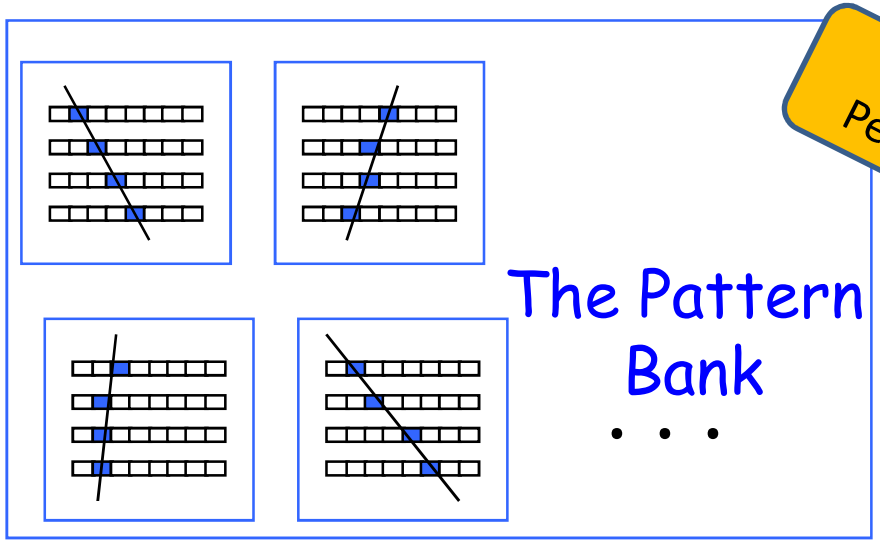
Pattern matching: is one of the possible algorithms.

The pattern matching compares the event with ALL the candidates tracks stored in a local memory (Pattern Bank).

The pattern matching can be very fast for online track reconstruction thanks to the Associative Memory (AM) parallelism [see CDF use-case]

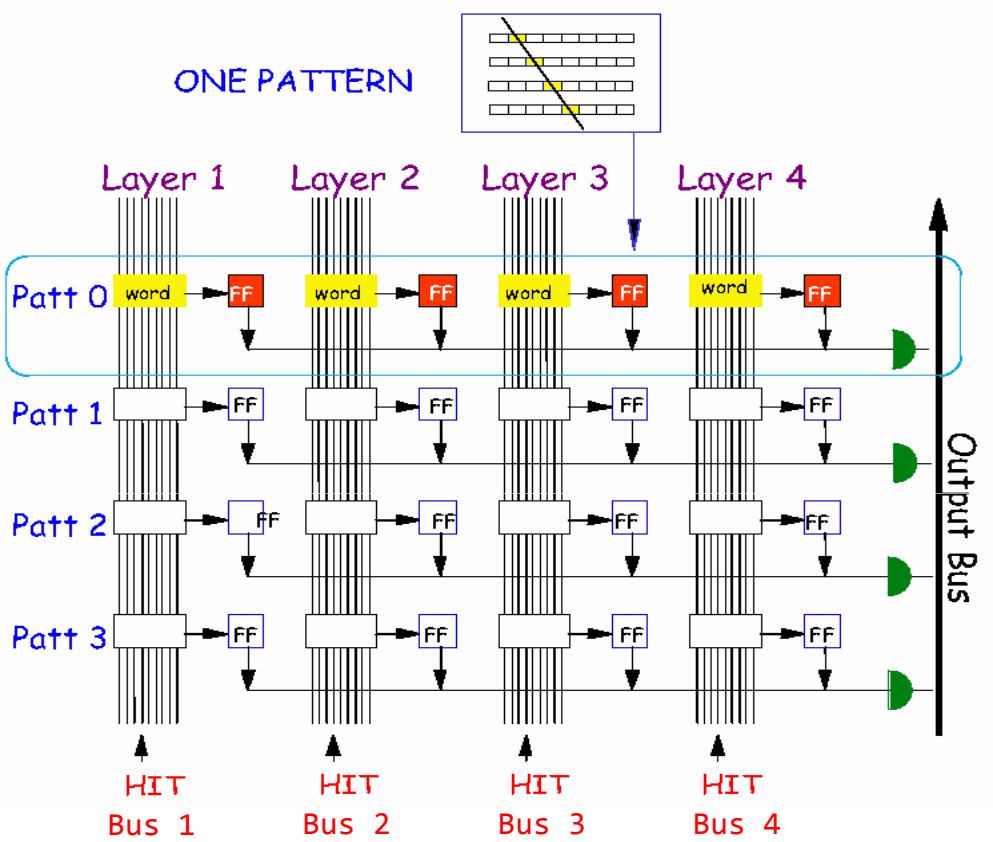






See Björn Penning Talk

Associative Memory for track reconstruction



HIT = detector channel fired by a particle

ROAD = fired patterns

- Dedicated device:

  Maximum parallelism !
- Each pattern with

  private comparator
- Tracks found during

  detector readout !

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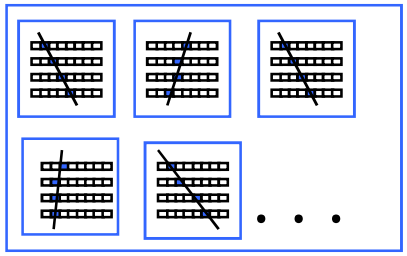
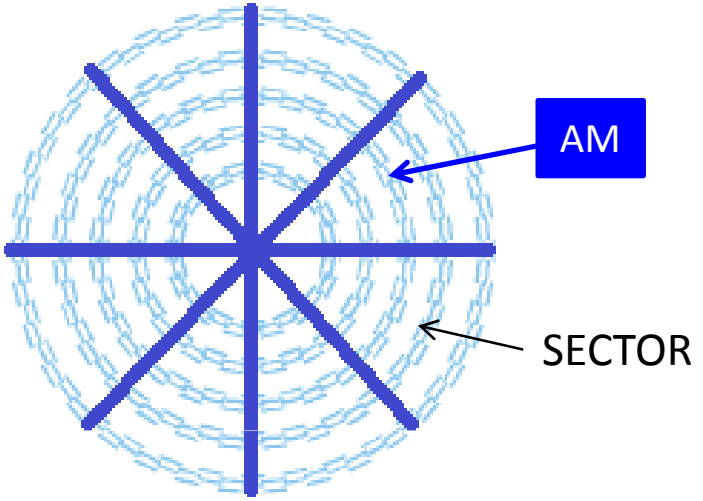
L1 and L2 trigger with AM

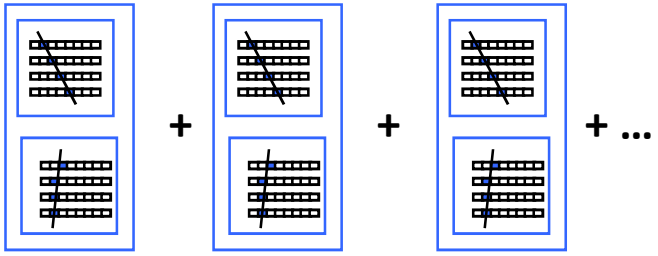
The associative memory can be used both in level1 and level2 trigger

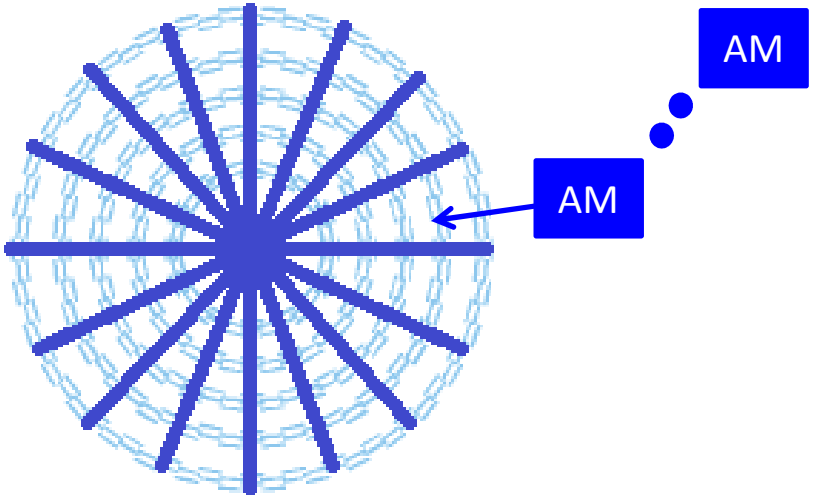
L2: Lower input rate (100kHz), ordered events, longer latency (~25usec for FTK)
=> one big pattern bank to process 1 event at a time





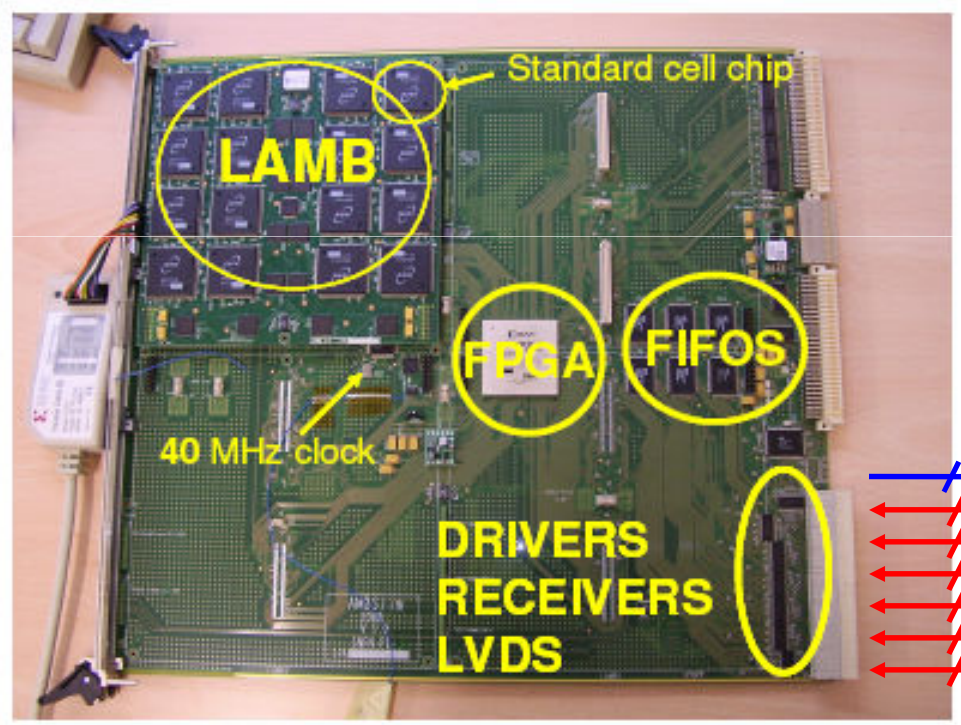
L1: High input rate (40MHz), mixed events, low latency (~6usec)
=> multiple (but smaller) pattern banks for multiple events parallel processing





Existing hardware: AMBSlim and CDF LAMB

A single motherboard for **level1** and **level2** trigger applications (AMBSLIM, SLIM5 experiment) thanks to flexibility of the powerful **control FPGA**.



FPGA: **XILINX** VIRTEX2pro 1696 pin

6 input buses (21bit each)

1 output bus (30bit)

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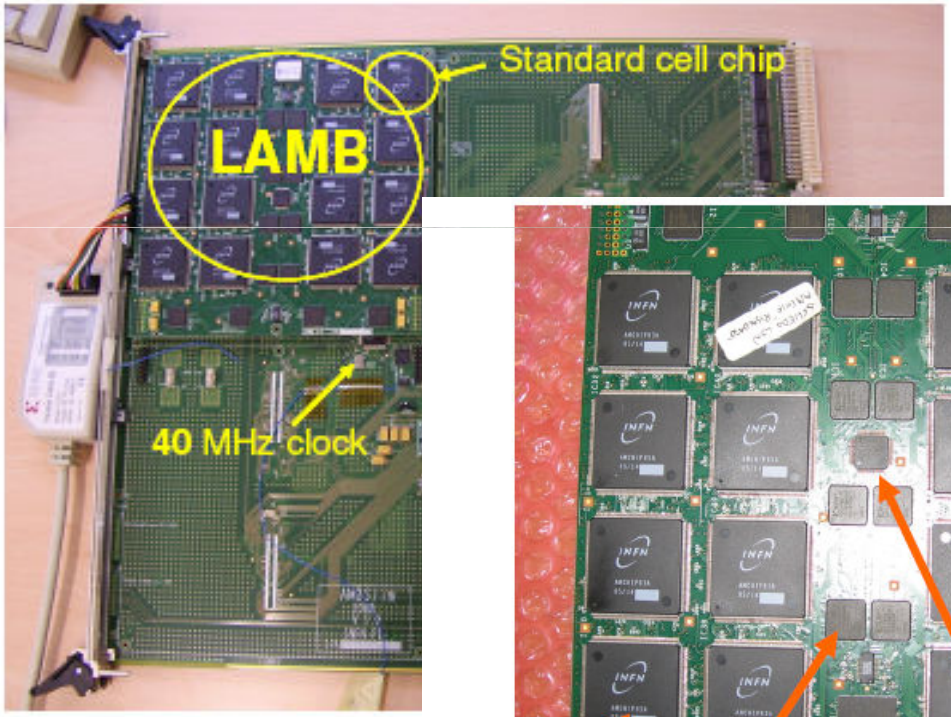
A single motherboard for **level1** and **level2** trigger applications (AMBSLIM, SLIM5 experiment) thanks to flexibility of the powerful **control FPGA**.



FPGA: **XILINX** VIRTEX2pro 1696 pin

6 input buses (21bit each)

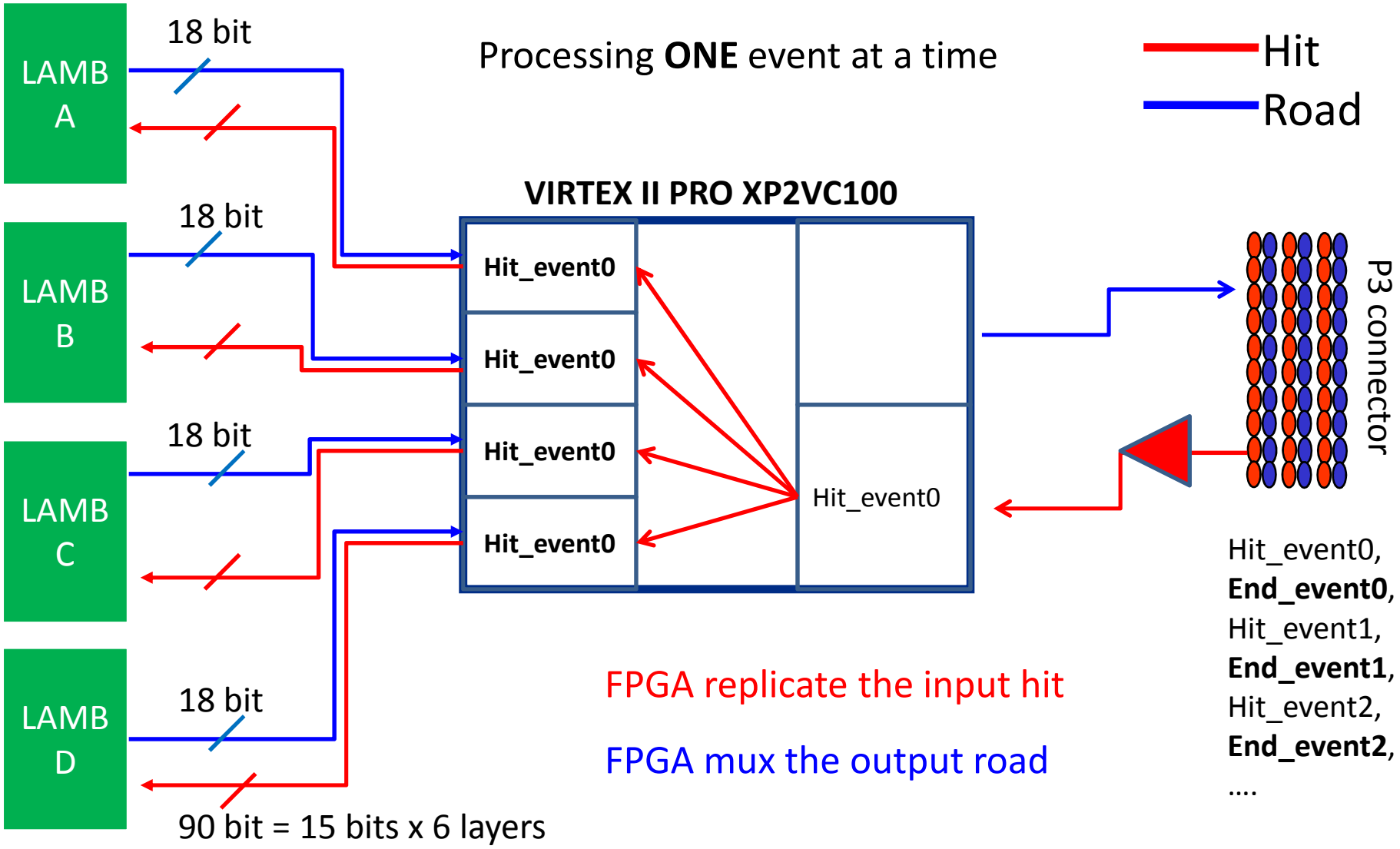
s (30bit)

1 AMchip: 5Kpattern

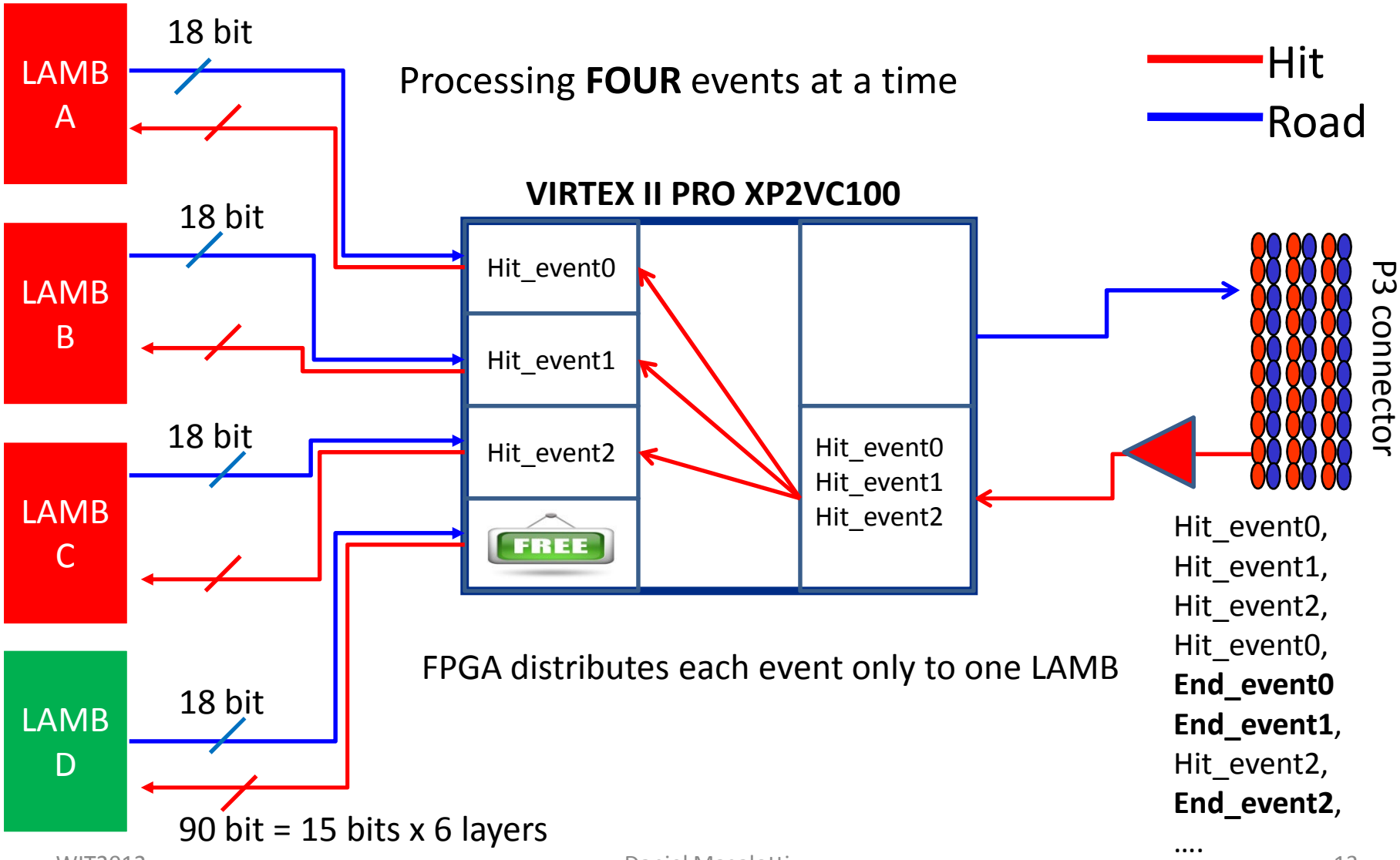
INDI: Input Distributor (fan-out)

GLUE: mux roads from AMs

AMBoard Logic Control (Level 2)



AMBoard Logic Control (Level 1)



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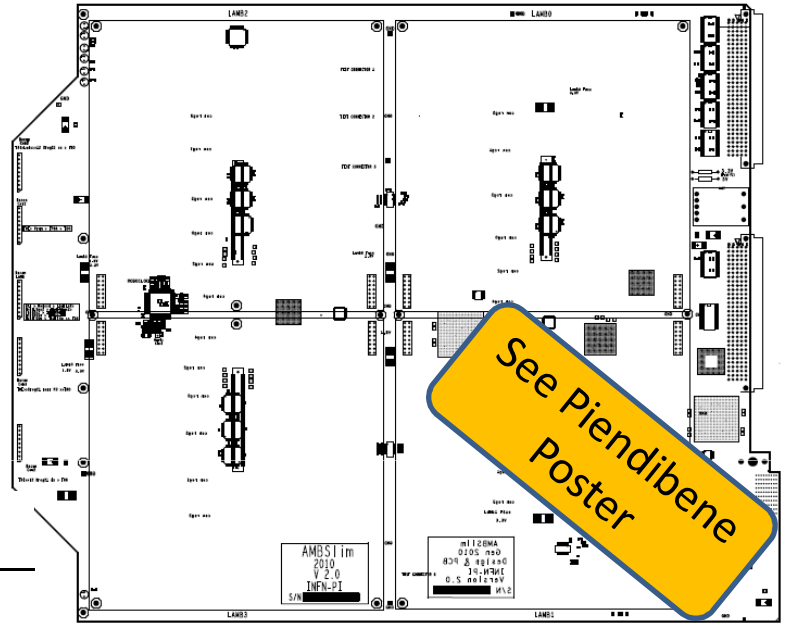
Hardware upgrade

NEW AMCHIP

See Annovi Talk

OLD	NEW	
40	**100**	MHz
6	**8**	#input parallel buses
4.3	**12**	Input BW Gbit/s
1	**1**	# output bus

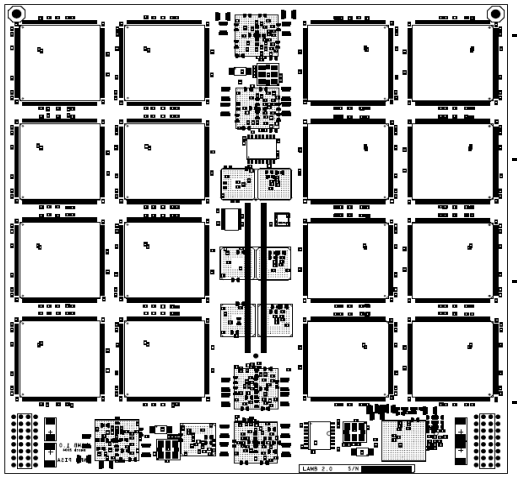
NEW AMBOARD



See Piendibene Poster

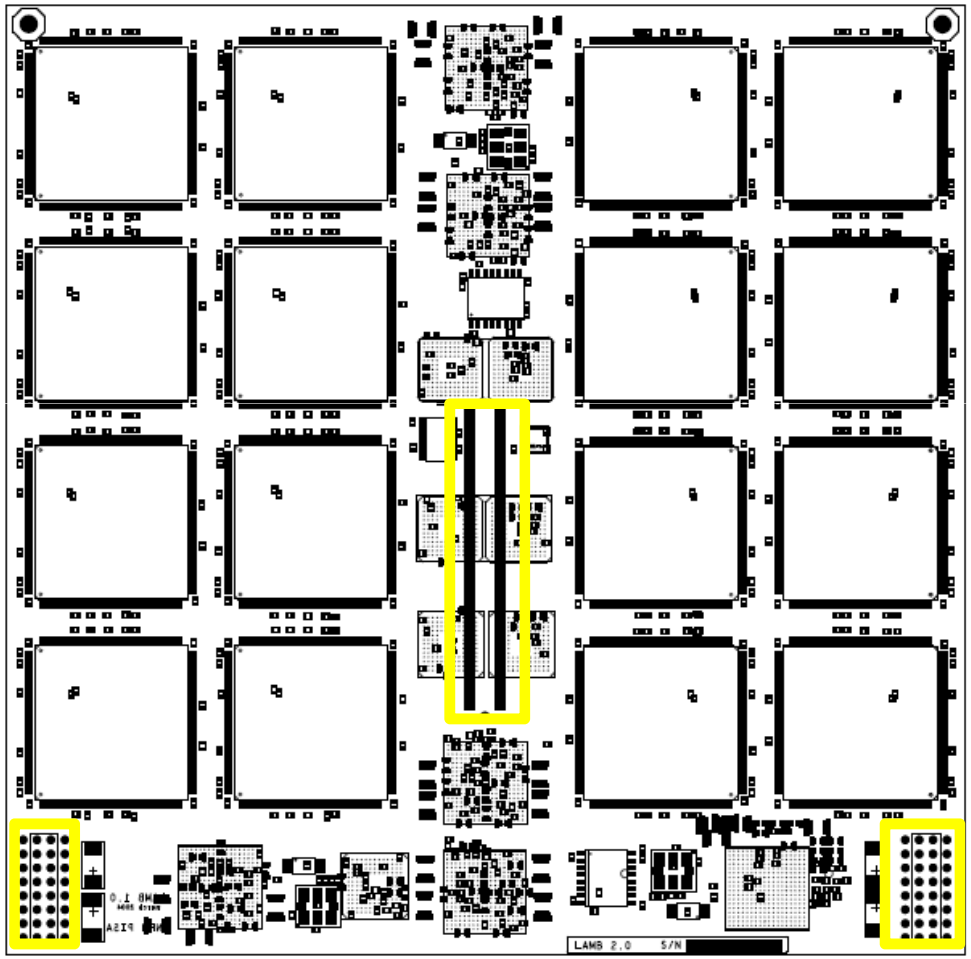
OLD	NEW	
6	**12**	#input bus
1	**16**	# output bus

NEW LAMB



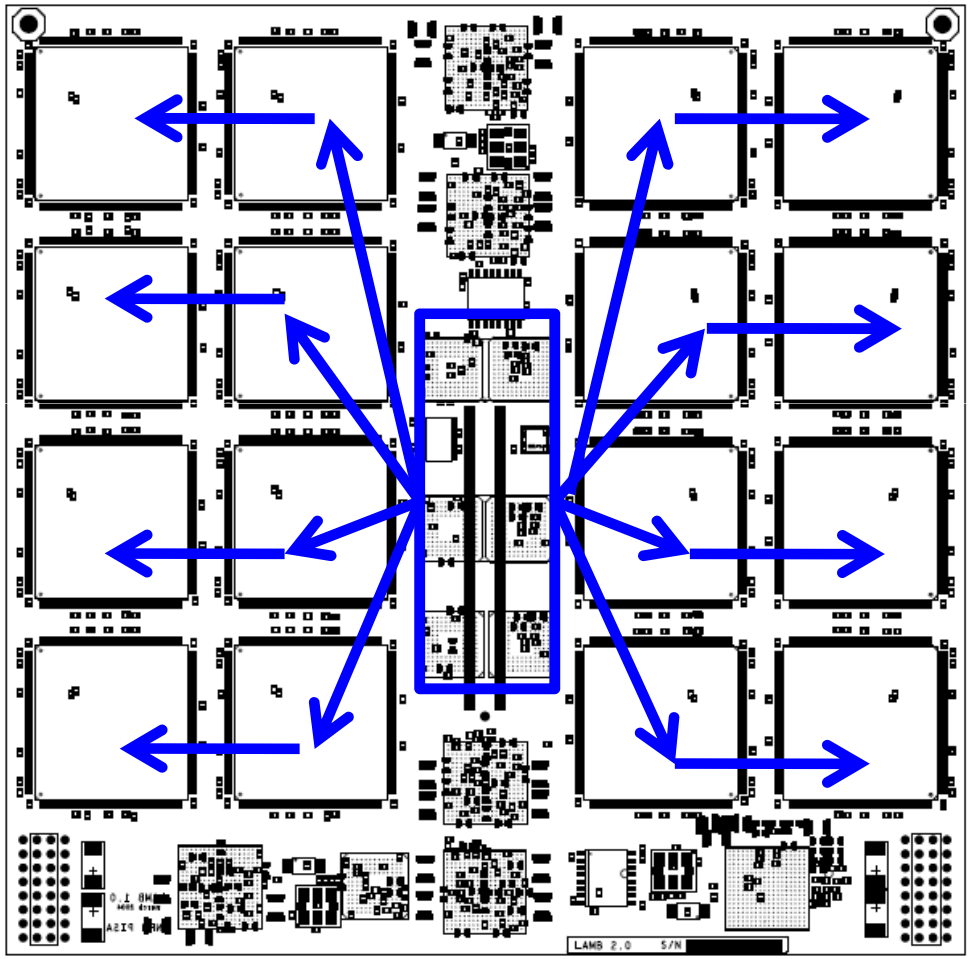
OLD	NEW	
6	**8**	#input buses
0	**4**	# serial link bus
6	**4**	# parallel link bus
1	**4**	# output bus

Level 2 LAMB



Core voltage @ 1.2 V
I/O voltage @ 3.3 V

Level 2 LAMB



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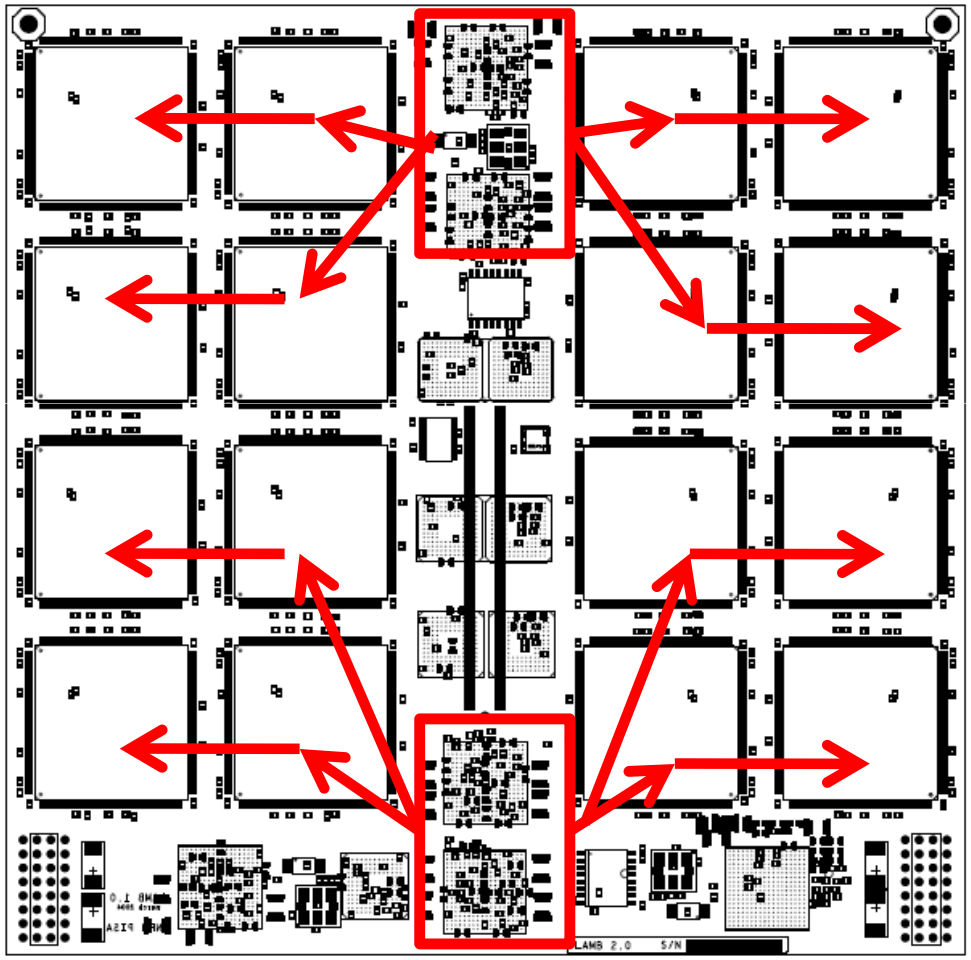
I/O voltage @ 3.3 V

CPLD – Input Distributor for parallel buses

4 bus parallel (0,1,3,5)

Level 2 LAMB



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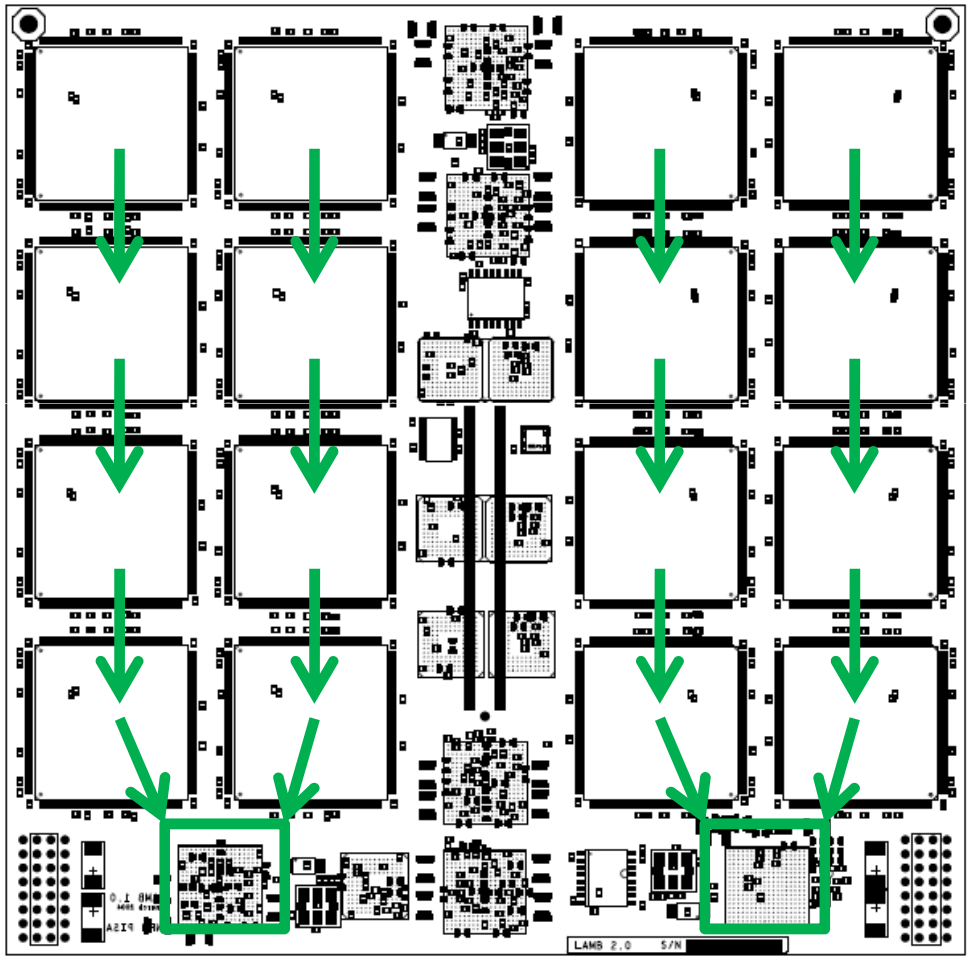
Spartan 6 – Input Distributor for serial buses

4 bus serial(2,4,6,7)

Level 2 LAMB



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I/O voltage @ 3.3 V

CPLD – Input Distributor for parallel buses

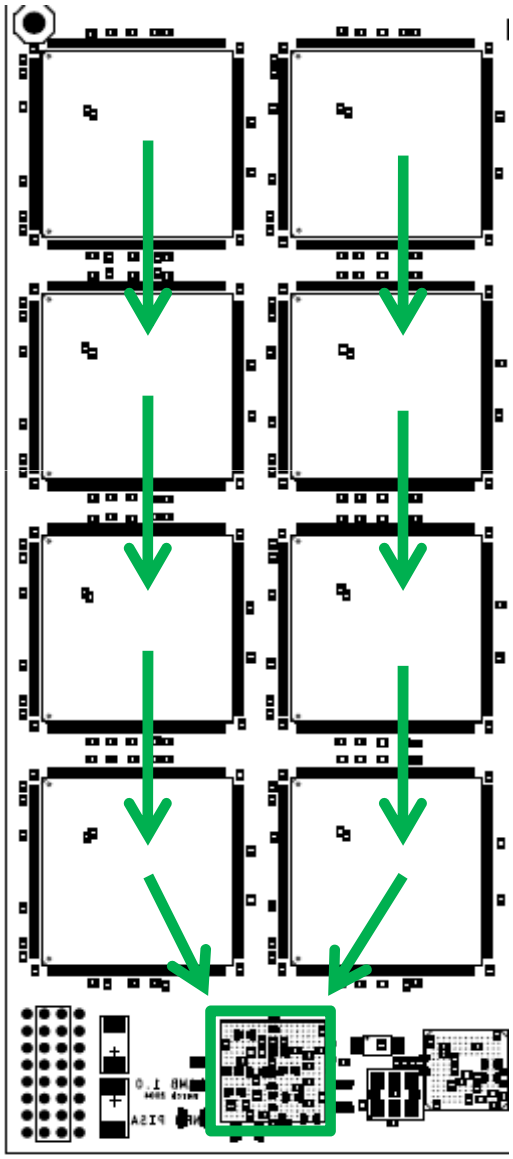
4 bus parallel (0,1,3,5)

Spartan 6 – Input Distributor for serial buses

4 bus serial(2,4,6,7)

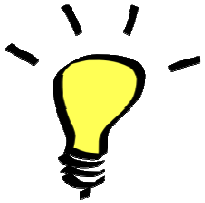
Spartan 6 – GLUE for output road

Limitation of current LAMB for L1 trigger



What is the limitation of LAMB?

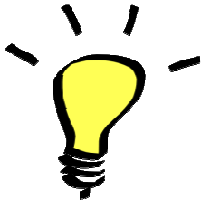
- Pipeline connection of AMchips



Star Connection

- All output flux from AMchip are connected at the GLUE

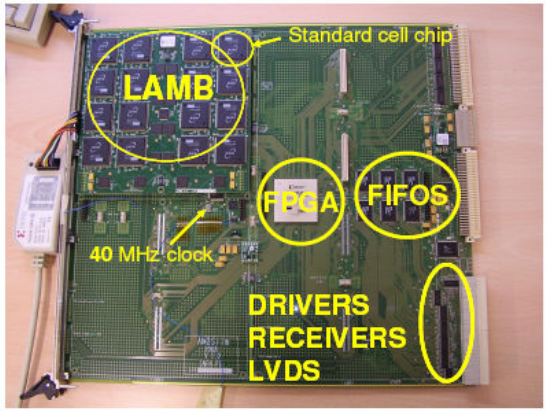
- Mixed standard (parallel and serial)

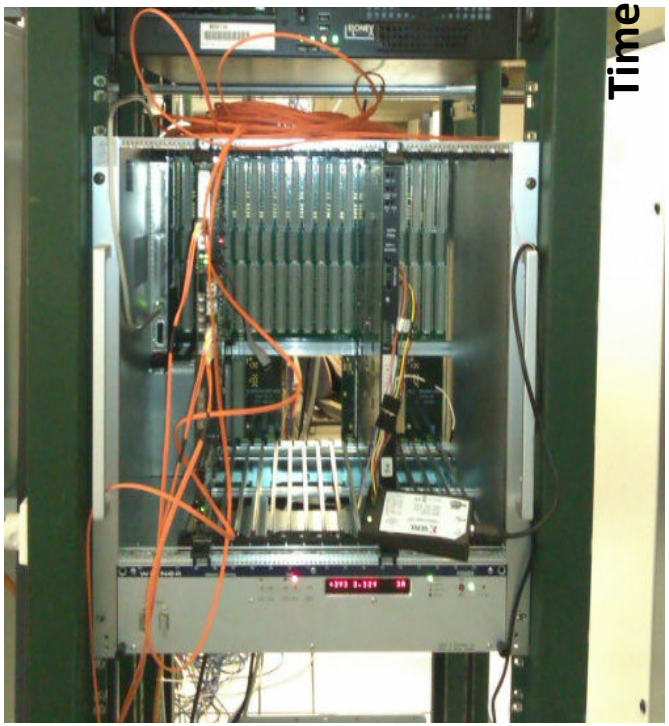


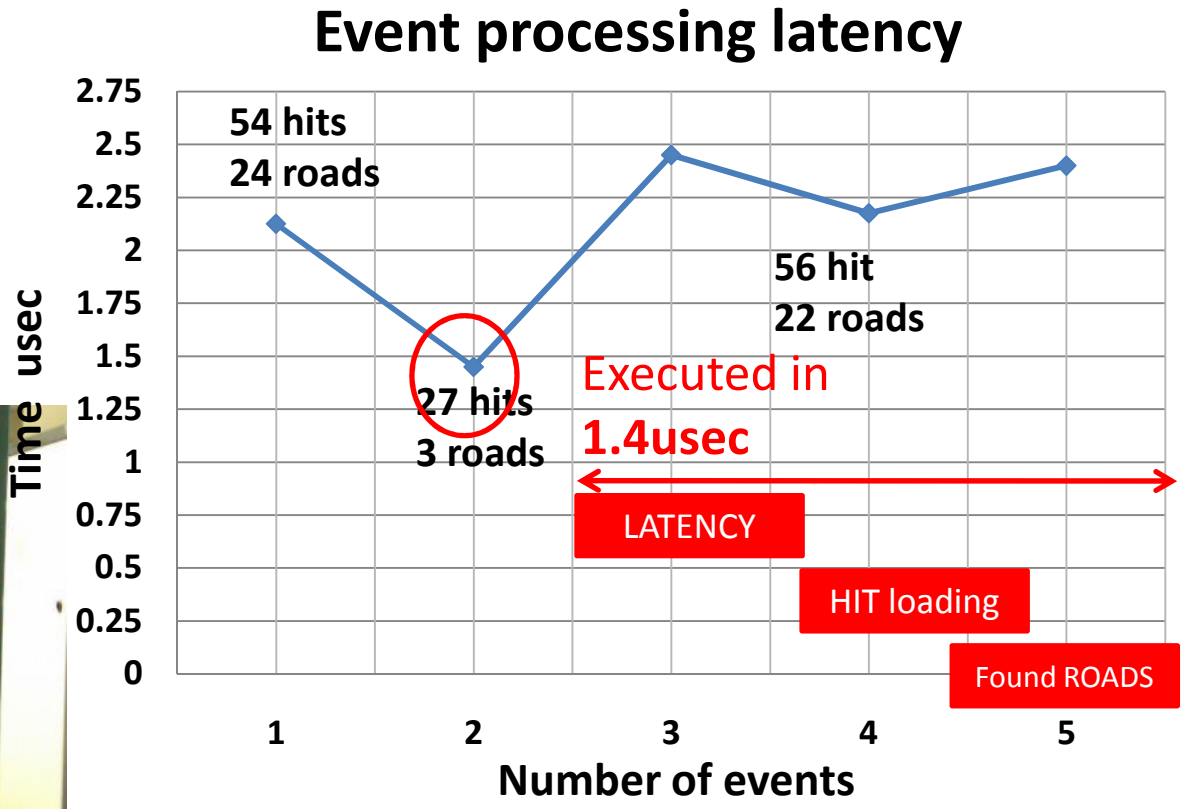
Serial Link

- Communication AMBOARD – LAMB and communication LAMB – AMCHIP will be ALL serial

Limitation of current LAMB for L1 trigger





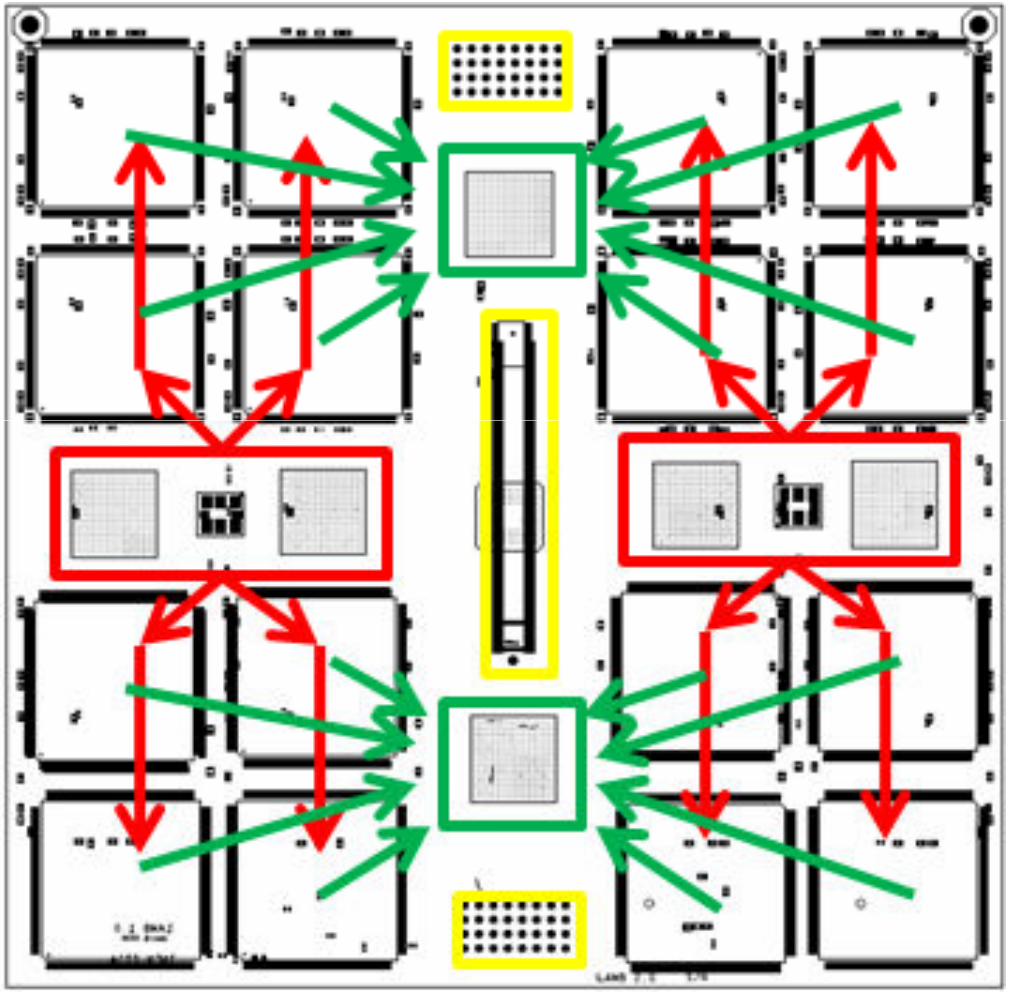


Period of clock **25ns** => reduce to **10ns (new AMChip)**

25 cycle to empty AMBoard – AMchip pipeline => **can be reduced**

Star LAMB for L1

16 serial links to GLUE



Spartan 6 – Input
Distributor for serial buses

Spartan 6 – GLUE for
output road

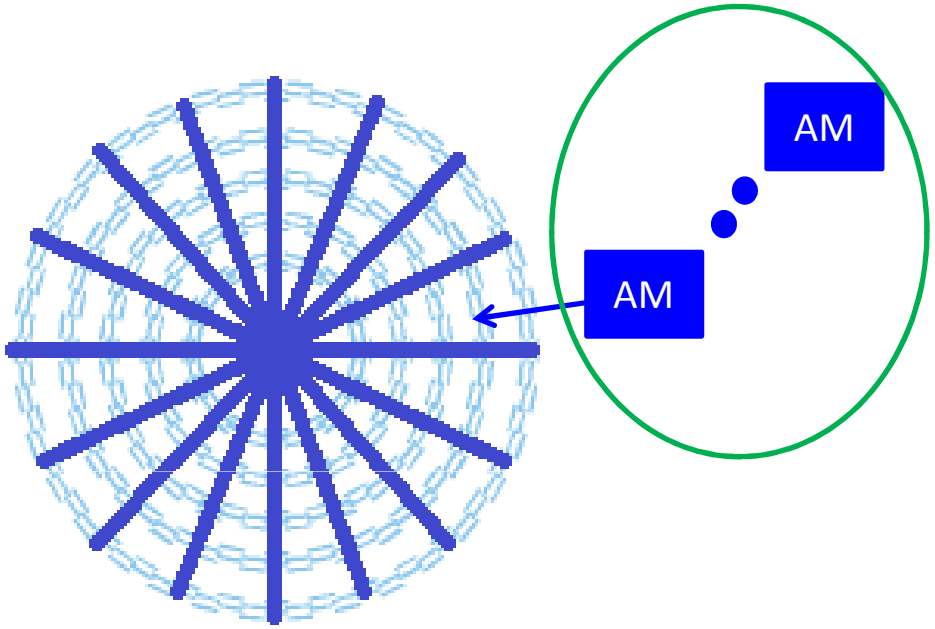
16 road flow in input of each FPGA – GLUE

Now Ratio 16 to 2

Increase number of serial link for output bus
Use more powerful and expensive FPGA

Future FPGA Ratio 1 to 1

Limits for the AM HW



2 or 4 boards x number of sectors?

~ 200 or 400 boards

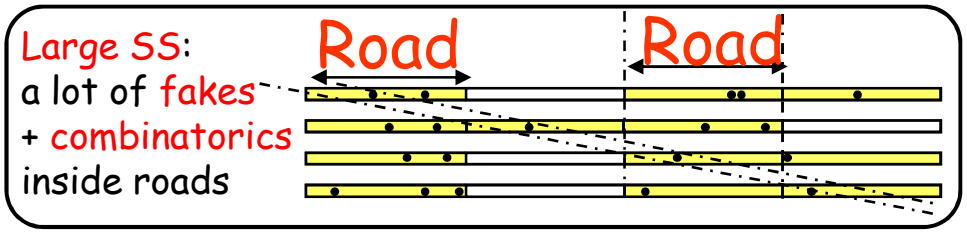
~ 10M patterns/board

What can we do if the number of pattern is not sufficient to reduce to ~ zero the fakes?

Would be useful to use the track fitting after the AM pattern matching to reduce the bank size keeping the fakes low.

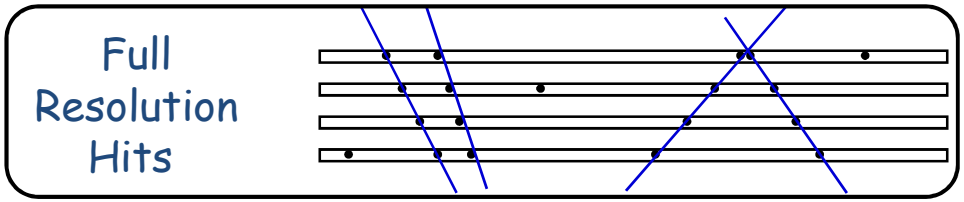
Fighting against FAKEs

Low resolution (large road size) produce a lot of fakes



ROAD SIZE: a parameter to balance the AM size & number of fake

High resolution (small road size) necessary to kill the fakes



It is necessary to use thin patterns -> large AM bank

Using the Track Fitting @ Level 1 we can use larger patterns & smaller banks

Logic density increases with time
Track Fitting possible @L1 in Phase II

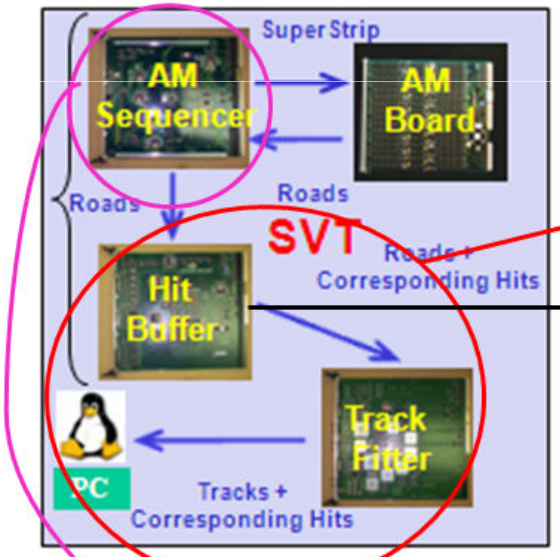
- SVT: yesterday
- FTK: today
- 2020?

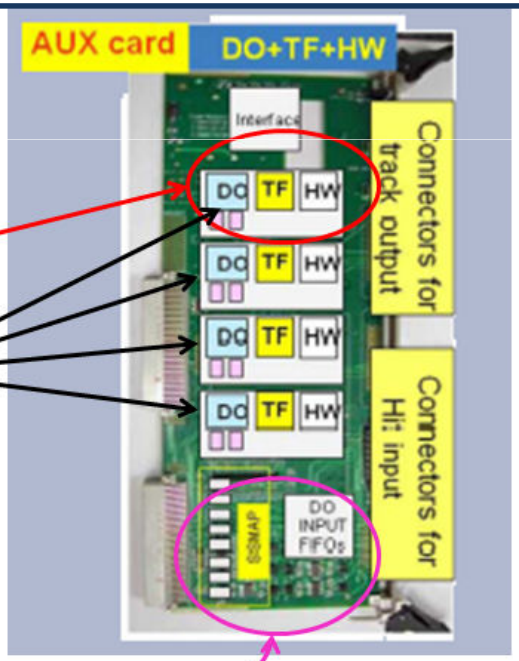
AMSequencer – Hit Buffer - Track Fitter
= 3 9U VME boards

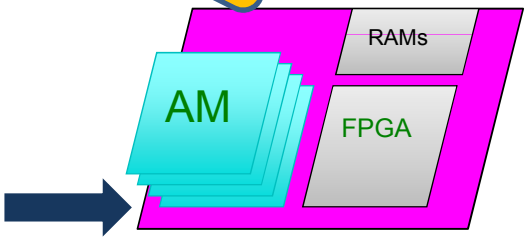
All in a mezzanine!
It's possible to multiply x 4

All in the AMchip!
It's possible to multiply x 128

See Ted Liu talk







LOW Latency
LOW cost

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Conclusion

- We have shown the use of the Associative Memory for L1 and L2 trigger **exploiting the existing HW**
- We have described an ongoing **HW improvement** of the AM system
- We have described a **new version of LAMB** necessary for **the L1 trigger applications**
- **Track Fitting could be feasible at L1** in the far future

BACKUP

How many patterns we could fit in modern FPGAs?

The present: choice based on cost and package:
XC6SLX150T-4CSG484 (19x19 mm^2) 4 GTPs 296 pins (our package is LQFP208)
373 $ today → 16400 AMchips → **6 M$**
23 k slices, even assuming **~8 slices/pattern →**
~2.9 k patterns/FPGA <<< 80 kpat/(our Amchip: 12x12 mm^2 65 nm)

The future http://www.xilinx.com/technology/roadmap/7-series-fpgas.htm
Best Virtex 7 XC7V200T (new family not available now)
305 k slices → ~ 38 kpatterns/FPGA < 80 kpat/(our Amchip)
Using FFs: **2,443 Mff → ~120 FF/pattern → ~ 20,4 kpat/FPGA**
Even using Slices and FFs together < 80 kpat/(our Amchip)

Even choosing the **best device of next years**
Even if we don't care about **cost and package**
Even with very **optimistic hypothesis** on a difficult design

we don't get our **AMchip power!**