From hybrids pixels to smart vertex detectors using 3D technologies

3D microelectronics technologies for trackers

Outlook

- **Introduction : Which technologies and what are the challenges ?**
- **A process "embedded" 3D : Tezzaron/ Chartered example**
- **Post-processed 3D : convenient processes for new tracker architectures ?**
- **Conclusions**

Which technologies for our challenges ?

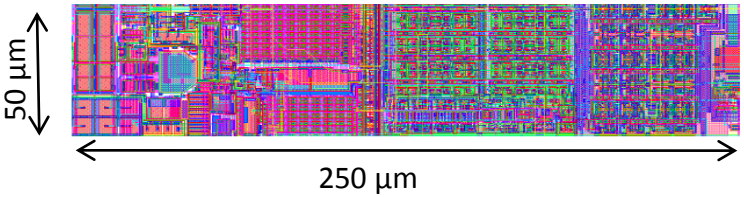
- **HL LHC : high luminosity, high pile up , high dose**
- **To keep the tracker performance one need to improve pixel granularity:**
  - reduce occupancy
  - improve resolution (and 2 tracks separation)
  - reduce inefficiencies in the readout
- **Several ways (solutions?) for pixels detectors themselves**
  - move to higher density technology like 65 nm
  - move to 3D electronics with in-pixel TSVs
  - move to CMOS HV (see talk I.Peric)
- **Ways for evolution of global architecture of the trackers**
  - Post-processed 3D →New module concepts

"Process embedded " 3D

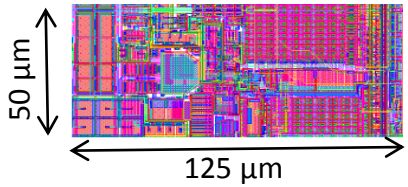
A disappointing experience ?

Goals

- **Reduce pixel area without changing tech. node by association of 2 or more layers of 3D technologies**



FE-I4 CMOS 130 nm



FE-TC4 CMOS 130 nm 2 layers

- Needs in-pixel communication between the 2 tiers → small TSVs → part of the process itself
- Main advantage : Adequate techno selection for the various functions
- Main drawback : Few (very few) vendors at the moment

Tezzaron-Chartered 3D run

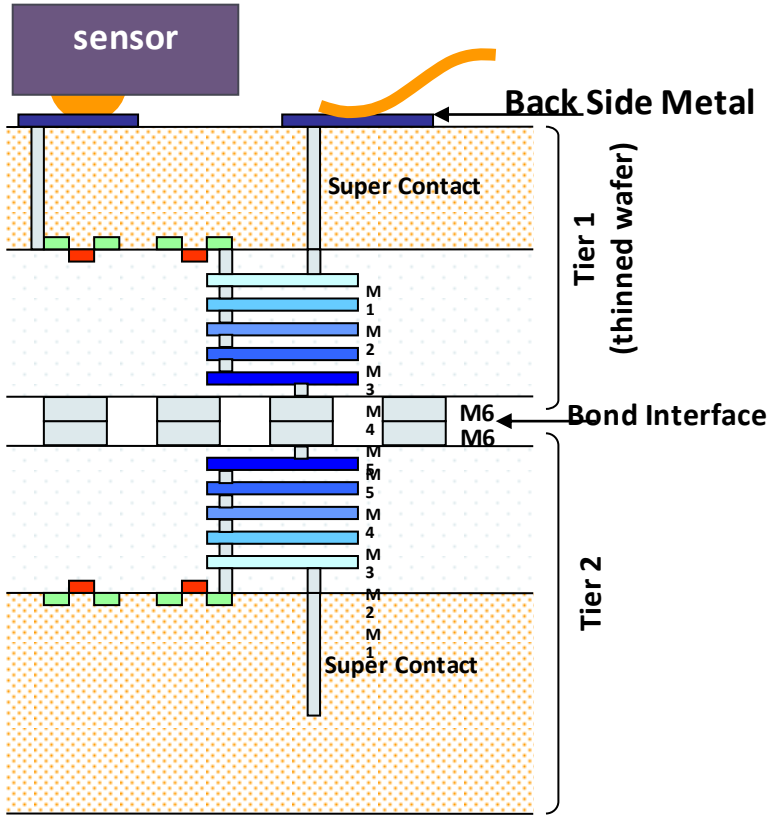
- **3D consortium created in 2008 (with MAPS and Hybrid pixel communities) and 3D run in 2009**

Main technology features

- 130 nm
- Large reticle (≈26 x 30 mm)
- 6 metal levels (M6 is the bond interface)
- Wafer to wafer, face to face bonding
- Vias 1.6 x 1.6 µm with 3.2 µm pitch
- Bond interface : copper
- Upper tier thinned down to 10 µm

Many production problems

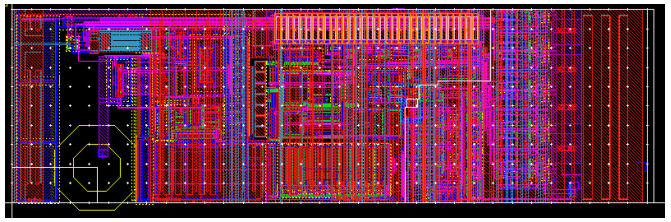
- Design rules evolution
- Chartered-GF restructuration
- Tezzaron hybridization tools



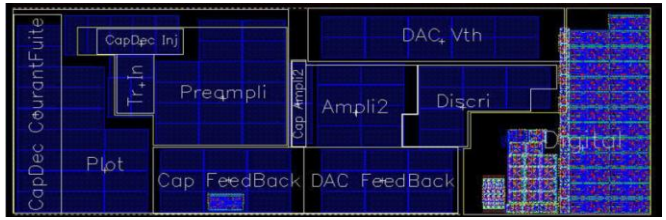
No complete 3D at the moment but some interesting results

FE-TC4-P1

- Pixel matrix of 14 x 61 pixels , pixel size 50 x 166 µm
- Analog tier is very close to FE-C4-P1 (GF version of FE-I4-P1)
- Digital tiers in 2 flavors : DC (Bonn design) close to FE-I4 one, DS not intended for read-out but for studying coupling between tiers
- Only one electrical connection per pixel (discriminator output)
- Design of each tier allow separate test (even in 3D stack)



FE-TC4 analogue part



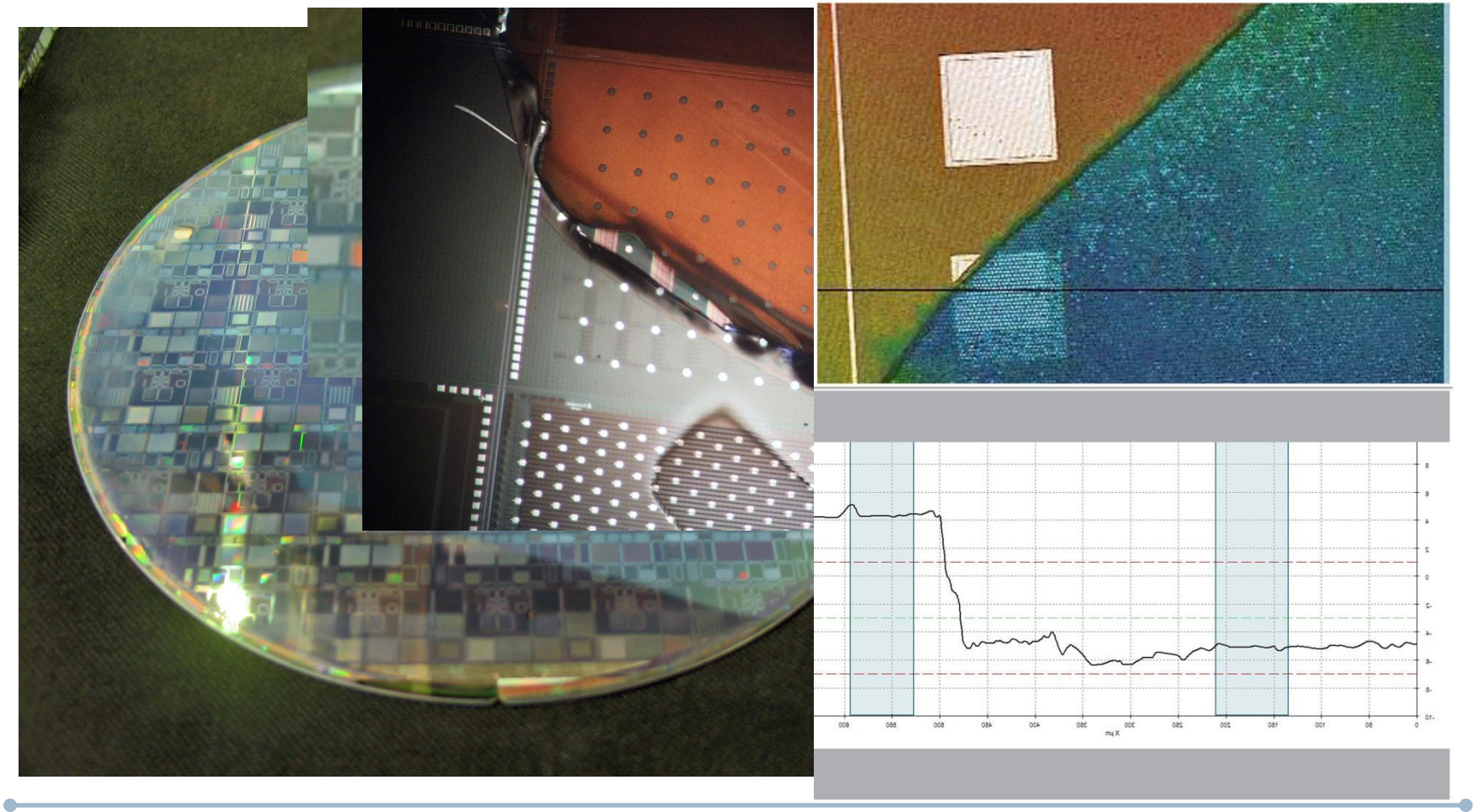
FE-TC4 digital simple part

Analog tier, DC tier, DS tiers tested separately (February 2011)

First 3D assemblies AE-DC and AE-DS arrived in (September 2011)

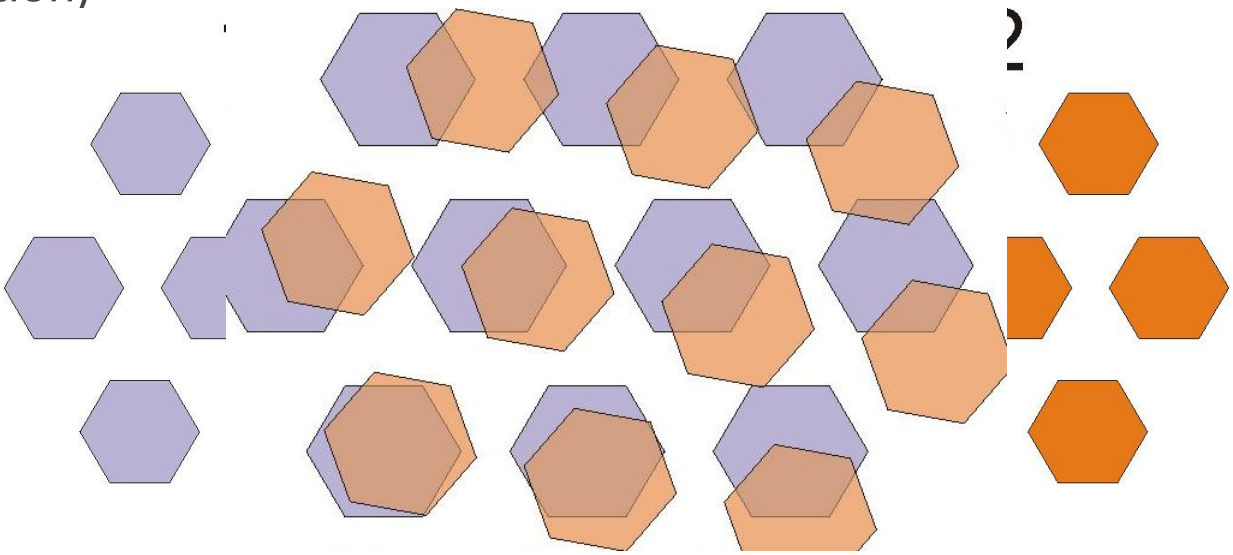
3D wafers

- **Defects visible to the naked eye**



What's happened?

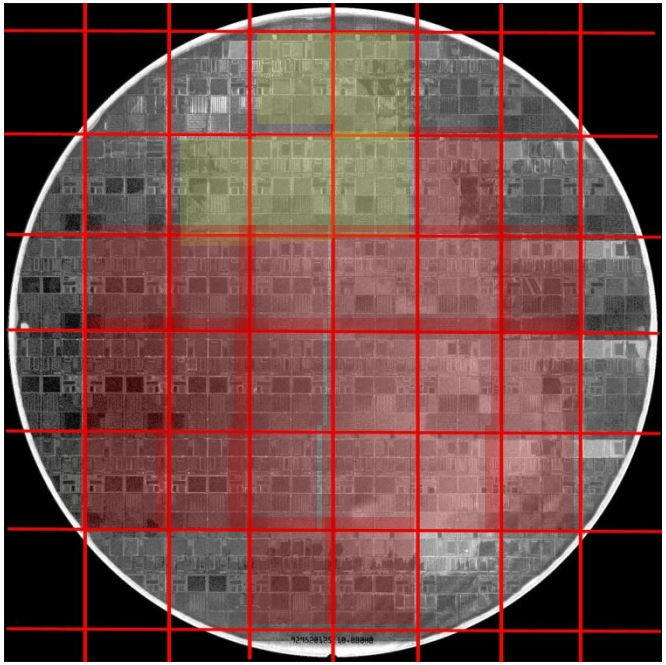
- **Bond interface between 2 wafers is done by dense copper bonds**
  - These bonds are mainly mechanical (just few of them have electrical function)



  - Alignment should be "perfect" to avoid poor mechanical adhesion → Problem in thinning top wafer and massive short

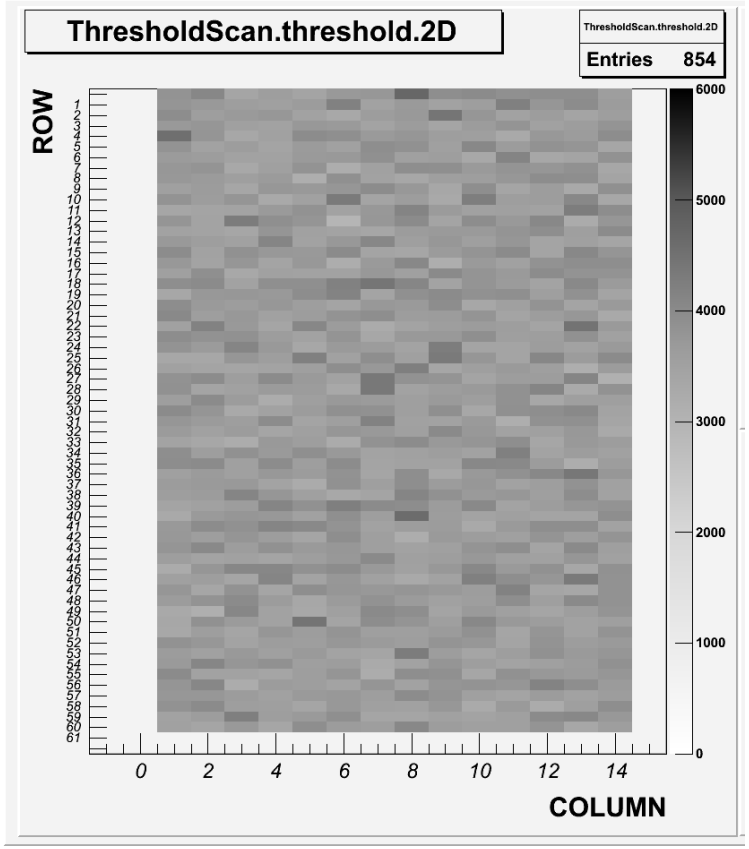
Results

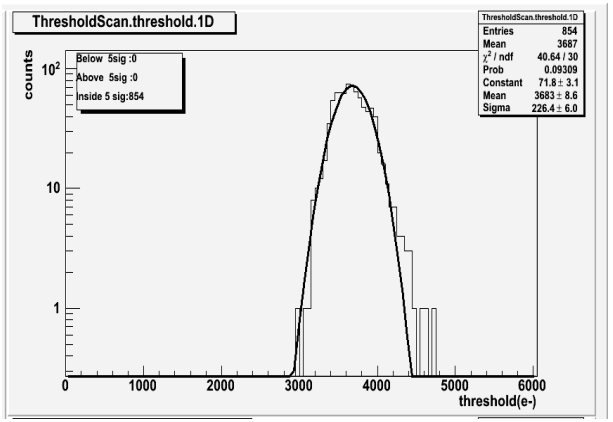
- **Only few chips on the wafers should be powered →**
  - Other ones having massive shorts between power supplies
- **After dicing and wire-bond of these few chips**
  - The 2 tiers can be operated separately (tier at the bottom is powered through the top one)
  - No one chip demonstrates in-pixel communication

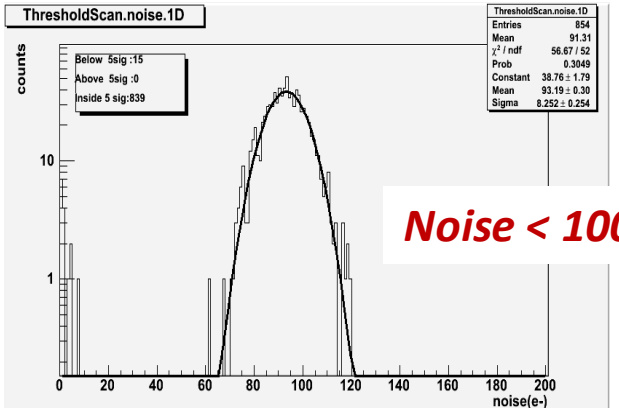


Analogue part

- **The 10 µm thick analog part behaves as un-thinned one**





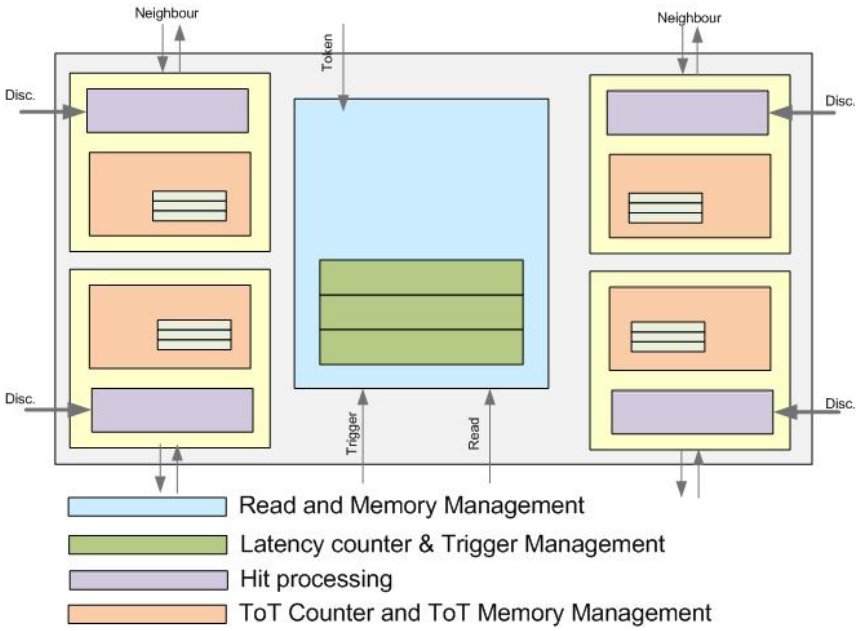


Noise < 100 e- rms

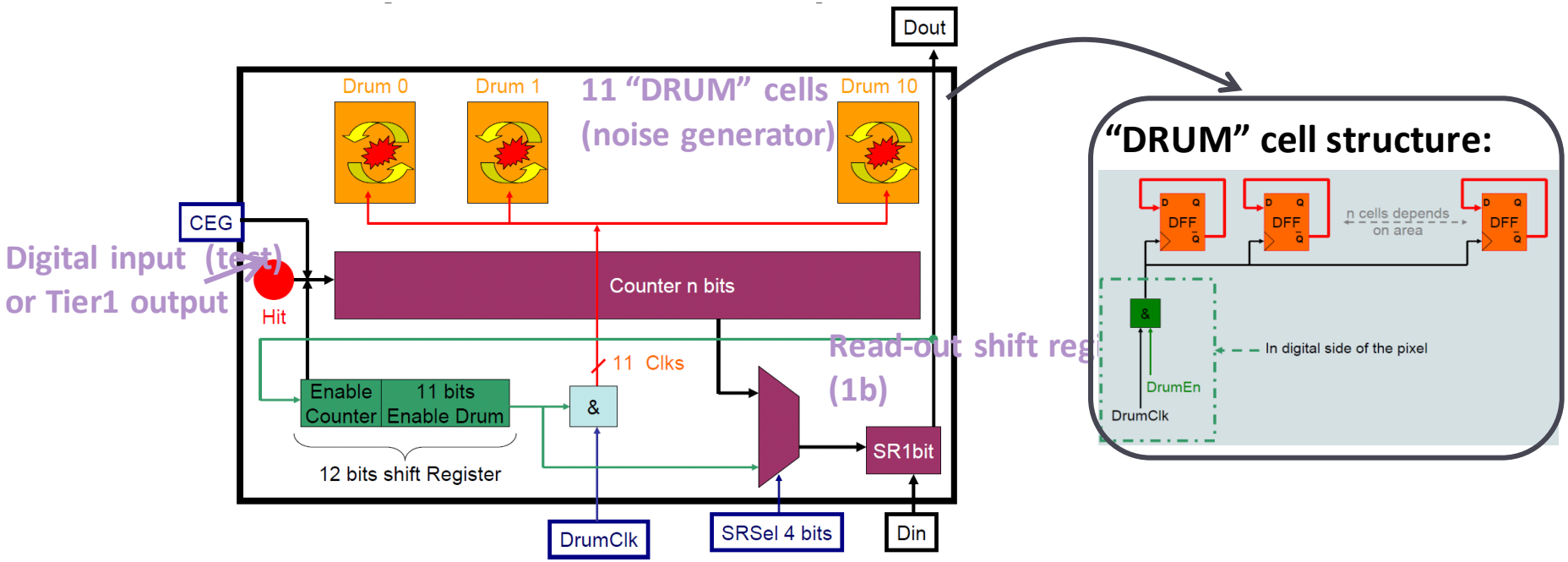
Complex digital fully working

- **"A la FE-I4" read-out**
  - 4 pixel regions
  - Simplified periphery and control logic
  - Fully tested at Bonn

Fully working even if the floating inputs (due to unconnected analog pixels) produce spurious hits



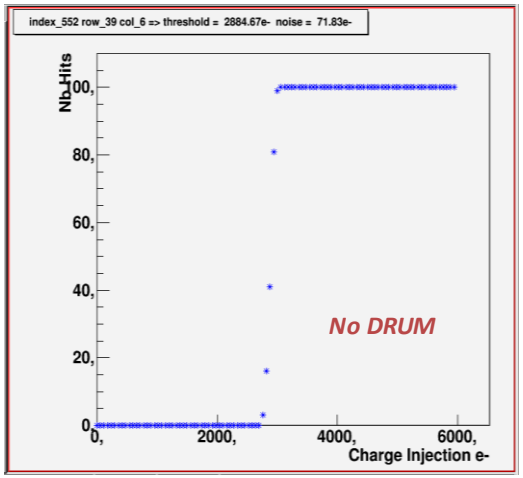
Shielding studies with Digital Simple



Test Shielding strategy :

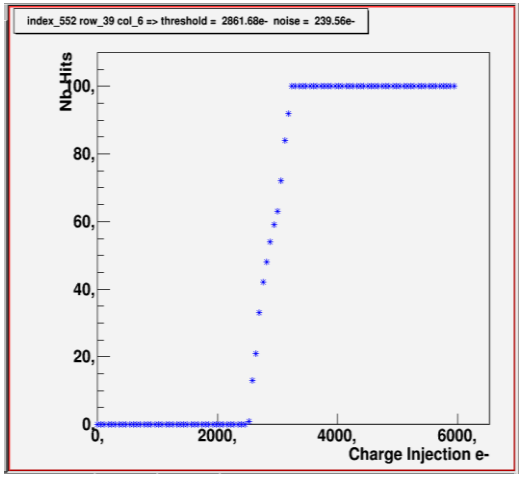
- **5 columns without any shielding (reference),**
- **4 columns with shielding in metal 5,**
- **2 columns with shielding in metal 3,**
- **2 columns with both shielding.**

S curves with "Drums" activation



Col 6 Row 39
(no shielding)

72e- → 240 e-



- **If no shielding → Noise increase by a factor 3 !**
- **Shielding with M5 proved to be efficient (no difference with/ without digital activity)**

Conclusions for "in-process" 3D

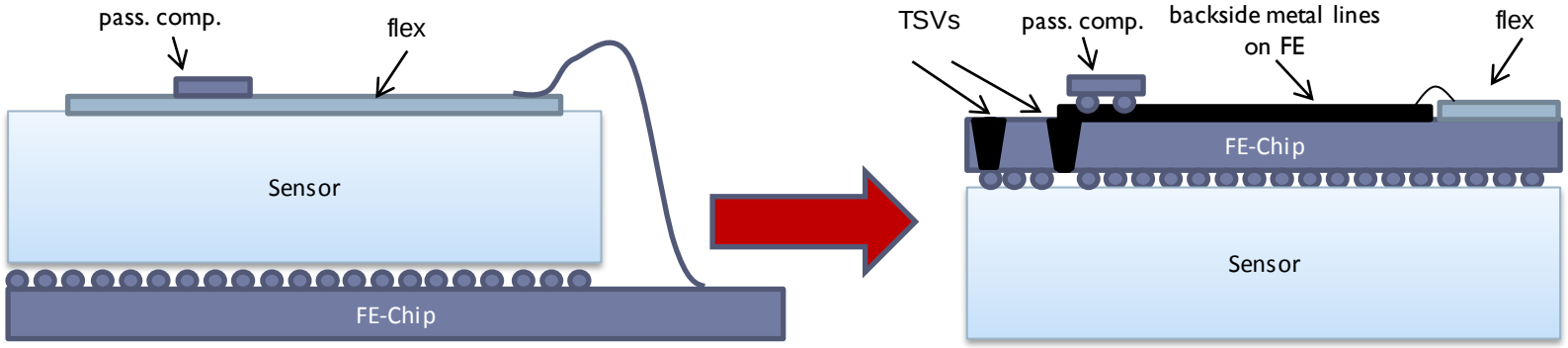
- **A "leaning" 3D stack**
  - Many difficulties during the process (3 years !!)
  - But :
    - 2D technology (Chartered/GF) results compatible with IBM ones even for radiation hardness
    - **No performance degradation with thinning (10 µm)**
  - Run replaced for free (we are again waiting for the wafers !)
  - New runs foreseen this year (through CMP / Mosis)

"Post-processed 3D"

New ways to build trackers?

Purposes

- **Look at the 3D post-process capabilities in order to find new ways to build modules and staves**
  - Material reduction (estimation for IBL : 0.13% of X_0)



  - Direct connection of service lines (or flex) on chips bakside

Ongoing efforts

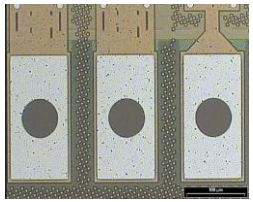
- **Various groups working in this direction in ATLAS**
  - Orsay(LAL), Munich, Bonn, CPPM
- **2 main Europeans vendors**
  - IZM (Berlin and Munich)
  - LETI (Grenoble) with 3D initiative

IZM Berlin / Bonn University

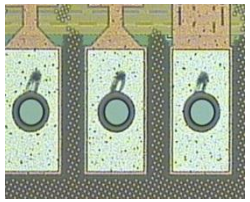
SI LAB
Silizium Labor Bonn

Front side processing

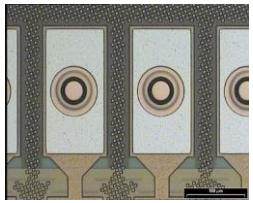
Al pad opening by wet etching



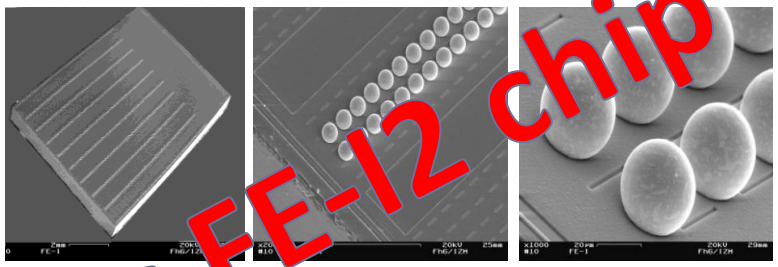
BEOL SiO_2 stack etching



Cu electroplating – interconnection plug to Al pad

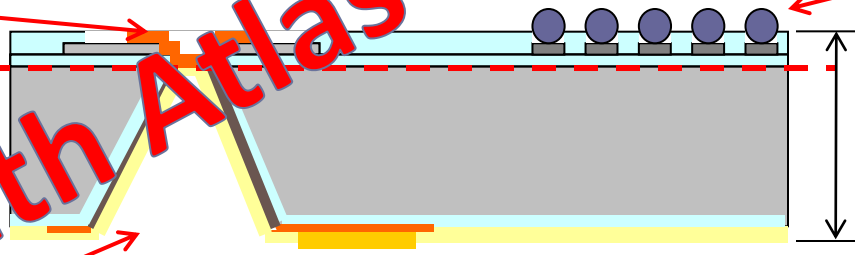


Bump deposition and dicing



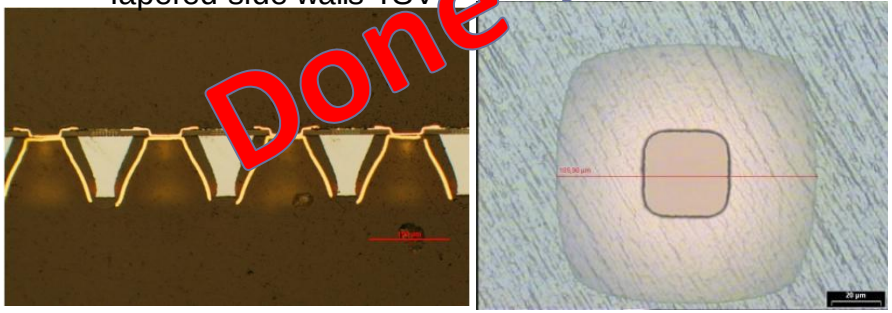
Done with Atlas FE-I2 chip

Back side processing

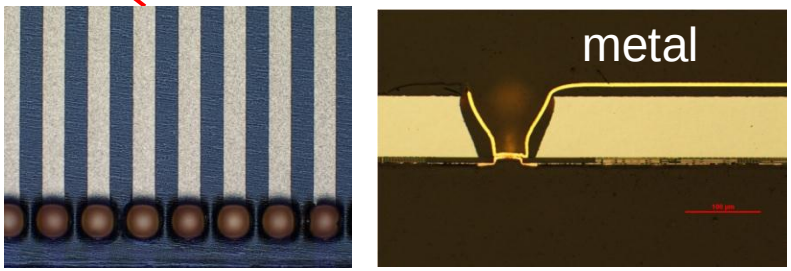


Thin chip!
90µm

Tapered side walls TSV



Backside redistribution

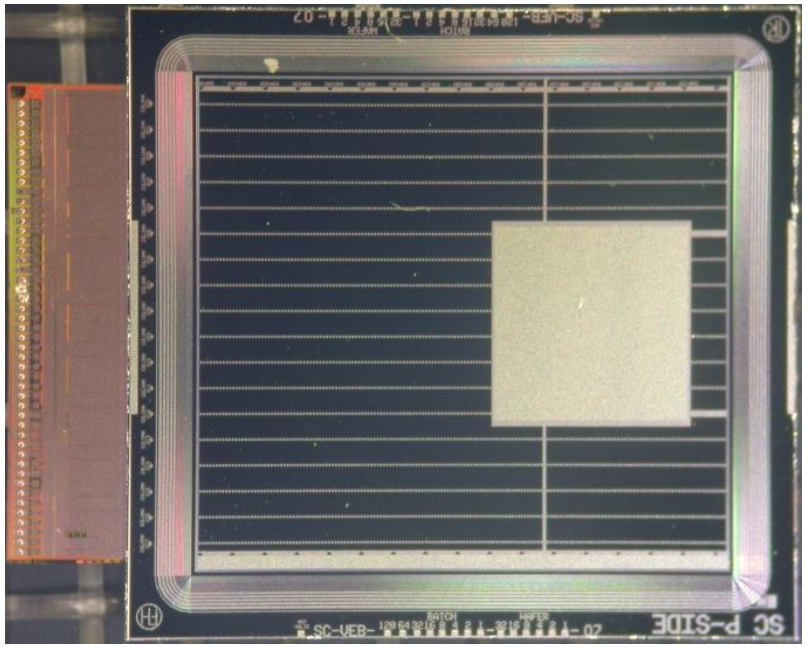


FE-I2 modules with TSV

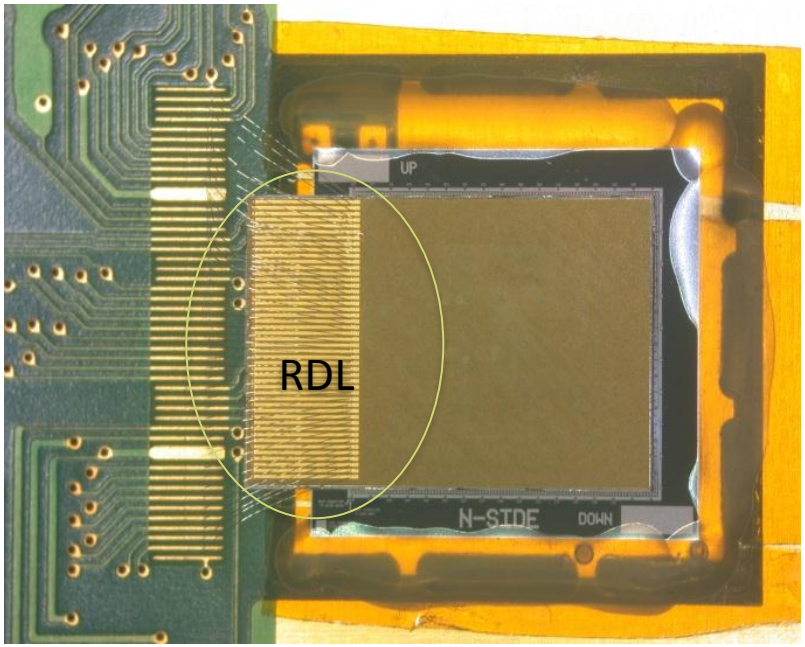
- **FE-I2, 90 µm thick with TSV et RDL**
- **Hybridized on N-N sensor**
- **2 mounted on board**

SI LAB
Silizium Labor Bonn

Module front side



Module "backside"



FE-I2 modules with TSV

- **Chips with TSV are working fine**
  - No extra noise induced by TSV process
  - But lot of disconnected pixels → No handle wafer used

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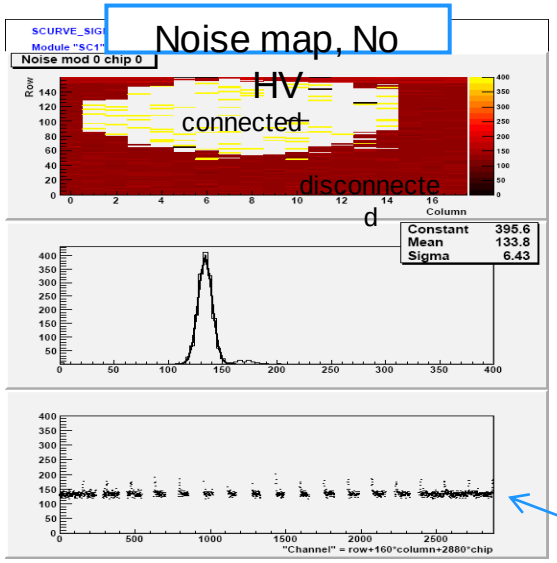

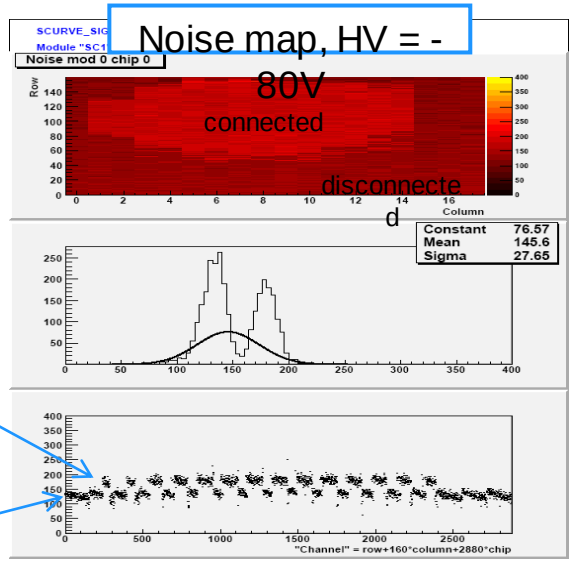

Connected pixels: **~180e**

Disconnected pixels: **~130e**

- **Use FE-I4 chip and the thin flip chip method yet used for FE-I4**
- **Bonn/CPPM with Aida funding**

Conclusions

- **3D microelectronics technologies are rapidly evolving (with the industry needs).**
- **Interesting results for our community are yet obtained**
- **These technologies could certainly offer some "revolution" in tracker world**
  - New modules and stave concepts
  - Coupling HV-CMOS sensor with RoC by direct copper bonding?