A hybrid module architecture for a prompt momentum discriminating tracker at HL-LHC

WIT2012 Workshop on Intelligent Trackers
3-5 May 2012, INFN Pisa

Outline

- Motivation
- General concept
- Module assembly
- ASIC functionality
- Overview of module features
- Further improvements
- Conclusions and outlook

Outline(*)

- Motivation
- General concept
- Module assembly
- ASIC functionality
- Overview of module features
- Further improvements
- Conclusions and outlook

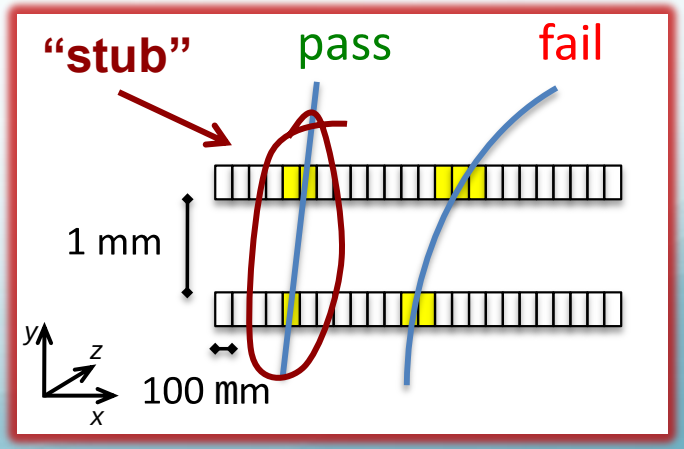
(*) Most of the ideas and the work by A. Marchioro.
All the credit (and all the nasty questions) to him!

Motivation

- Tracker input to Level-1 trigger
  - μ, e and jet rates would exceed 100 kHz at high luminosity
    - Even considering "phase-1" trigger upgrades
  - Increasing thresholds would affect physics performance
    - Performance of algorithms degrades with increasing pile-up
      - Muons: increased background rates from accidental coincidences
      - Electrons/photons: reduced QCD rejection at fixed efficiency from isolation
  - Add tracking information at Level-1
    - Move part of HLT reconstruction into Level-1!
- Full-scope objectives:
  - Reconstruct "all" tracks above 2 ÷ 2.5 GeV
  - Identify the origin along the beam axis with ~ 1 mm precision
  - Goals:
    - Maintain overall L1 rate within 100 KHz
    - Keep latency within ~ 6 μs (ECAL pipeline 256 samples = 6.4 μs)
      - The current limit is the Tracker

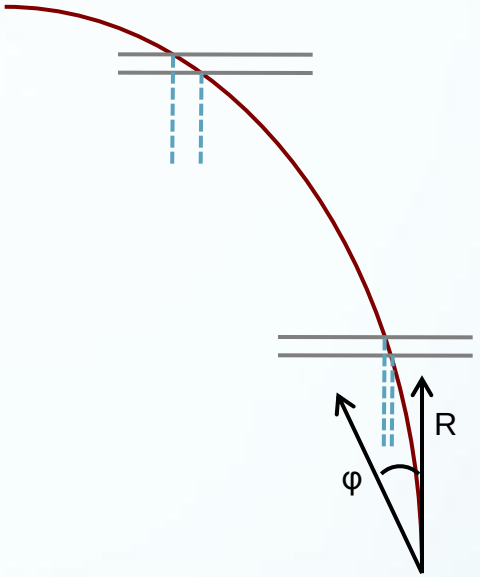
General concept

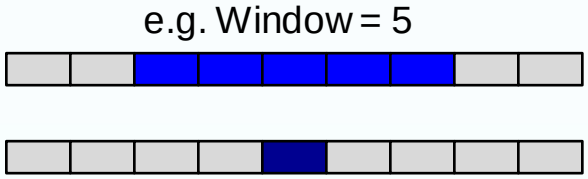
- Silicon modules provide at the same time "Level-1 data" (@ 40 MHZ), and "readout data" (@ 100 kHz, upon Level-1 trigger)
  - The whole tracker sends out data at each BX: "push path"
- Level-1 data require local rejection of low-p_T tracks
  - To reduce the data volume, and simplify track finding @ Level-1
    - Threshold of ~ 1÷2 GeV ®data reduction of about one order of magnitude
- Design modules with p_T discrimination ("p_T modules")
  - Correlate signals in two closely-spaced sensors
    - Exploit the strong magnetic field of CMS
- Level-1 "stubs" are processed in the back-end
  - Form Level-1 tracks, p_T above 2÷2.5 GeV
    - To be used to improve different trigger channels



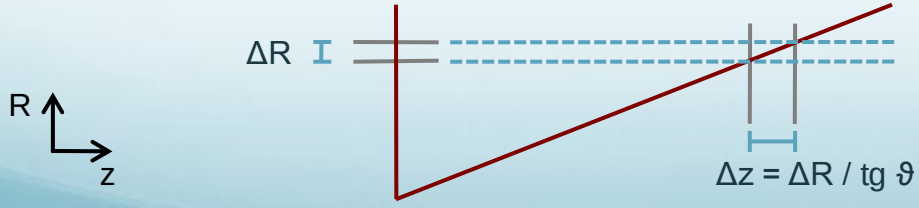
More on p_T modules working principle

- Sensitivity to p_T from measurement of $\Delta(R\varphi)$ over a given ΔR
- For a given p_T, $\Delta(R\varphi)$ increases with R
  - A same geometrical cut, corresponds to harder p_T cuts at large radii
  - At low radii, rejection power limited by pitch
  - Optimize selection window and/or sensors spacing
    - ★ To obtain, ideally, consistent p_T selection through the tracking volume





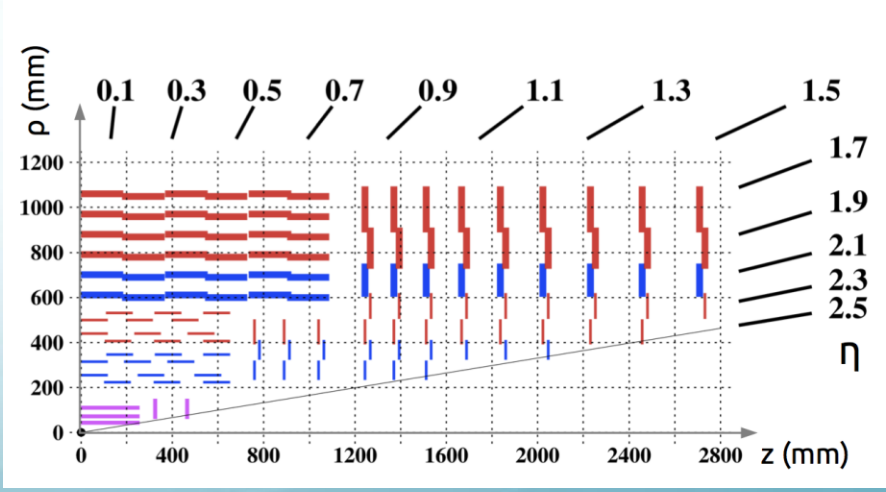
- In the barrel, ΔR is given directly by the sensors spacing
- In the end-cap, it depends on the location of the detector
  - End-cap configuration typically requires wider spacing



p_T modules in the CMS Tracker Upgrade

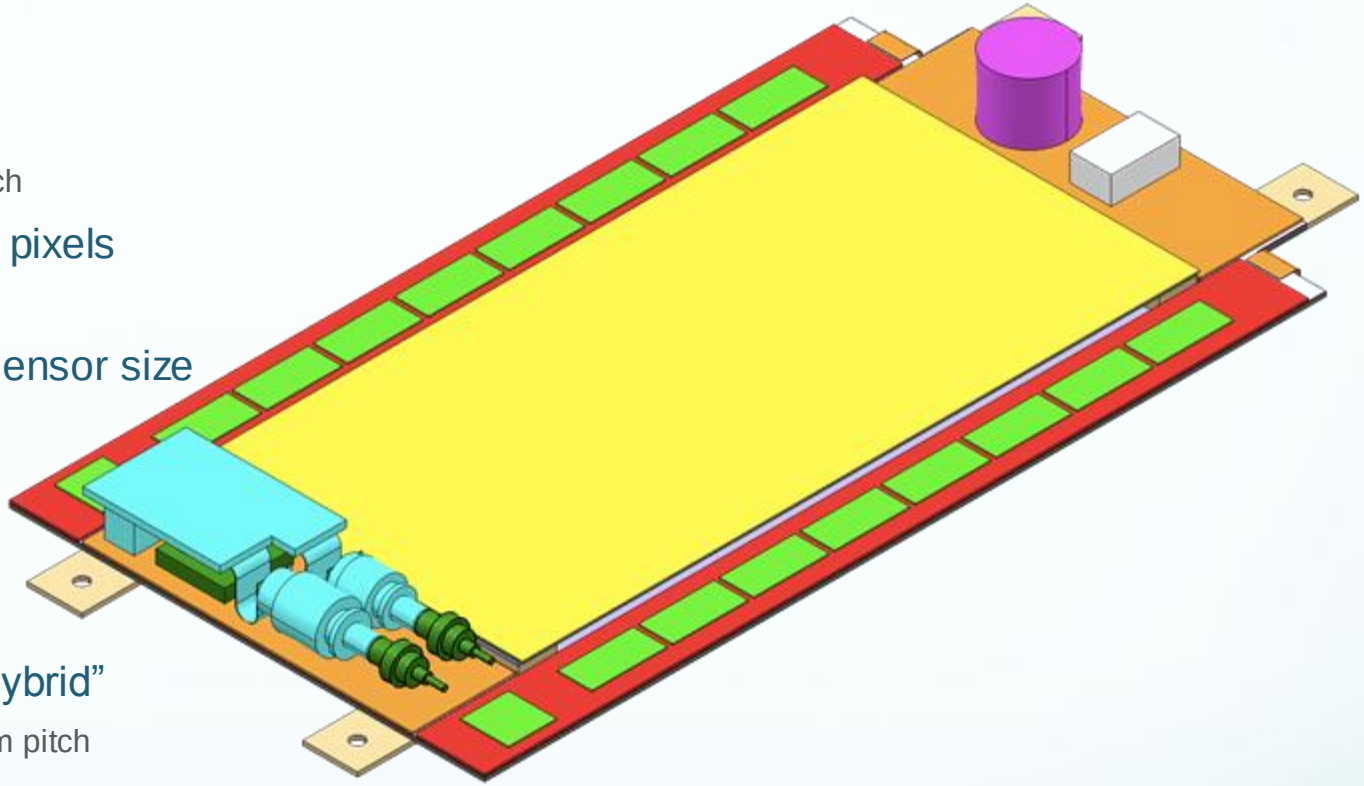
- The current CMS Outer Tracker covers the radial range [20:110] cm
- The region R>35 cm in the barrel can be covered by adjusting the acceptance window
- At lower radii, or in the endcap, tuning also the sensor spacing might be helpful (or necessary)
- Pixellated modules are required to gain z_0 resolution
  - 1÷2 mm long pixels
  - At least in ½ of the tracking volume

The CMS Tracker

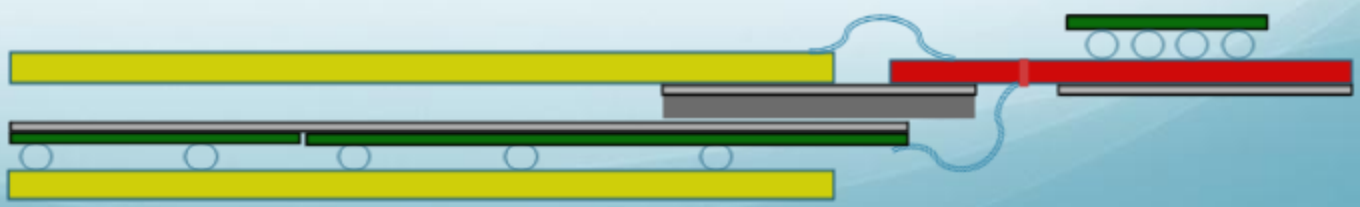


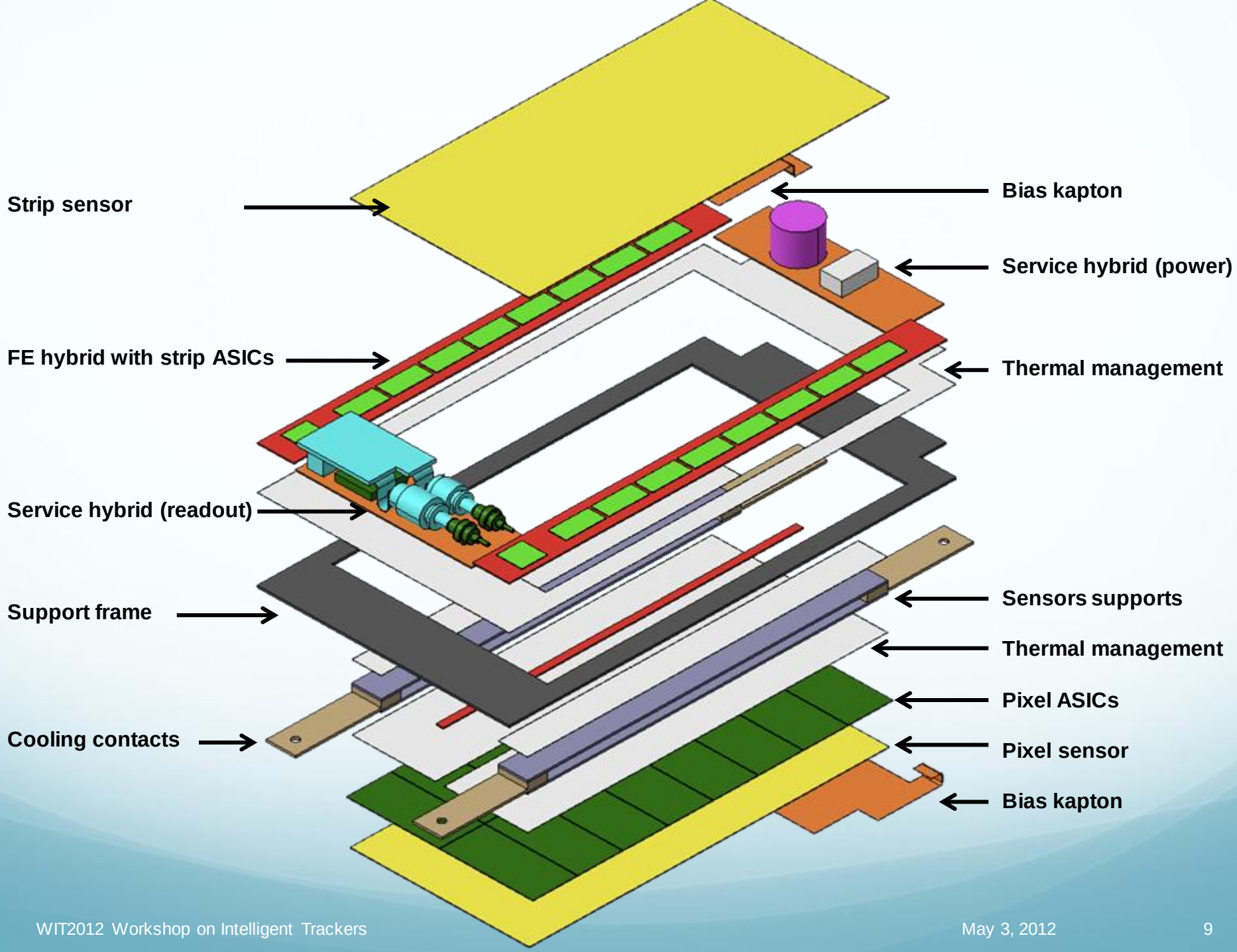
The PS (Pixel-Strip) module

- Sensors:
  - Top sensor: strips
    - 2×25 mm, 100 μm pitch
  - Bottom sensor: long pixels
    - 100 μm × 1500 μm
  - ≈ 5x10 cm^2 overall sensor size

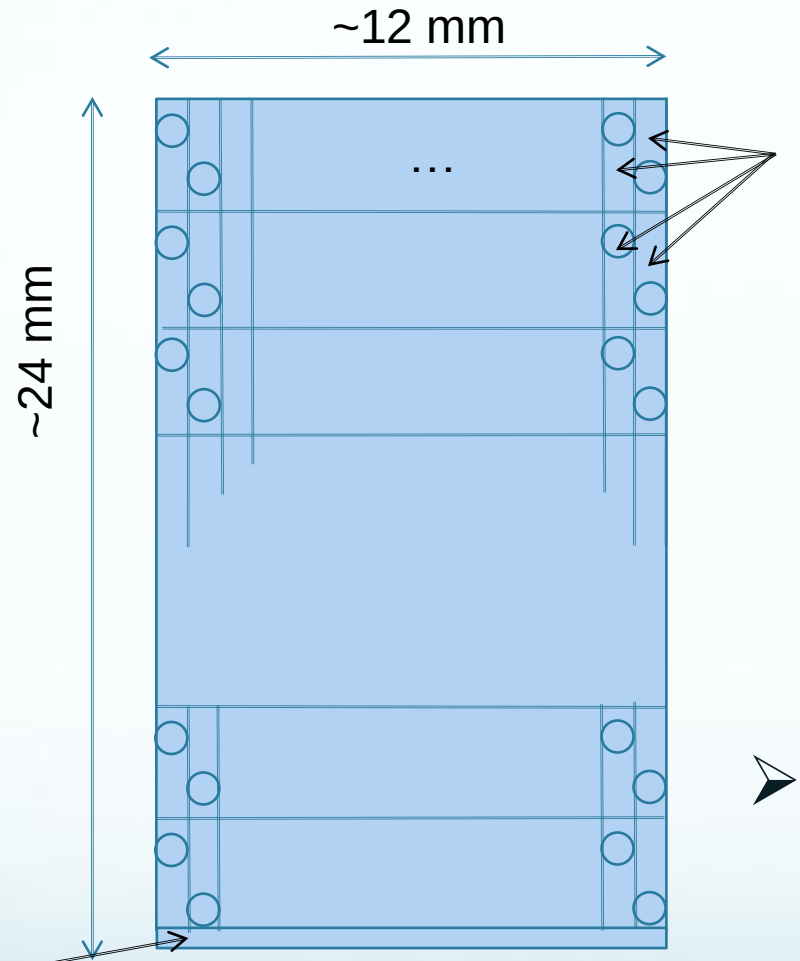


- Readout:
  - Top: wirebonds to “hybrid”
    - 1 wire per strip, 100 μm pitch
  - Bottom: pixel chips wirebonded to hybrid
    - 2 wires per pixel row, 50μm pitch
  - Correlation logic in the pixel chips
  - C4 bump-bonding




Strip sensor
FE hybrid with strip ASICs
Service hybrid (readout)
Support frame
Cooling contacts
Bias kapton
Service hybrid (power)
Thermal management
Sensors supports
Thermal management
Pixel ASICs
Pixel sensor
Bias kapton

Macro-Pixel-ASIC global floorplan

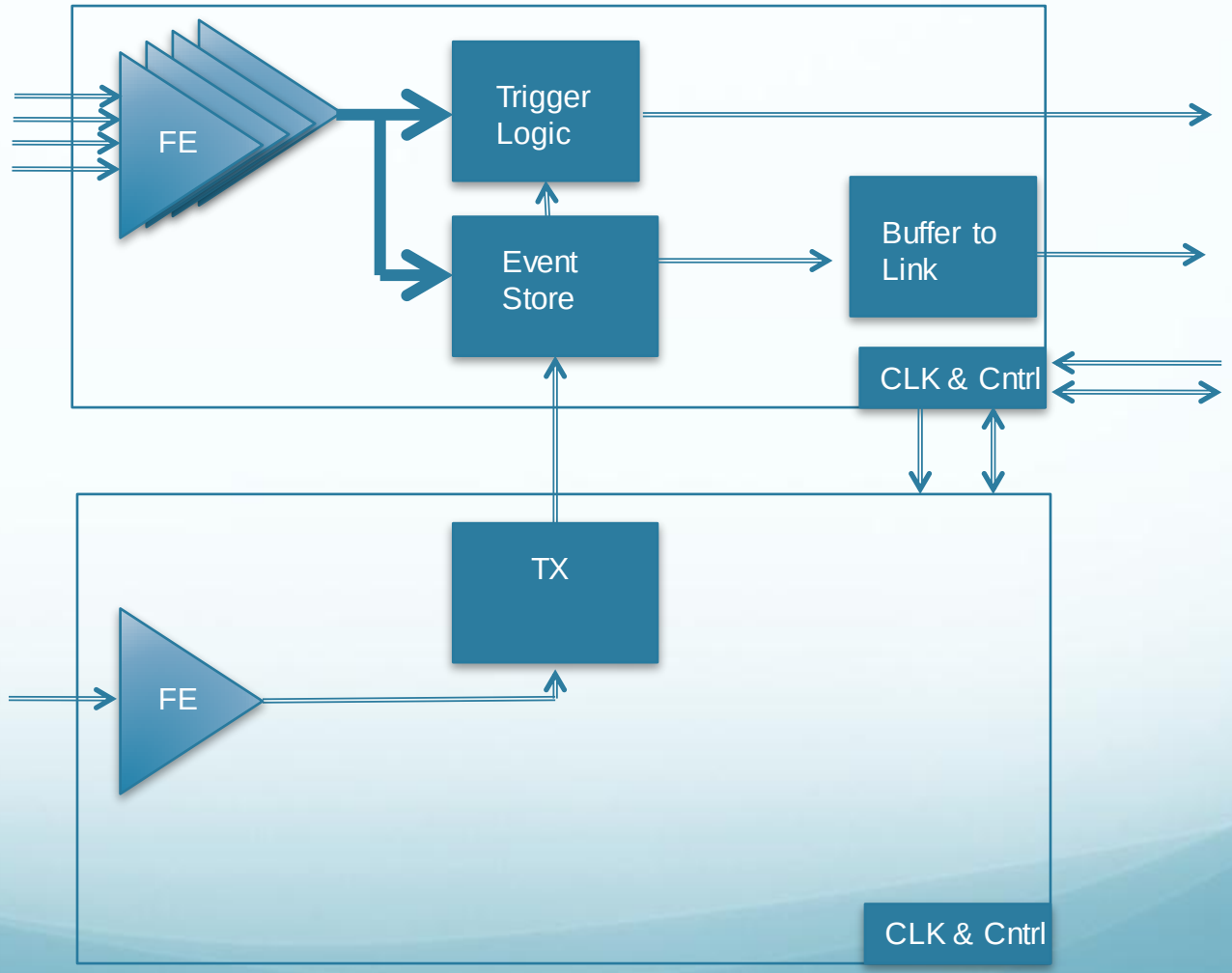


- MPixel ASIC size:
  - ~ 12 x 24 mm2
  - Pixel size: ~ 100 µm x 1500 µm
  - # pixels: 128 x 16 = 2048
  - Readout on one edge only

Module functional block diagram

- Coincidence and data handling in the pixel ASIC

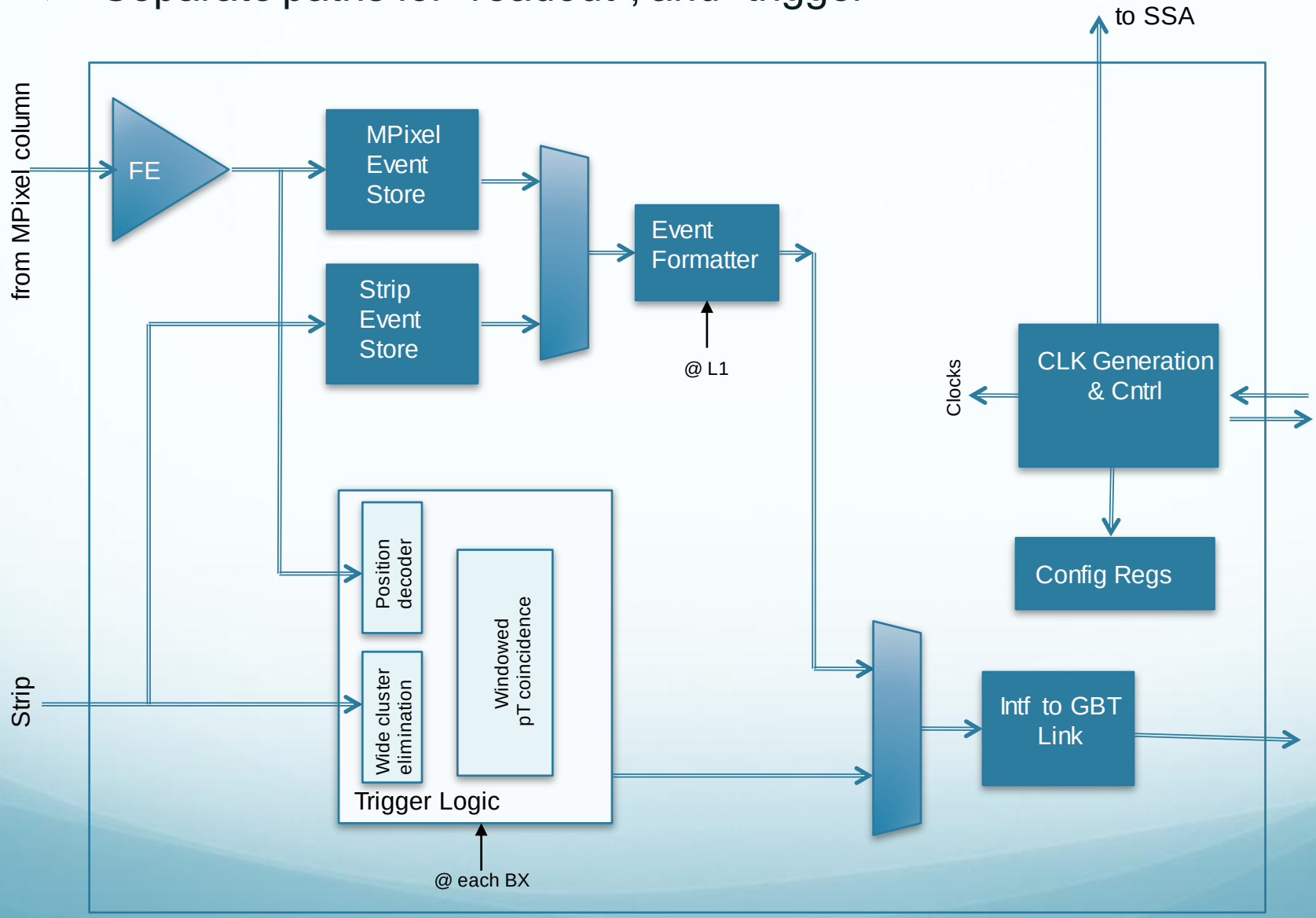
Pixel Layer
MPA



Strip Layer
SSA

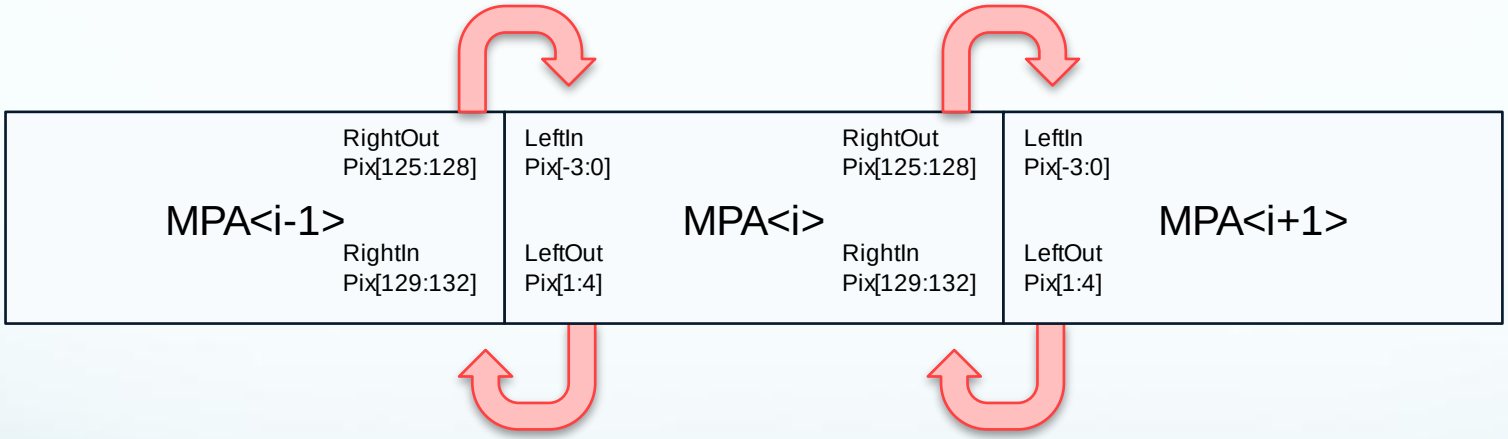
MPixel ASIC: more details

- Separate paths for “readout”, and “trigger”



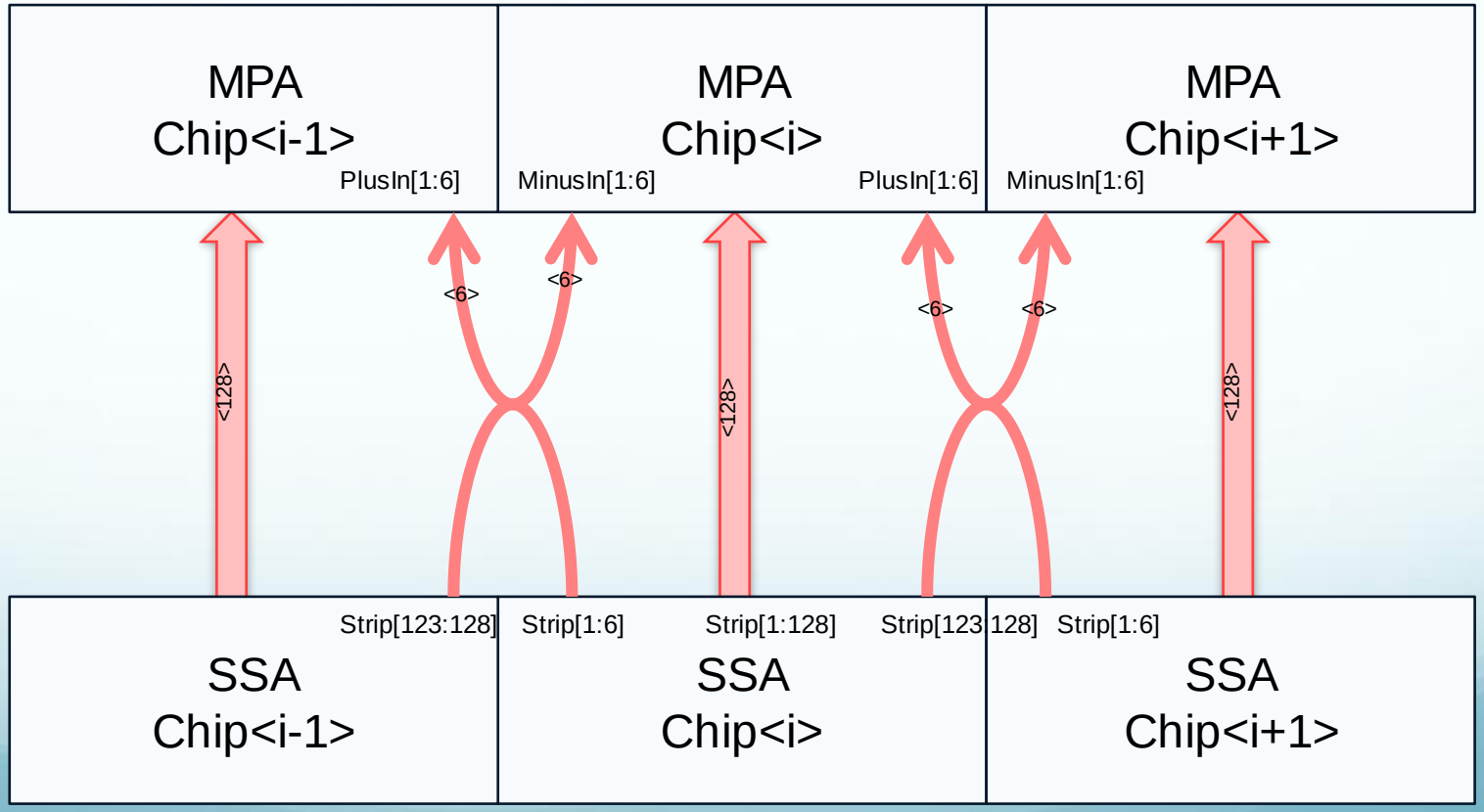
Chip-to-chip connectivity mapping

- 3 channels for clusters across chip edges

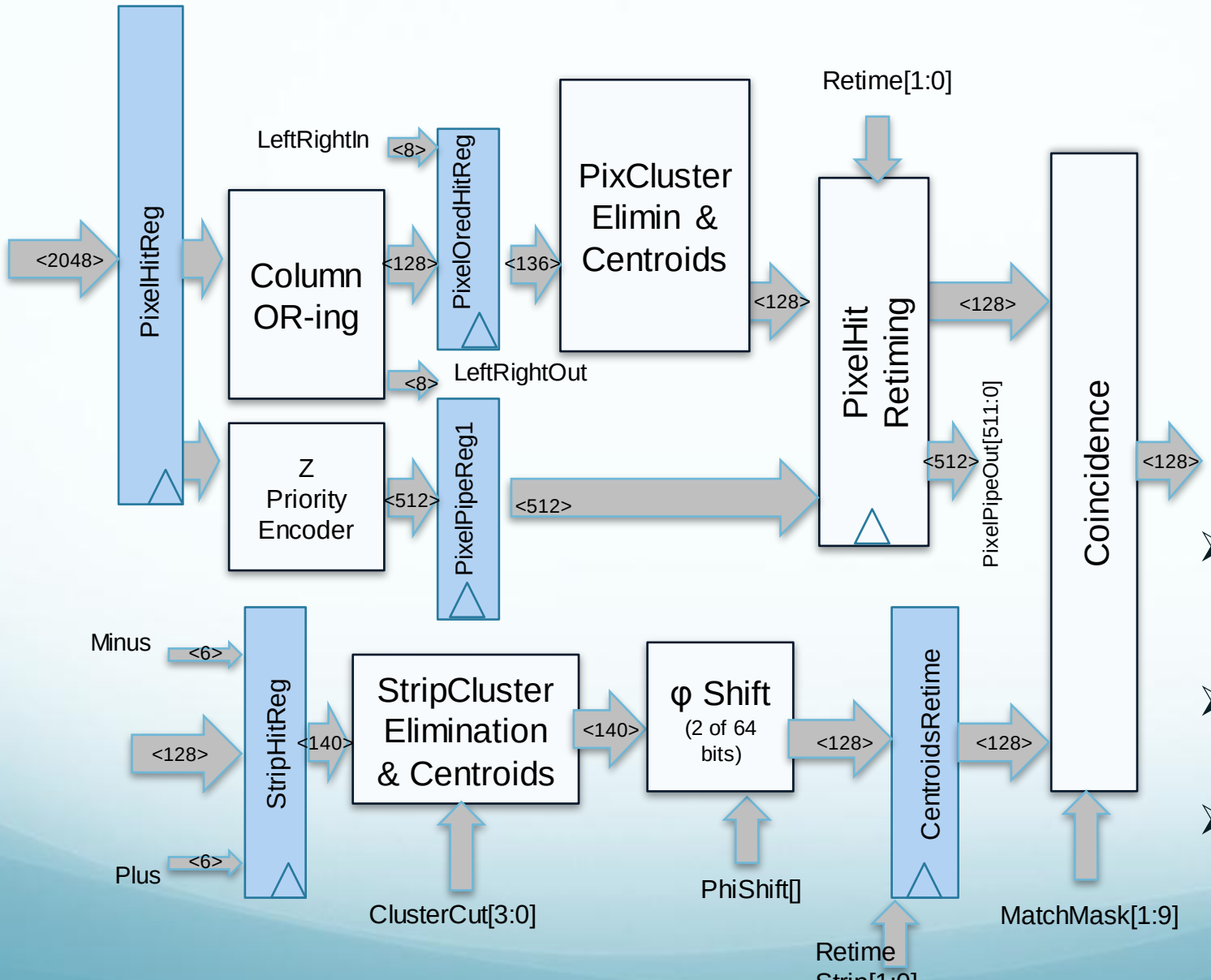


Strips to pixel connectivity mapping

- 6 channels for stubs across chip edges



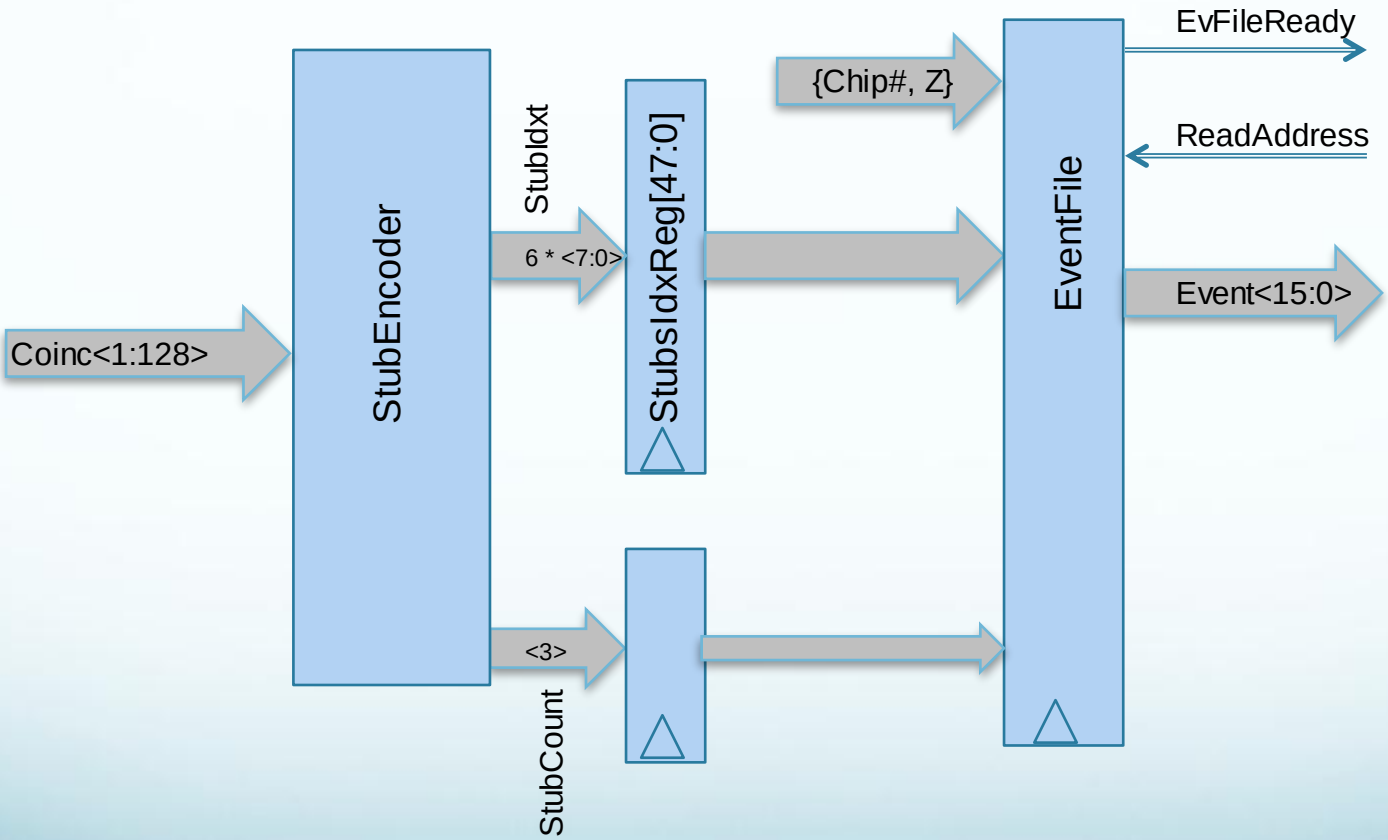
Trigger (coincidence) generation



- Pixel column OR-ed for φ coincidence
- Wide clusters rejected
- Programmable φ shift

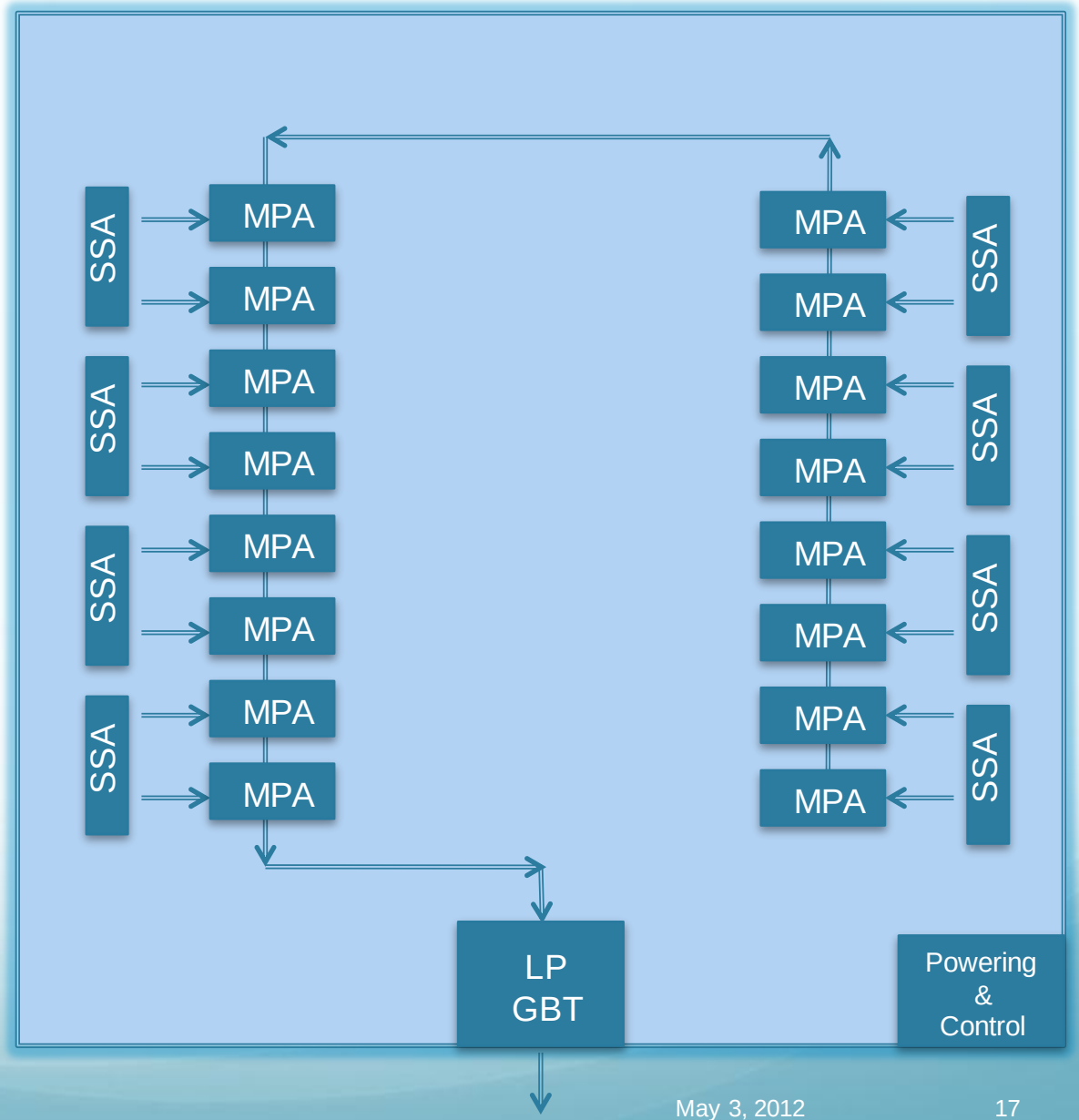
Event Formatting

- N of stubs and addresses
  - Maximum 6



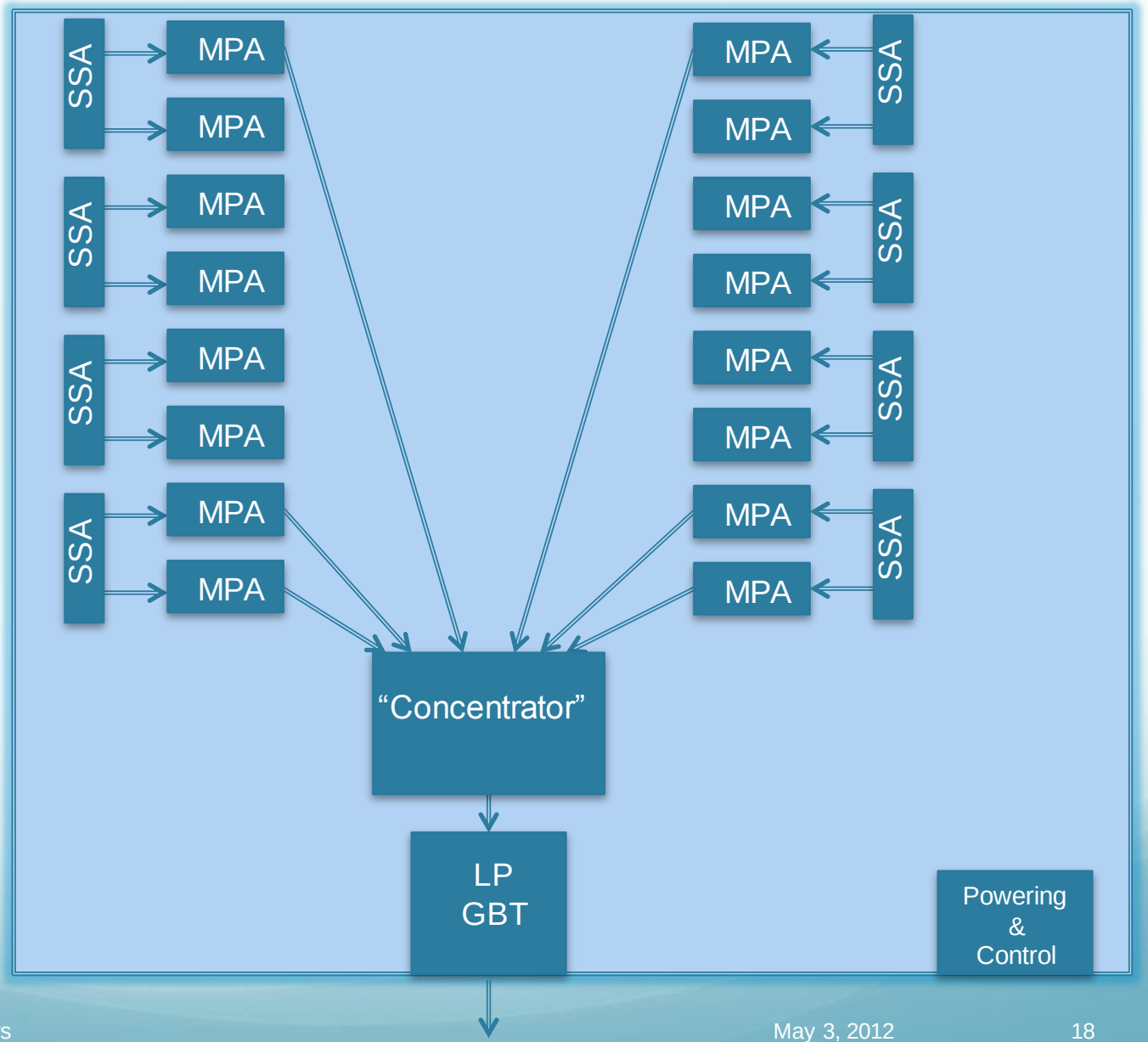
Module Read Out Architecture

- Option 1: ring-like architecture
  - Less lines
  - Efficient use of bandwidth



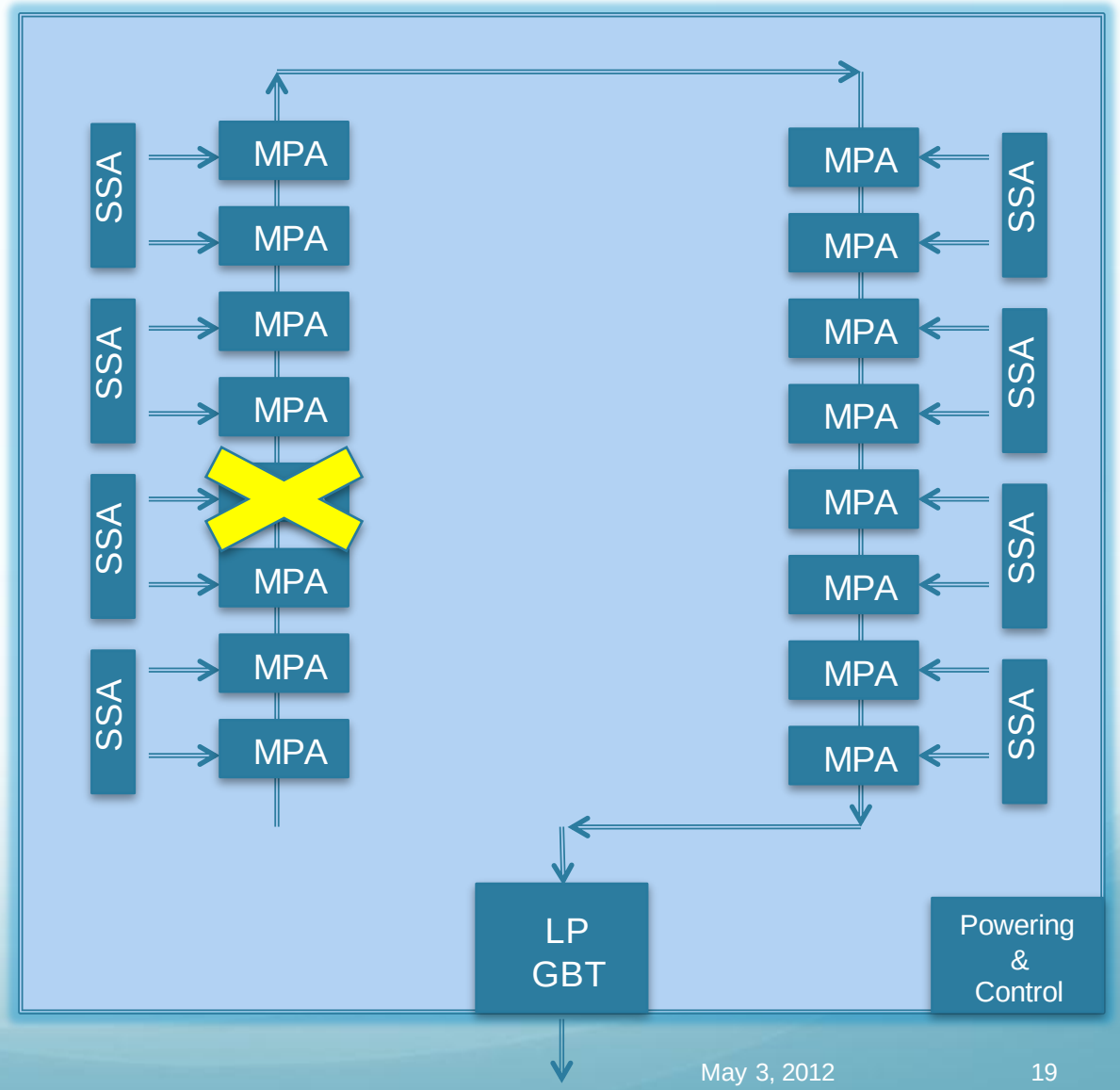
Module Read Out Architecture

- Option 2: star-like architecture
  - Intrinsically robust
  - Conceptually simple
  - More lines

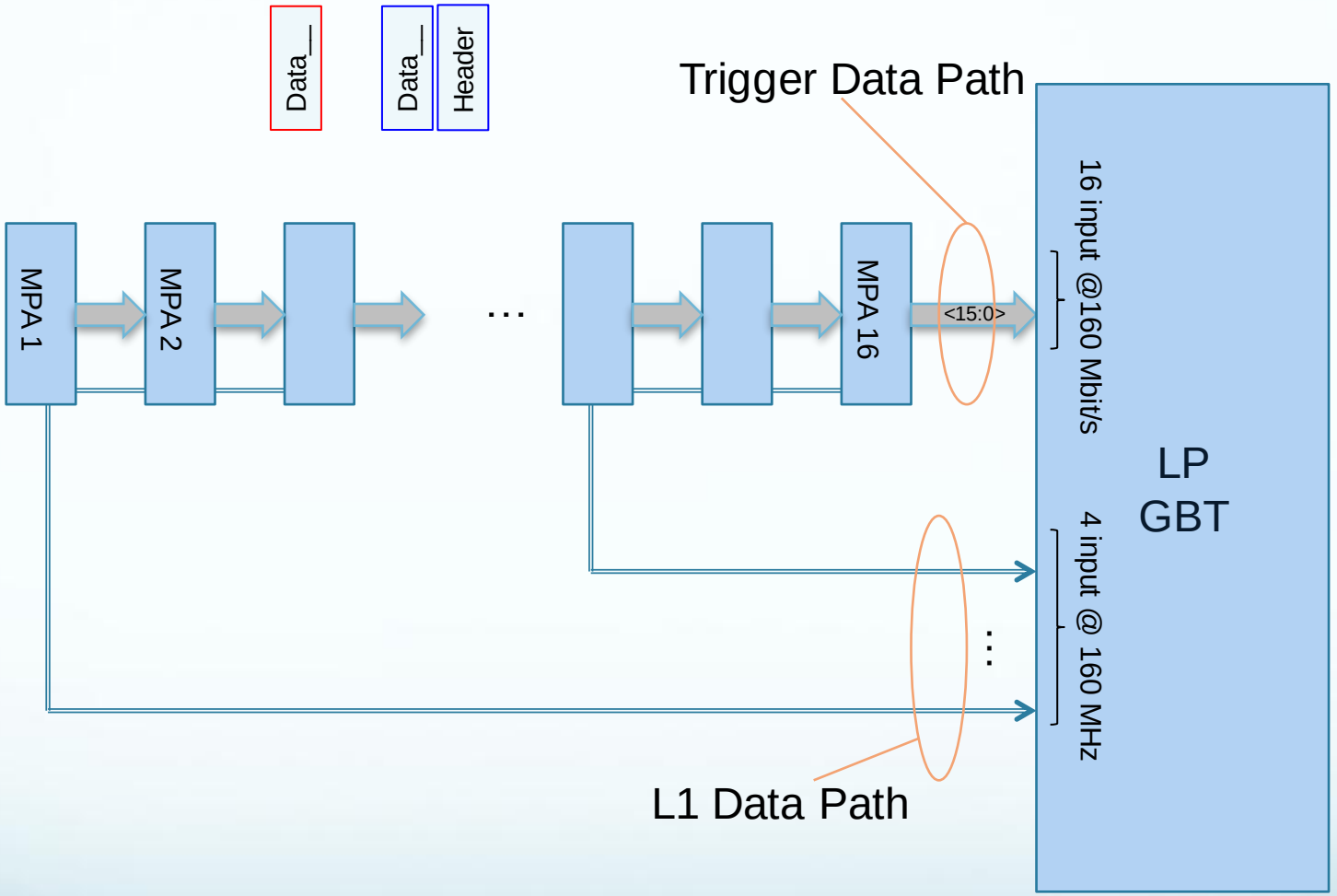


Data Collection with Redundancy

- Recover robustness by inverting data flow



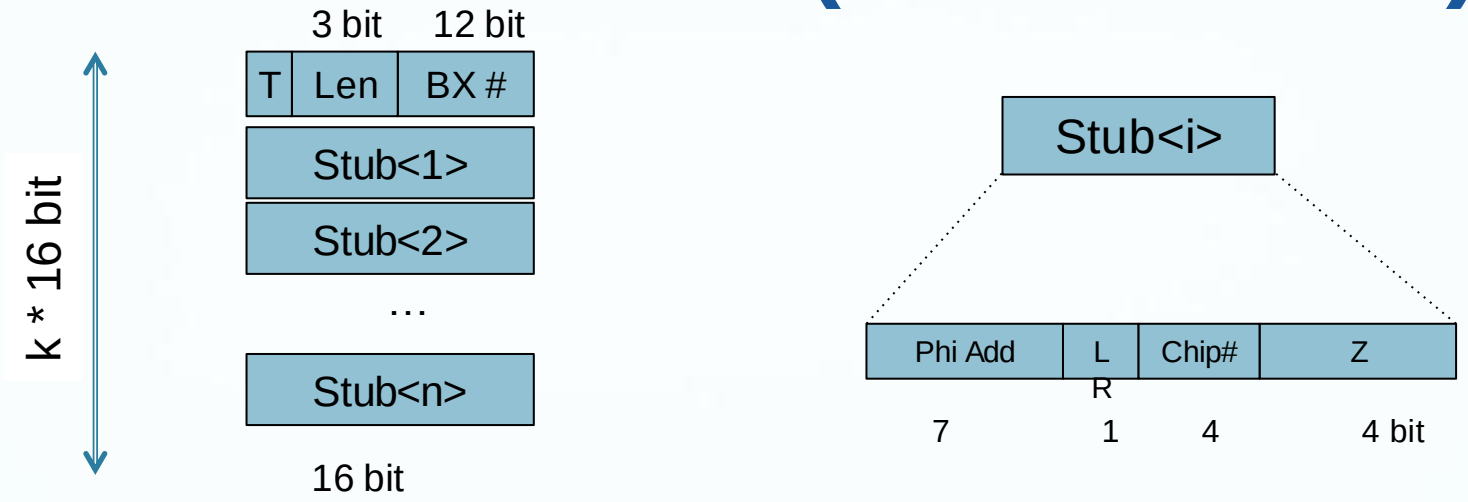
Data Collection on module



- Separate inputs for “trigger” and “readout”

LP-GBT available BW:
20 bits @ 160 Mbit/s

Event Format (first version)



- Header
  - T bit indicates truncation to 7 stubs
  - Len: 3 bit event (i.e. # of stubs) length
  - BX: 12 bit bunch crossing #
- Stub
  - 7 bit phi address
  - 4 bit Z coordinate (each MPA has 4, two MPA in Z per module)
  - 4 bit chip #
  - 1 bit free
- k max is 8 (1 header + 7 stubs), avg 3 stubs every 25 ns
- N.B. Bending magnitude not yet included!

PS Module Power estimates

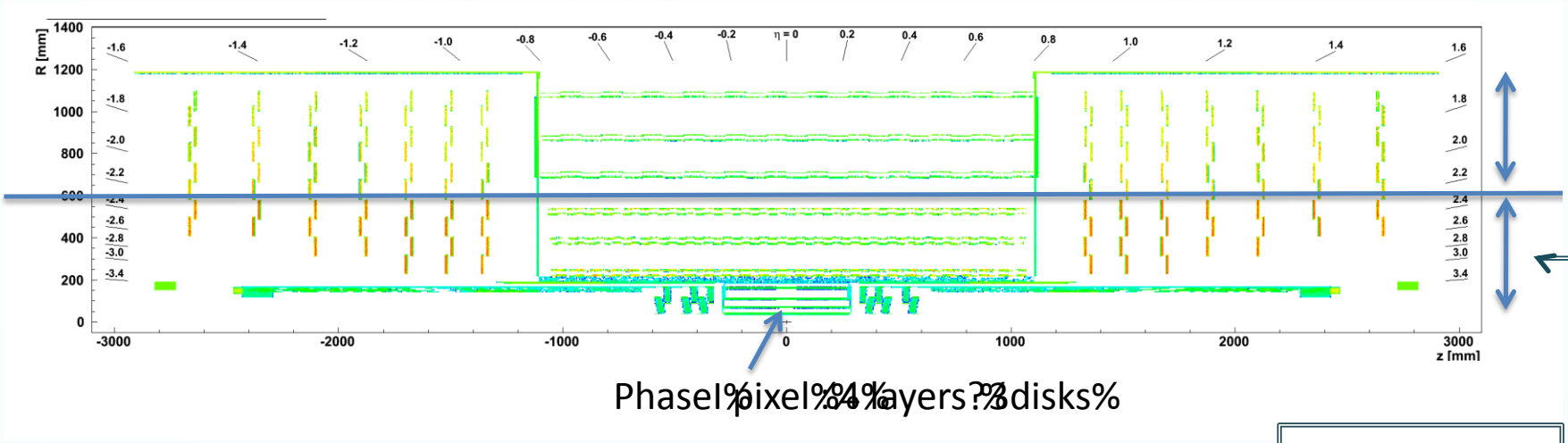
- The pixel front-end is the driver

	# elements	Pwr/element[mW]	Power [mW]
Pixel	2048 * 16	< 0.080	2,620
Strips	256 * 8	0.250	512
Trigger Logic @ 160MHz with α = 1%	10^6 * 16 * 160	0.000015	384
LP-GBT	1	500	500
DC-DC [η = 85%]	1	600	600
Total			**~4,600**

Summary of functionalities

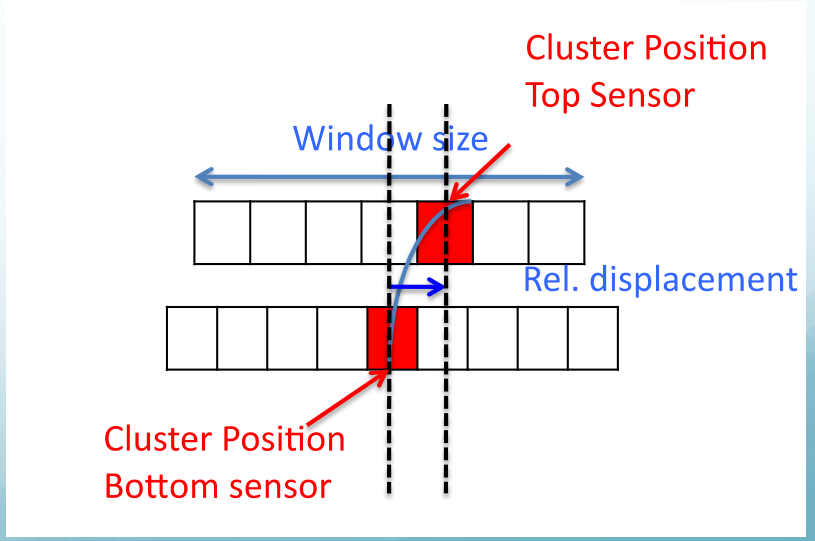
- Clock and resync generation (based on bunch structure)
- Lateral extension to neighbor MPAs and SSAs
- MPA to SSA retiming
- Cluster centroid calculation (approximated to left for even cluster)
- Phi re-alignement
- Coincidence Pixel-Strip finding
- L1 Event buffer for both pixels and strips in MPA
- Stub position encoding (limited to 6 per MPA)
- Event building in ring configuration
- Bus output to LP-GBT
- Not yet implemented:
  - Sign and magnitude of bending in stub

Performance in simulation



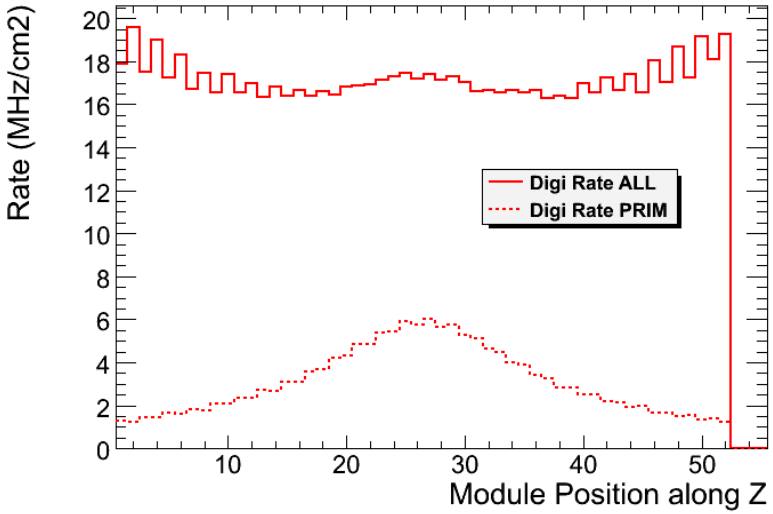
Digitizer, clusterizer, "stub maker"

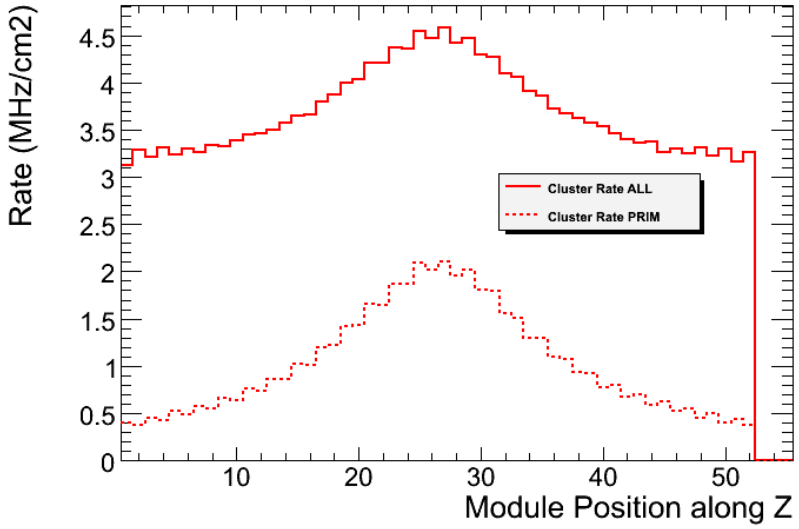
- Meant to be realistic
  - ★ To be reviewed
  - ★ All results "fresh and **preliminary**"

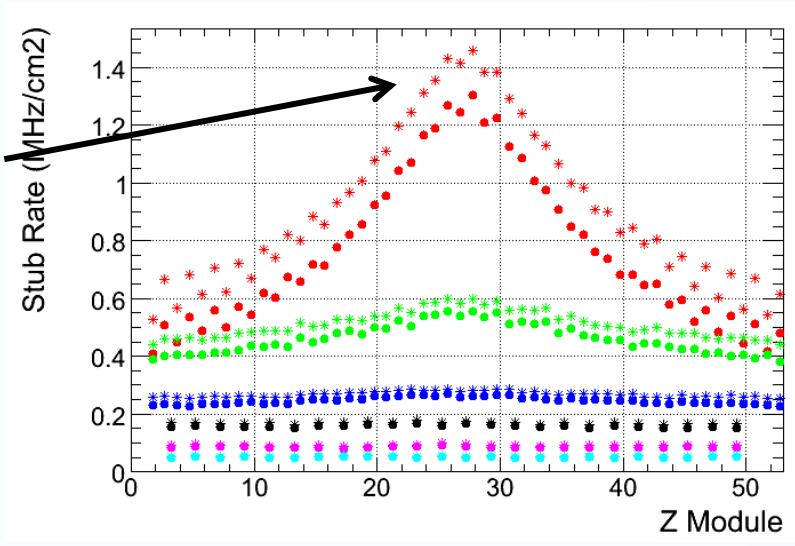


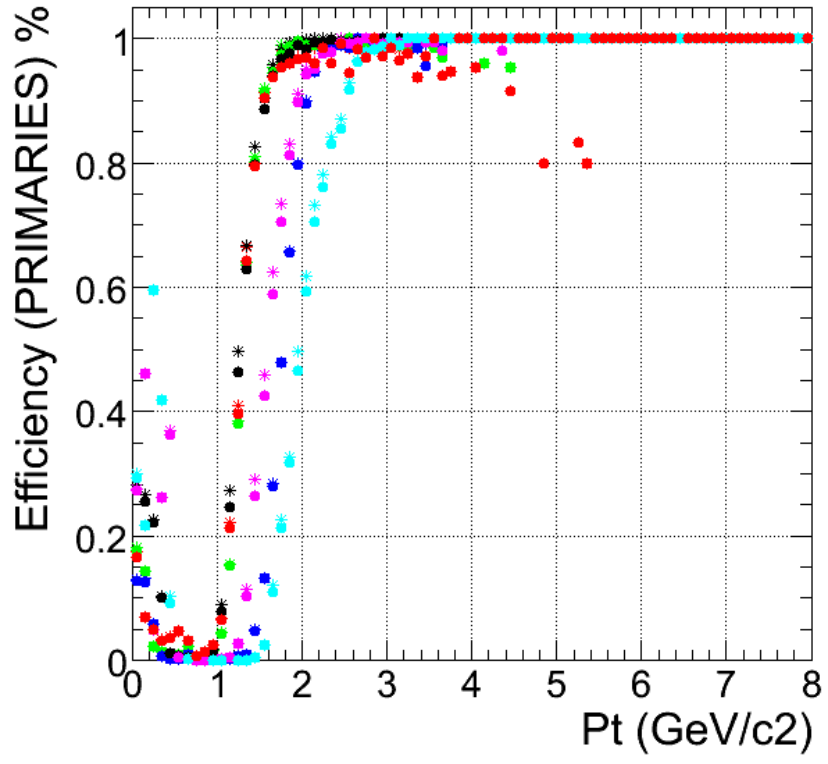
Stub finding

- Barrel layer 1 @ 23 cm, sensor spacing 2.6 mm





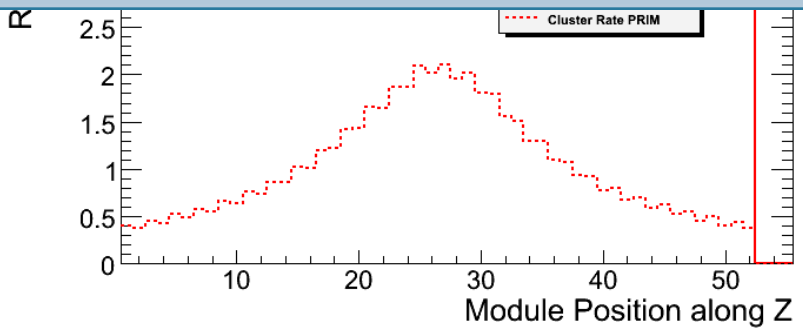


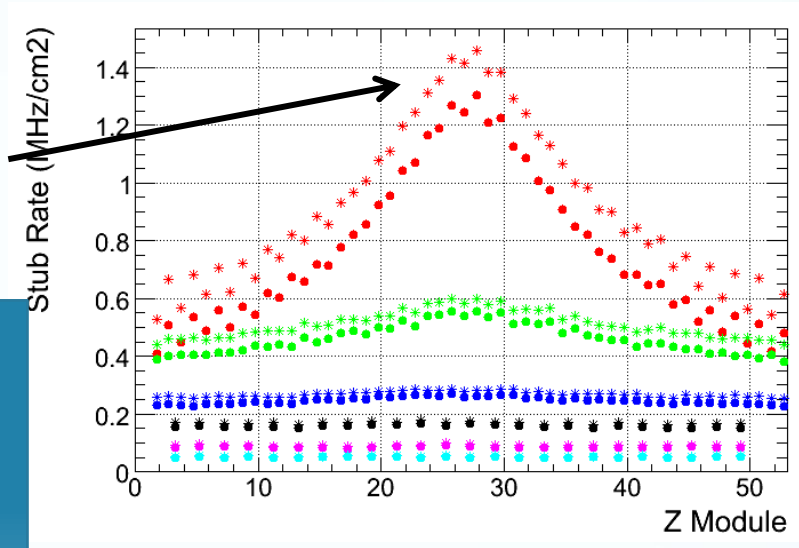


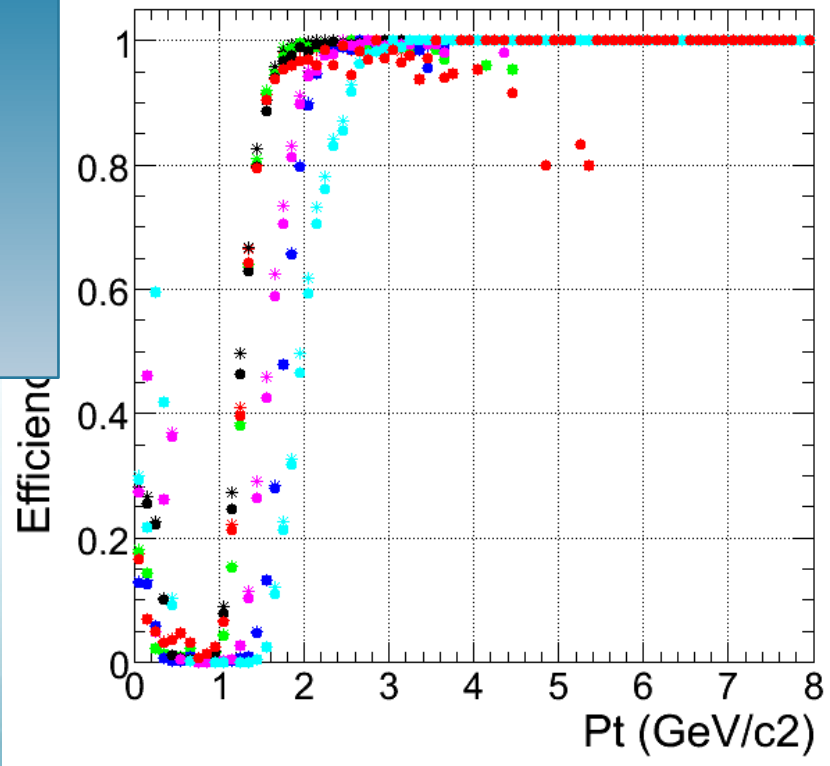
Stub finding

- Barrel layer 1 @ 23 cm, sensor spacing 2.6 mm

- Good performance for p_T > 2 GeV
  - This was the target
- Estimated average stub rate in worst case ~ 1.5 / module / 25 ns
  - Cfr peak:
    - 6 / chip
    - 7 / module
  - Average:
    - 3 / module
  - Margin for further improvements!

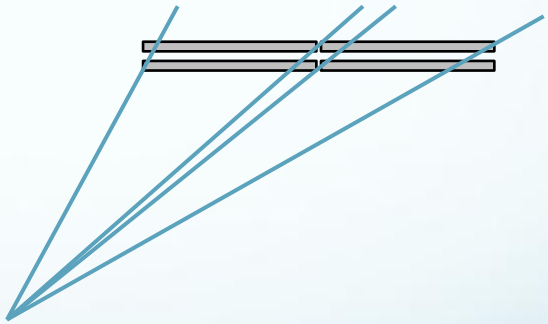






Summary of module features

- "Horizontal" transmission
  - Path for data longer, but not relevant in power budget, driven by pixel chip
  - No interposer. Potentially lighter.
  - Sensors spacing is tunable with nearly no drawback up to ~ 4 mm.
    - Can be used at low radii (down to R $\gtrsim$ 20 cm – but not lower!)
      - Helps for z_0 resolution.
    - Can be used also in endcap.
- Relies on commercial technologies
  - But do they work for our "product"? R&D needed!
- Two halves of the module independent
  - Inefficiency for stub finding in the middle.
    - But can be solved (more later)



- Self-contained building block
  - Includes all auxiliary electronics: the module *is* the system!
- Size limited to ~10×5 cm^2 is part of the concept
  - At least for the time being…

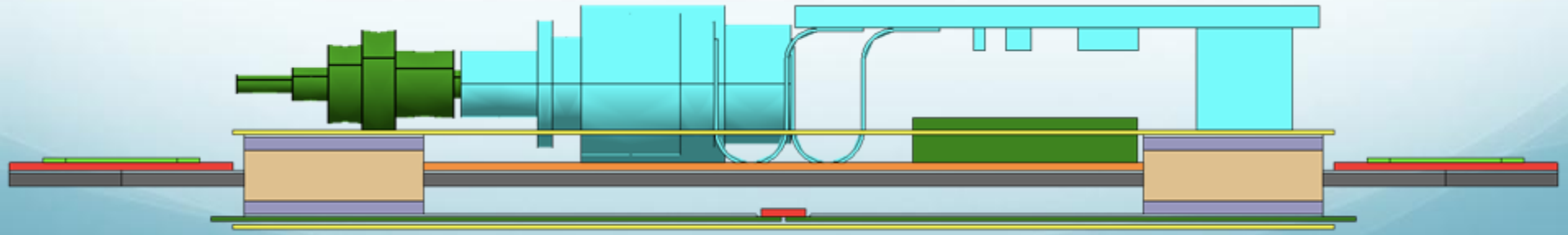
Material estimate

	Mass (g)	X/X0
Sensors	**4.29**	**0.43%**
Hybrids	**2.18**	**0.13%**
Cooling	**3.67**	**0.19%**
ASICs	**2.60**	**0.26%**
Frame	**7.59**	**0.39%**
HV	**0.17**	**0.01%**
Alu	**2.44**	**0.22%**
Power conv	**2.07**	**0.12%**
Connector	**0.29**	**0.02%**
Screws	**0.48**	**0.08%**
Opto	**3.00**	**0.15%**
TOTAL	**28.79**	**1.98%**

- Very preliminary estimates
  - Some conservative, some possibly… not!
- Radiation length normalized to active area
  - I.e. ~ radiation length of a hermetic surface built with these modules
  - Services and support structures to be added!

Further improvements (I)

- Interconnection between module halves
  - R&D on TSVs ongoing
  - Dedicated test chip produced in ¼ µm technology
    - It works!
  - Very encouraging results
    - Despite hiccup due to dummy structures under pads to be etched!
- Eliminate stub finding inefficiency in the middle
  - Can also help to distribute power over the large chip surface



Further improvements (II)

- Reduce pitch on strip sensor to 50 μm
  - Wirebonding pitch 50 μm on both sides
  - Additional ~500 mW power
    - Not on sensor, no problem for cooling
    - DC-DC converter?
  - Better resolution on Δ(Rφ)
  - From 41 μm to 32μm (25% improvement)
  - Same top-bottom connectivity with ×2 speed
  - Small increase in bandwidth
    - But there is margin, and the data reduction will work better
- Improve p_T discrimination and tracking resolution
- Virtually no impact on module design and mass
  - To be confirmed with detailed studies

Implementation plans

- Technology choice for ASICs: 65 nm CMOS
  - Mature technology with good support
  - Strong technology node that will be available for many more years
    - High yield, accurate simulation models etc…
  - 4× higher density of digital logic wrt 130 nm
    - Helps for the chip perifery
  - Some power saving
- Submit first analogue blocks in late 2012
- Continue simulation/improvement of digital logic
  - And validation with Monte Carlo simulation
- Evolve/optimize module design, following progress of hybrids developments, and TSVs

Summary and conclusions

- Promising concept of pixel-strip module with local p_T discrimination
- Choice of technologies driven by optimization for our specific needs
  - Lightweight assembly, optimization of performance (p_T threshold)
  - Use of commercial technologies, perspectives of high yield
    - ★ This concept is the result of a fairly wide investigation of different options
- Module design compatible with large-volume production, and assembly in a big detector
  - Design details to be optimized for automatic assembly
  - Can be tested and operated as a self-contained block
  - Easy to mount/dismount from the structure
- Several ideas for further improvements under study
- R&D on high-density hybrids (and TSVs) is a key element for the quality of the final design