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Nanosecond Timing Resolution with the APV25

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In an environment with high occupancy and continuous collisions, conventional readout of silicon strip detectors will lead to ambiguities in the time domain. This problem can in principle be minimized by reducing the shaping time, but that approach is limited by the noise penalty.

The APV25 chip, originally developed for the CMS experiment, includes an on-chip switched capacitor filter performing a “deconvolution” on three consecutive samples of the shaped signal in order to narrow down the signal to a single bunch crossing.

Unfortunately, this feature requires clock synchronous beam and thus cannot be used in case of quasi-continuous collisions which will occur in the future Belle II experiment at KEK (Japan). Nonetheless, multiple samples along the shaper output can be processed outside of the APV25 in order to determine both peak amplitude and timing of the sampled signal regardless of the asynchronous relation between particle and sampling, achieving a time resolution of a few nanoseconds. Moreover, the data processing can be performed in real-time using look-up tables in an FPGA. This allows comparing the timing of each hit to the trigger timing and discarding off-time background immediately, saving bandwidth, processing power and storage capacity in the subsequent DAQ.

Apart from the hit time finding, the future readout module for the Belle II Silicon Vertex Detector will also perform pedestal subtraction, common mode correction and zero suppression by FPGA firmware. In addition, the incoming analog data will be conditioned by a digital FIR filter. We will present the concept, existing prototypes, results from several beam tests on various (mostly double-sided) silicon strip detectors and what is under construction for the Belle II experiment.

Author: Dr FRIEDL, Markus (Austrian Academy of Sciences (AT))

Co-authors: Mr IRMLER, Christian (Austrian Academy of Sciences (AT)); STEININGER, Helmut (Austrian Academy of Sciences (AT))

Presenter: Dr FRIEDL, Markus (Austrian Academy of Sciences (AT))

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