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Instrumentation of a track trigger with double buffer front-end architecture

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The planned high luminosity upgrade for the LHC (SLHC), will increase the collision rate in the ATLAS detector by approximately a factor 5 beyond the present LHC design goal, while also increasing the number of pile-up collisions in each event by a similar factor. This means that
the level-1 trigger must achieve a higher rejection factor in a more difficult environment. We describe a possible design which splits the level-1 trigger into a two-level system, where the first level, using only calorimetry and muon chambers, defines regions of interest in the tracker
from which to extract information for a second, refined trigger. The use of a two-buffer front-end architecture will allow a significantly longer decision time to move data off the detector keeping the data bandwidth and buffer sizes moderate. We will describe the implementation of the scheme in the ATLAS tracker front-end electronics and the simulated performance of the system. Results on thresholds, rejection, bandwidth and trigger latency will be shown and compared with the present requirements for SLHC upgrade in ATLAS.

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