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3D Vertical Integration Technology for Fast Pattern Recognition

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Hardware-based pattern recognition for fast triggering on particle tracks has been successfully used in high-energy physics experiments for some time. The CDF Silicon Vertex Trigger (SVT) at the Fermilab Tevatron is an excellent example. The method used there, developed in the 1990's at Pisa, is based on algorithms that use a massively parallel associative memory architecture to identify patterns efficiently at high speed. However, due to much higher occupancy and event rates at the LHC, and the fact that the LHC detectors have a much larger number of channels in their tracking detectors, there is an enormous challenge in implementing fast pattern recognition for a track trigger, requiring about three orders of magnitude more associative memory patterns than what was implemented in the original CDF SVT. Scaling of current technologies is unlikely to satisfy the scientific needs of the future, and investments in transformational new technologies need to be made. As Moore's law is approaching severe limitations, it is expected that 3D Vertical Integration Technology will be the next scaling engine. More importantly, in certain cases, the 3D technology also provides novel design opportunities that are simply not possible in 2D and this is the case for fast pattern recognition, such as the associative memory approach. In this talk, we will present a new concept of using the emerging 3D vertical integration technology to significantly advance the state-of-the-art for fast pattern recognition within and outside HEP. A R&D collaboration based on this concept is being developed and the status of this R&D project as well as the future direction will be presented as well.

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