MCM-D Technology for Silicon Strip Hybrids

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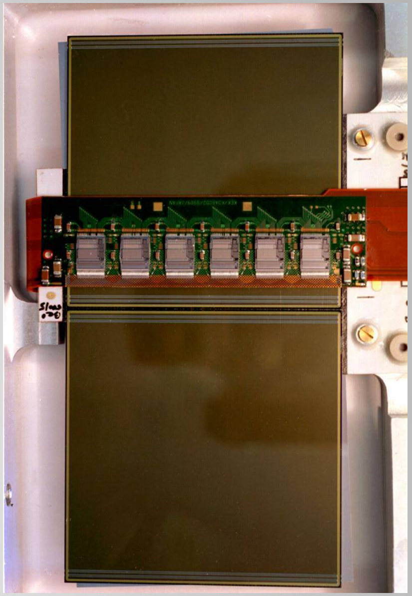
Outline of the Talk

- Introducing the concept
  - Building a hybrid directly on the silicon sensor
- First prototype run
  - Single ground plane on a silicon sensor
  - Electrical measurements
  - Irradiation results
  - CCE & beam test results
- Second prototype run
  - Fully functional hybrid on a blank wafer
  - Production/yield issues
  - Electrical performance
- Conclusions

ISSH: Integrated Silicon Strip Hybrid

- Traditional silicon module build (electrical parts)
  - Sensors, flex circuit, substrate, pitch adaptor, wire bonds, FE-chips, passive components
- A novel approach:
  - Multi-Chip Module – Deposited (MCM-D)
  - Deposit dielectric and metal layers directly on the silicon sensor
  - Layout concepts similar to PCBs
  - All-in-one: Sensor, hybrid, pitch-adaptor and strip connections
- Commercially available technology
  - Semi-industrial partner

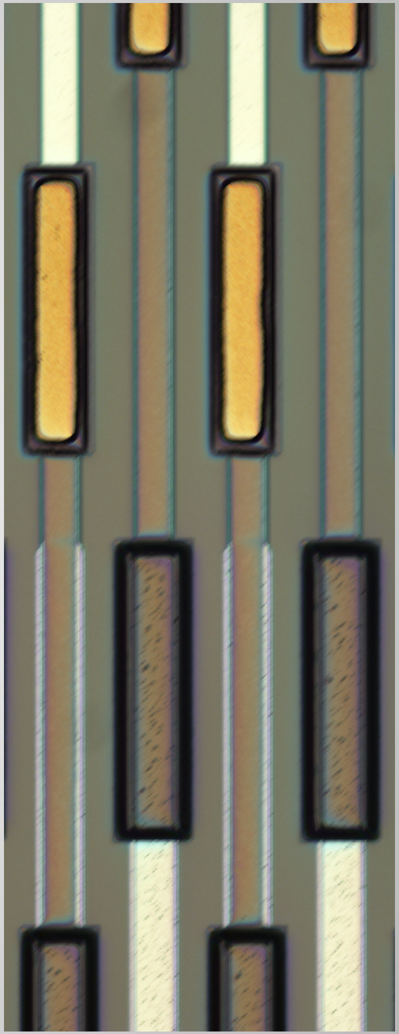


Current ATLAS/SCT module

Acreo *Contract R&D in electronics, optics, and communication technology*

Based in Stockholm and Norrköping, Sweden (http://www.acreo.se/)

Benefits and concerns



Connecting vias to sensor pads

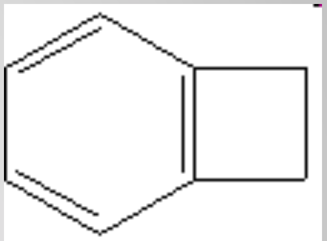
Potential benefits

- Reduced material
  - Thinner layers, no hybrid substrate
- Reduced build complexity
  - Single object from industry
- Increased integration
  - Higher interconnect density
  - Bump bonding of FE chips possible

Points to prove

- Electrical performance
  - Sensor
  - Hybrid (e.g. power distribution)
- Radiation hardness
- Mechanical integrity
- Production yields
- Cost

Technology description – MCM-D on Si wafers



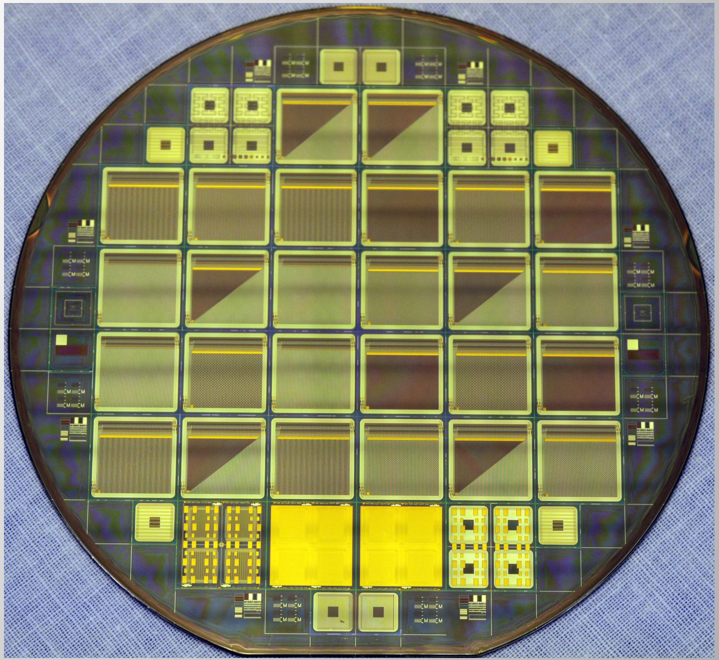
- Dielectric layers: Benzocyclobutene (BCB)
  - Deposited in layers of 3-15 µm thickness
  - Dielectric constant of 2.65
- Conducting layers: sputtered Cu/Ti
  - Standard thickness 1-2 µm
- Connecting vias: etched through BCB before curing
  - To the sensor
  - Between metal layers
- Feature sizes
  - Lithographic resolution: 10 µm
  - Good yield at 30 µm track width/spacing
  - Minimal via size at 15 µm thickness: 65 µm

First prototype run

Single dielectric and metal layer on sensor wafers

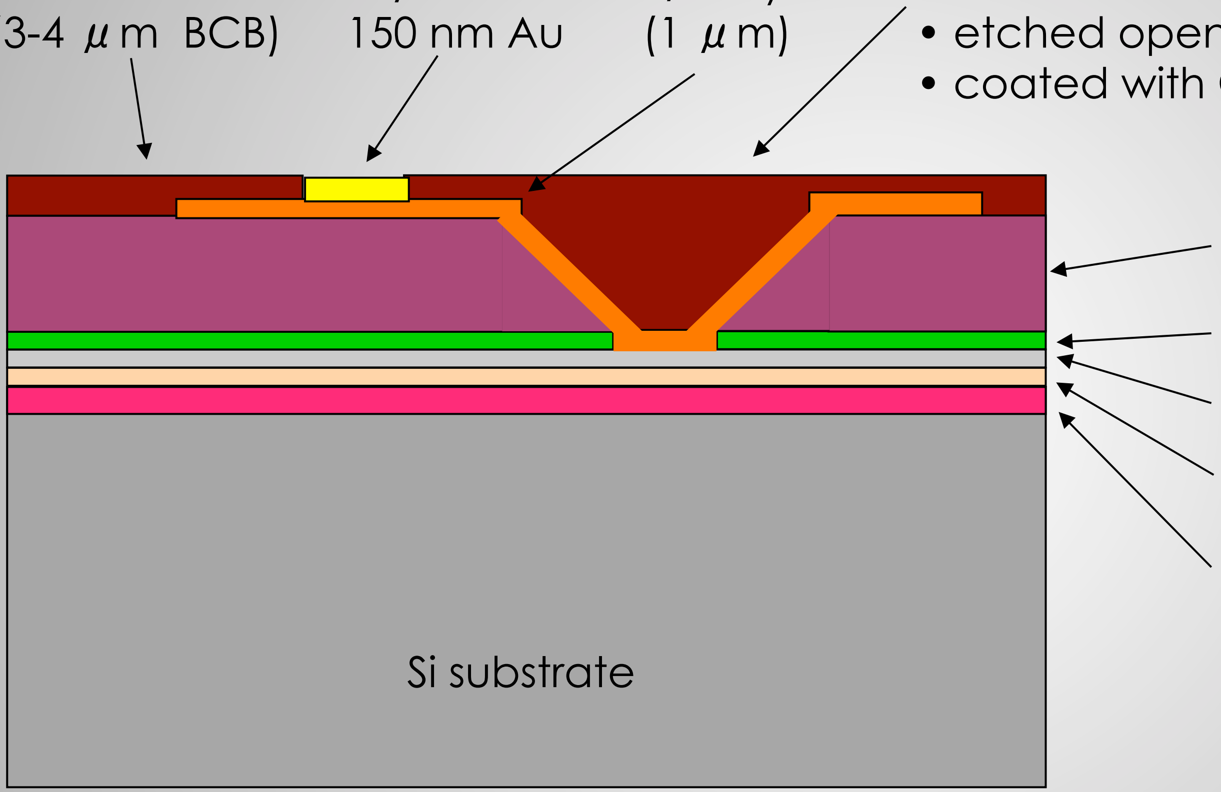
Single Layer Prototypes

- To evaluate the influence on sensor performance
- Single dielectric & metal layer on a sensor wafer
  - First two layers of a hybrid
- 26 mini-sensors per wafer
  - 6 different GNP plane configuration



- No GND plane
- Solid GND plane
- Triangular GND plane
- Meshed GND plane
  - 50% fill, 30 μm line
  - 50% fill, 80 μm line
  - 25% fill, 30 μm line

Cross-section of first prototype



Passivation
(3-4 µm BCB)

4 µm Ni +
150 nm Au

Cu/Ti layer
(1 µm)

Via
- etched opening in BCB (45 °)
- coated with Cu/Ti

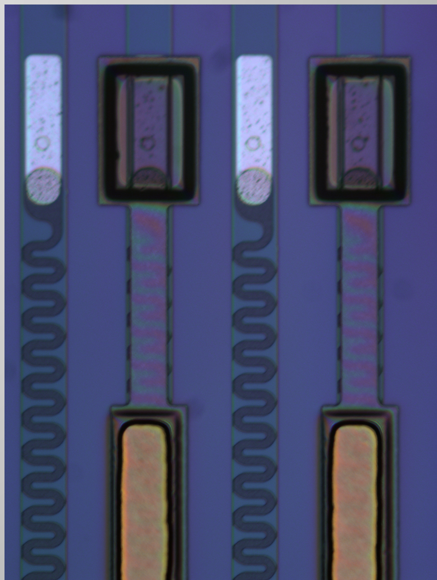
BCB (6 or 12 µm)
(dielectric)

Passivation (SiO_2)

Al strip

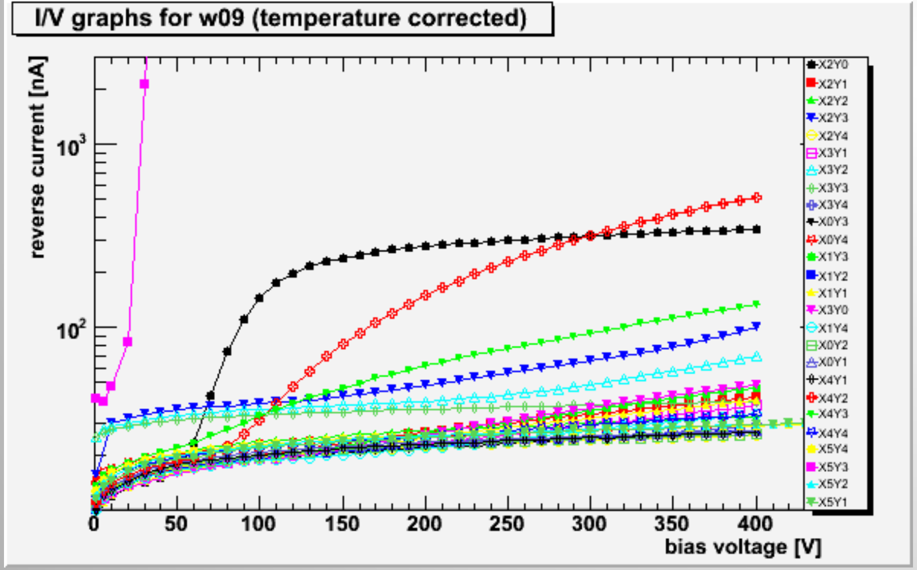
SiO_2

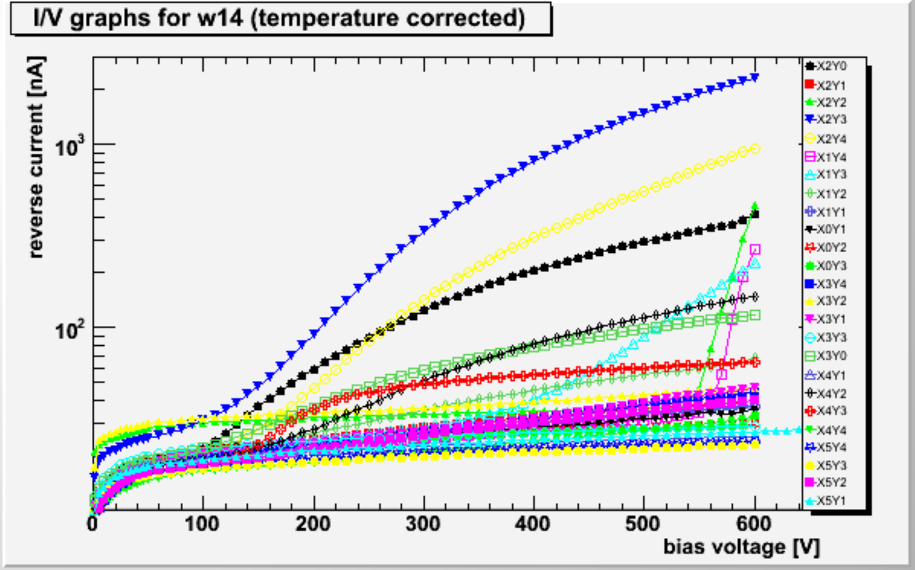
implant



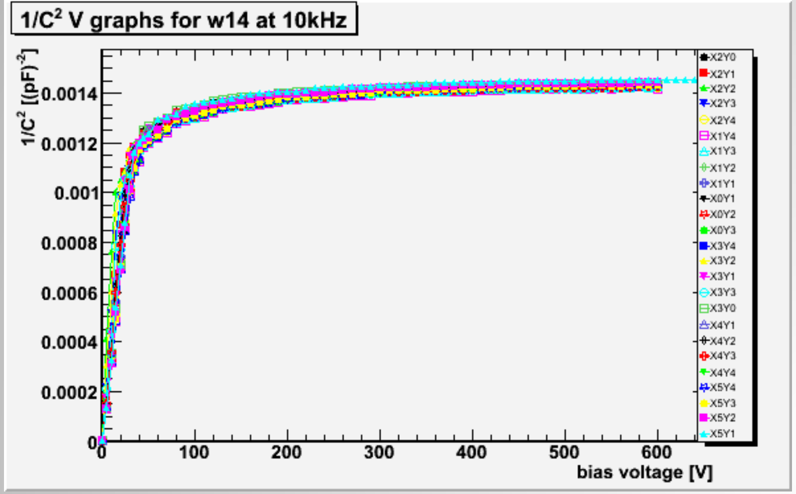
I/V Measurement: pre-irradiation

- 2 x 26 mini-sensors measured
  - 50 have less than 1 μA current @ 400 V

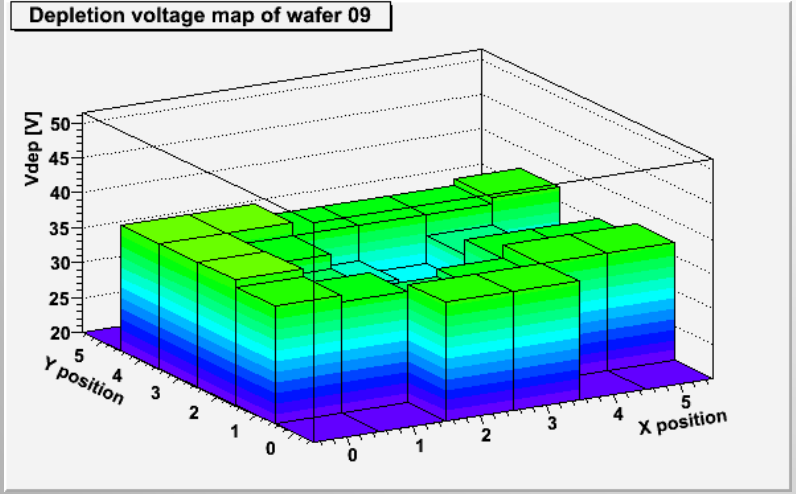


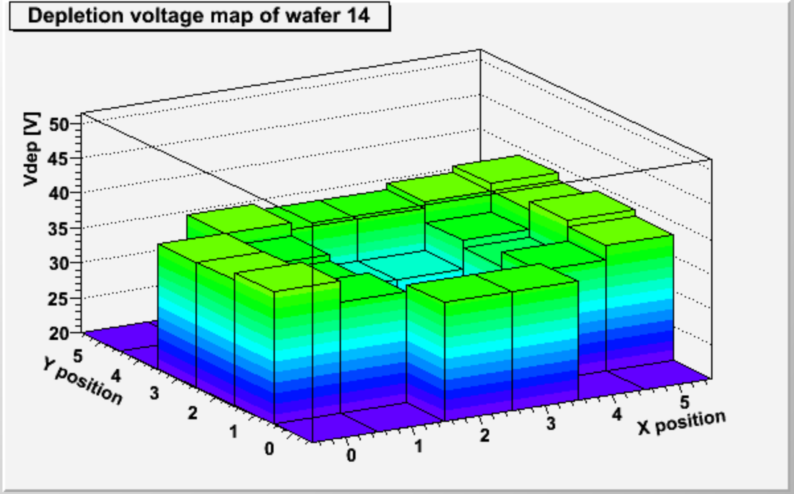


C/V Measurement: pre-irradiation



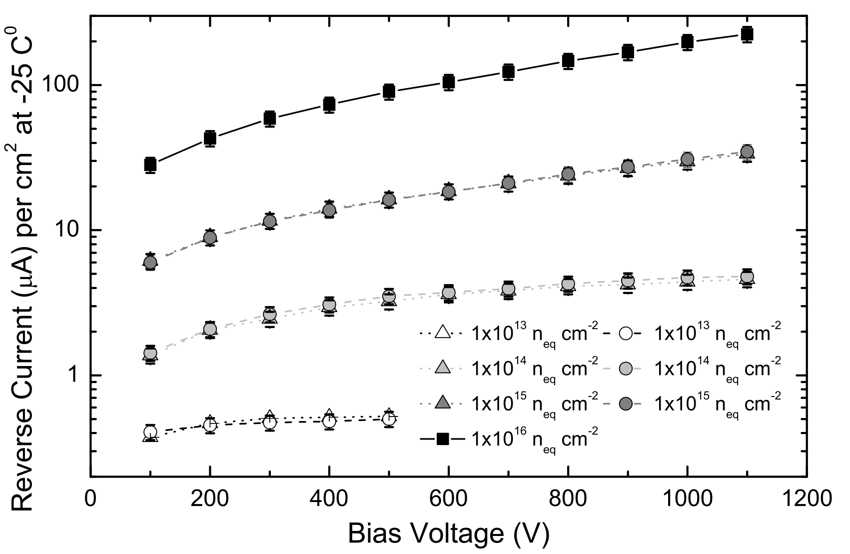
- 50 sensors measured
  - Depletion voltage 30 - 40V

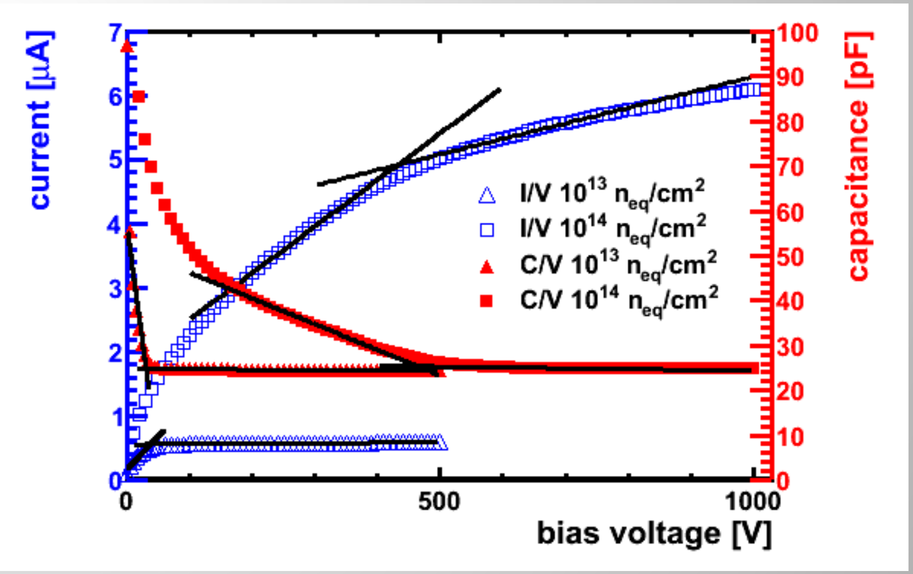




Post-processed sensor irradiations

- Irradiation with 26 MeV protons in Karlsruhe
- Range of sLHC fluences:
  - 10^{13}, 10^{14}, 10^{15} & 10^{16} [1 MeV n_{eq}/cm^2]
  - Corresponding to 1.4 – 1400 MRad dose





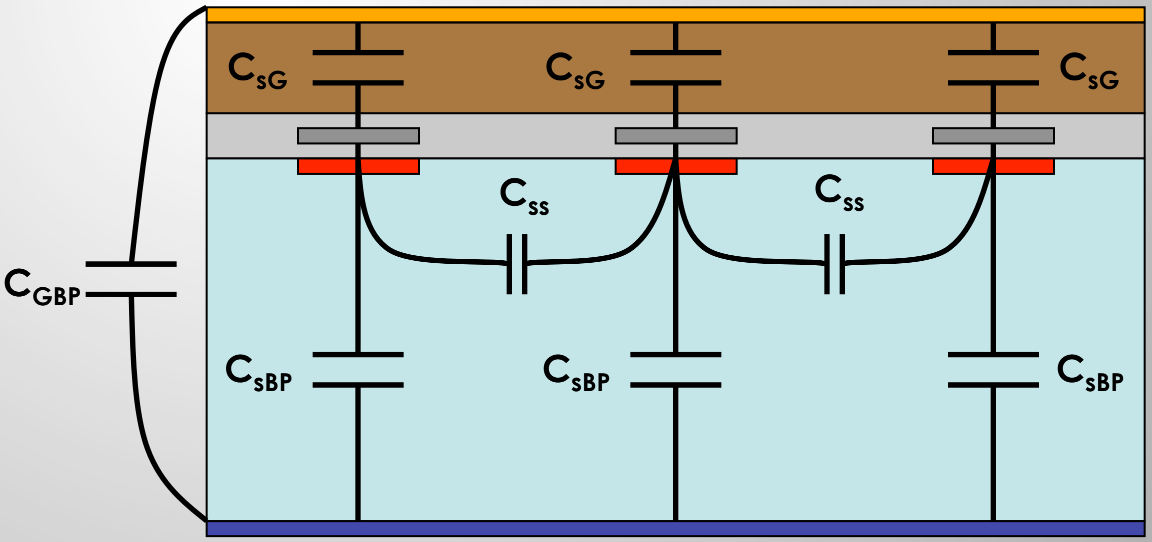
Capacitive Load on the Front-End

Total capacitance of one strip

- Normally dominated by coupling to nearest neighbours
- The GND plane add a new capacitive load
  - $C_{IS} = 2*C_{ss}$ (central strip to two nearest neighbours)
  - C_{sG} measured separately
  - C_{sBP} comes from C/V

$C_{IS} + C_{sG} + C_{sBP}$ is a good estimate of the total capacitance

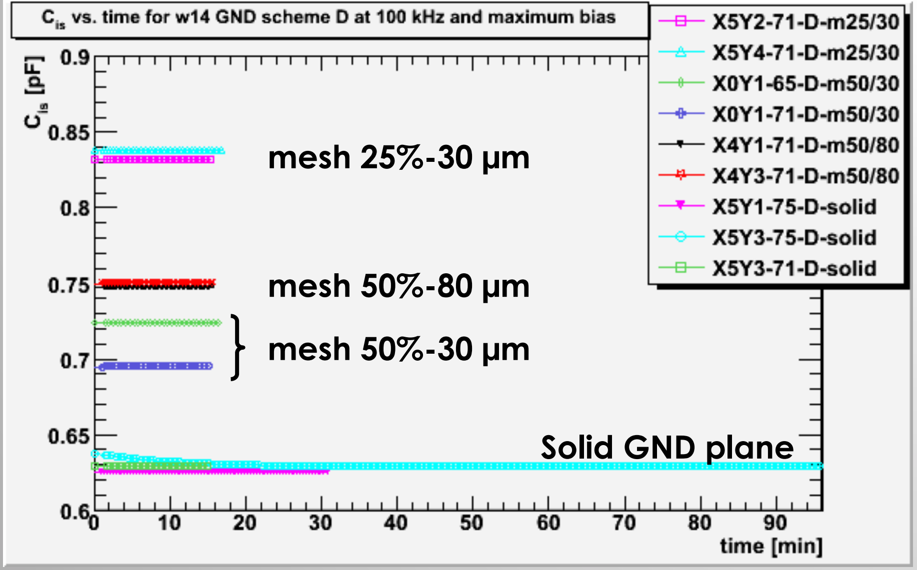
GND plane

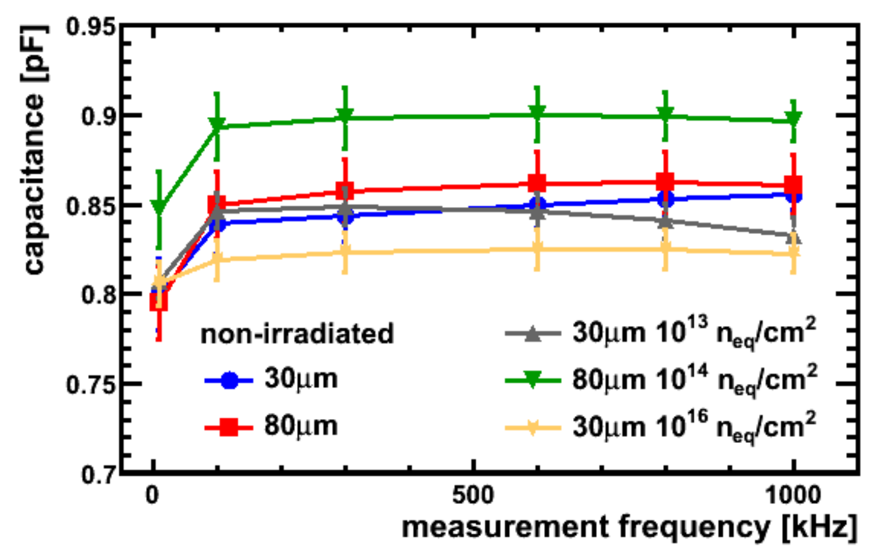


Back-plane

Inter-strip Capacitance

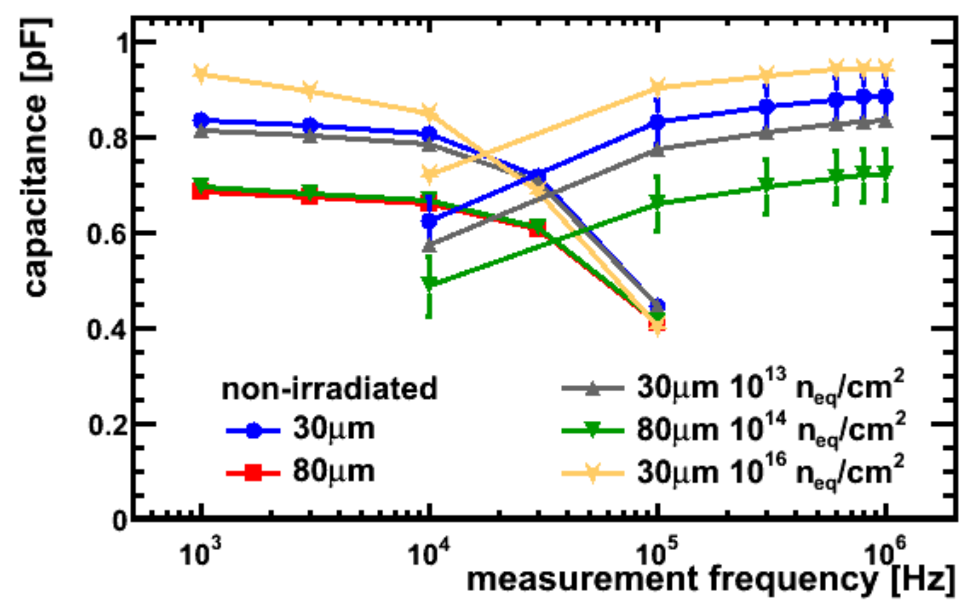
- Depends on the GND plane type (and dielectric thickness)
  - Lower Cis with more solid GND plane
  - Compensation of surface charge
- Unaffected by irradiation





Capacitance to GND plane

- Measured by two different methods
  - Bias rail to GND plane capacitance (low frequency)
  - 3 strips + edge capacitance (high frequency)



Depends on GND plane type

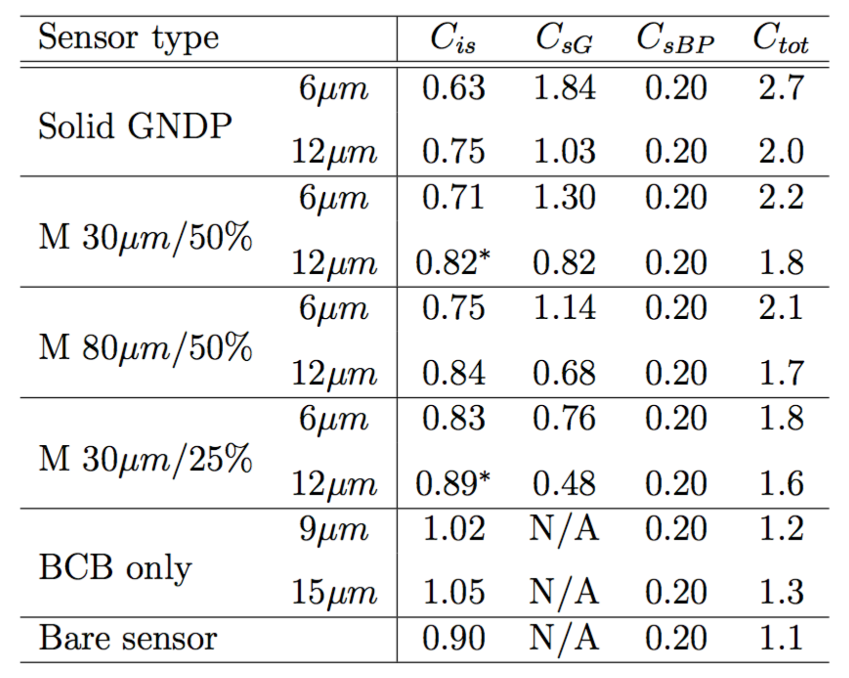
Depends on dielectric thickness

Unaffected by irradiation
- Small increase at 10^{16}?

Summary: Capacitive load on the front-end

- Total strip capacitance depends on the GND plane type and dielectric thickness
- No evidence of increase after irradiation
  - Possibly a modest increase at 10^{16}

Two dielectric thicknesses



Sensor type		C_{is}	C_{sG}	C_{sBP}	C_{tot}
Solid GNDP	$6\mu m$	0.63	1.84	0.20	2.7
	$12\mu m$	0.75	1.03	0.20	2.0
M $30\mu m/50\%$	$6\mu m$	0.71	1.30	0.20	2.2
	$12\mu m$	0.82*	0.82	0.20	1.8
M $80\mu m/50\%$	$6\mu m$	0.75	1.14	0.20	2.1
	$12\mu m$	0.84	0.68	0.20	1.7
M $30\mu m/25\%$	$6\mu m$	0.83	0.76	0.20	1.8
	$12\mu m$	0.89*	0.48	0.20	1.6
BCB only	$9\mu m$	1.02	N/A	0.20	1.2
	$15\mu m$	1.05	N/A	0.20	1.3
Bare sensor		0.90	N/A	0.20	1.1

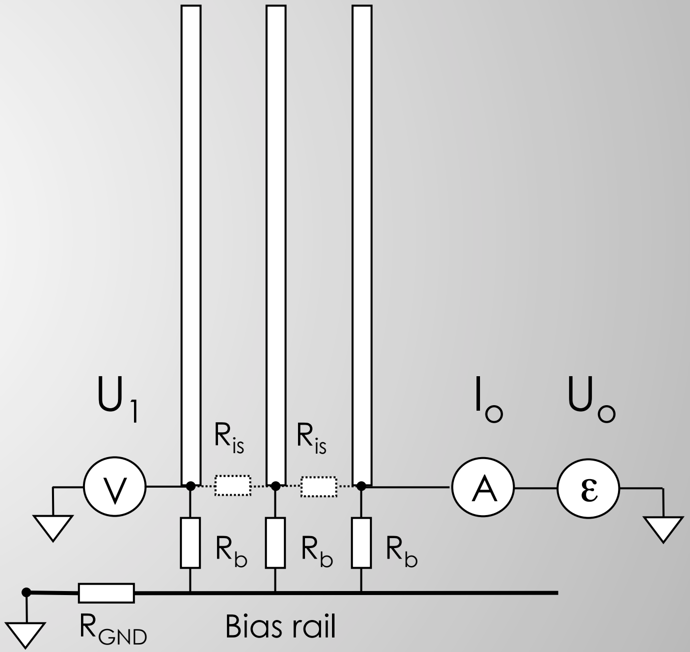
Pre-irradiation values

Load in pF/cm

Inter-strip resistance

- Apply voltage U_0 on one implant
  - Measure current I_0 and induced voltage U_1
- Dominated by stray resistances
  - Measurement gives a lower limit

$$R_{is} << \sqrt{R_b^3 / R_{GND}} \approx 10^9\ \Omega$$

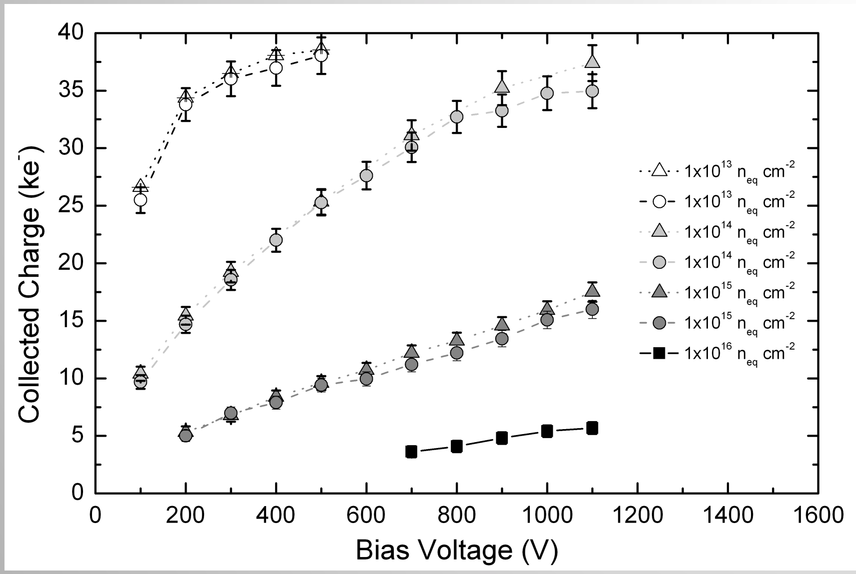


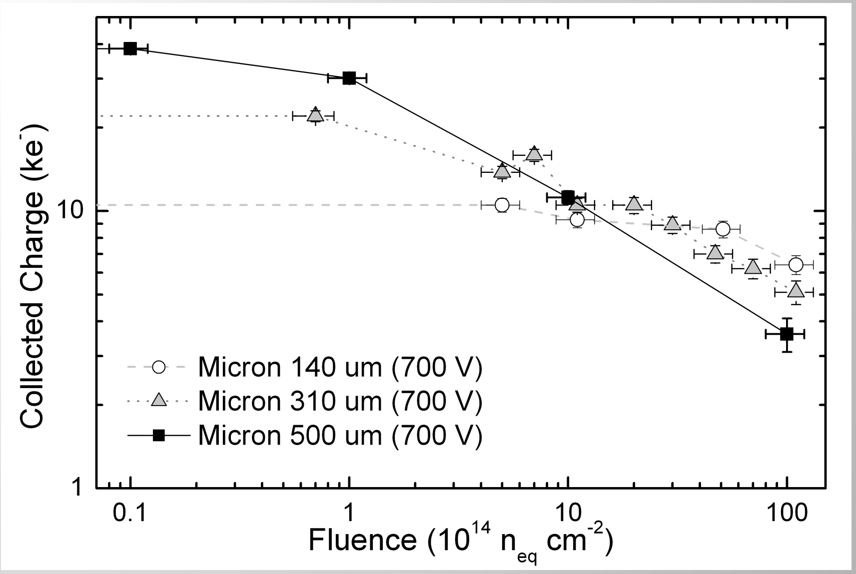
Measured inter-strip resistance sets a limit of $R_{is} > 250\ \mathrm{M}\Omega$

Limit not changed by irradiation

Charge Collection Efficiency (CCE)

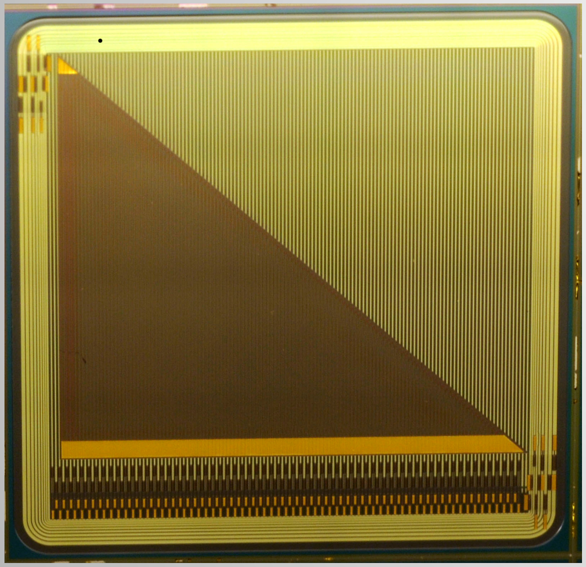
- CCE measured with a β-source vs. bias voltage
  - Using analogue SCT128A chip
- Results as expected for 500 μm thick sensor
  - Compared to non-processed 300 and 140 μm sensors

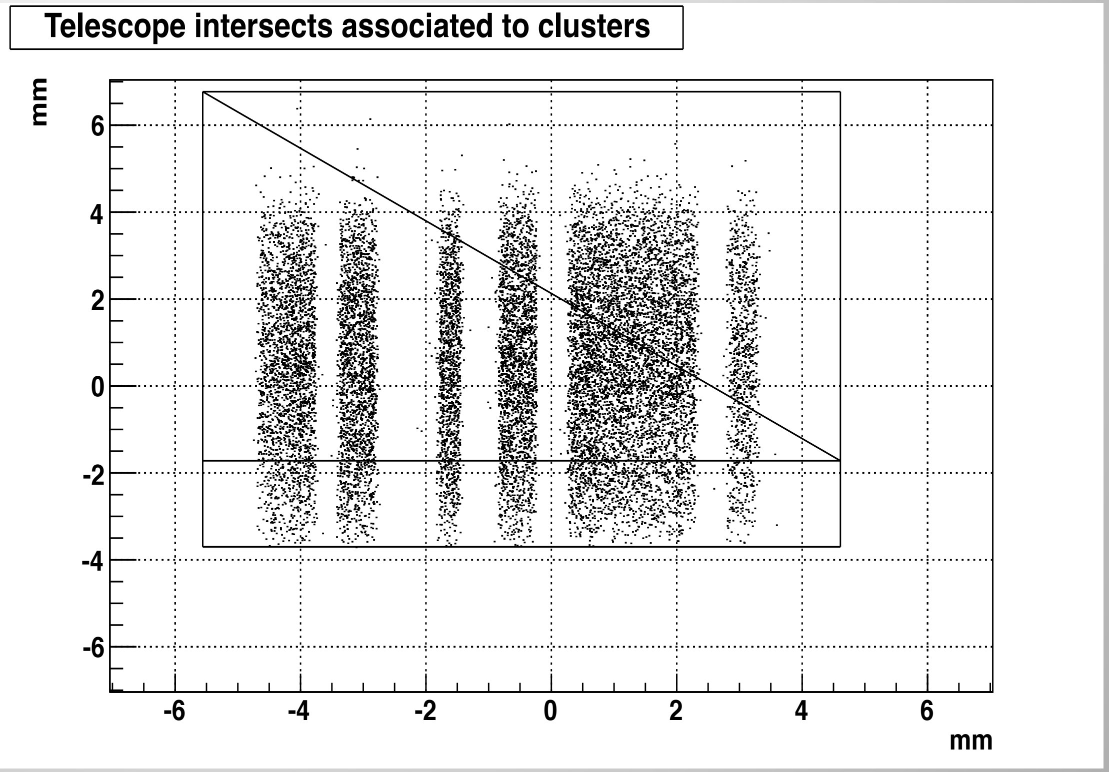




Beam Test: CERN SPS

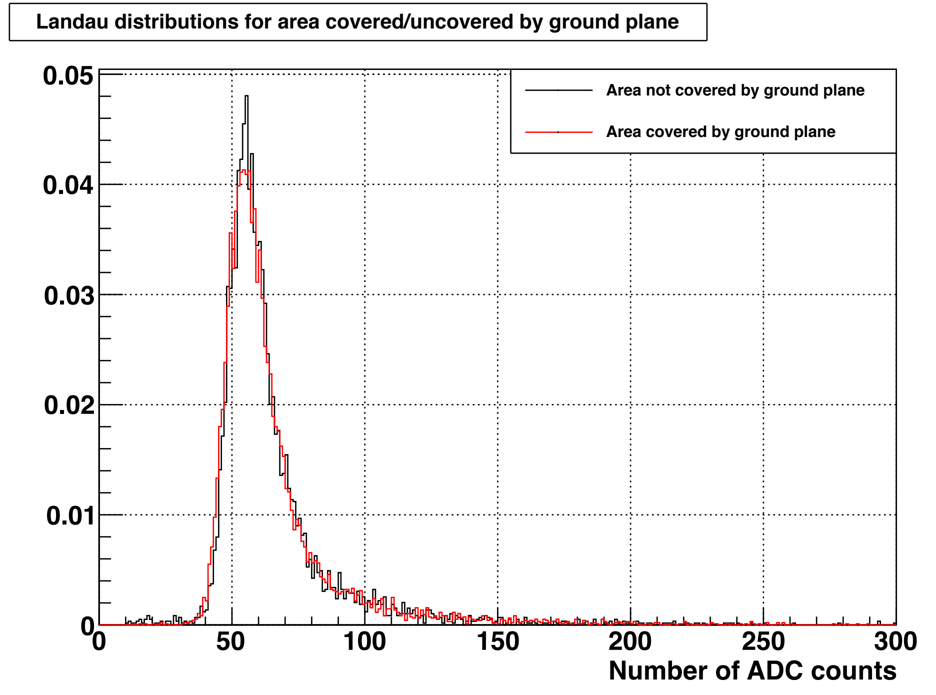
- Using the Timepix telesocpe
- Sensor with triangular GND plane
  - Compare area with and w/o GND plane



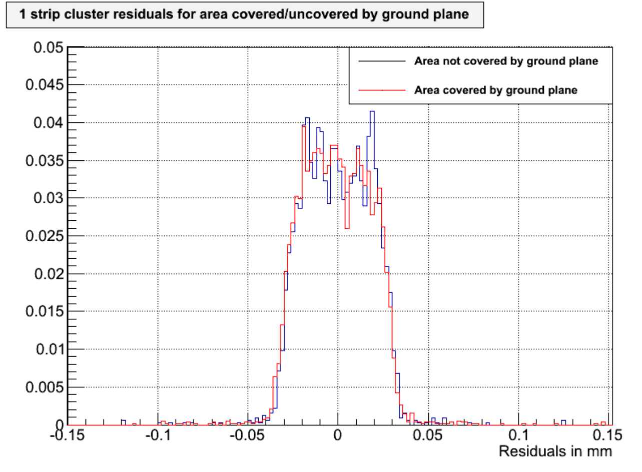


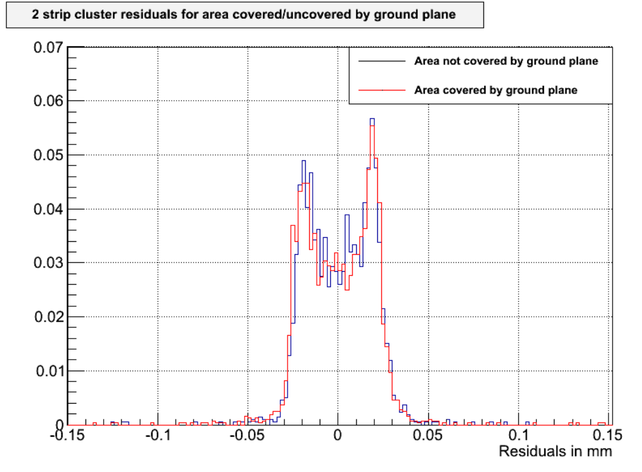
Beam Test – preliminary results

- No difference observed between the two areas
  - Detailed analysis in progress



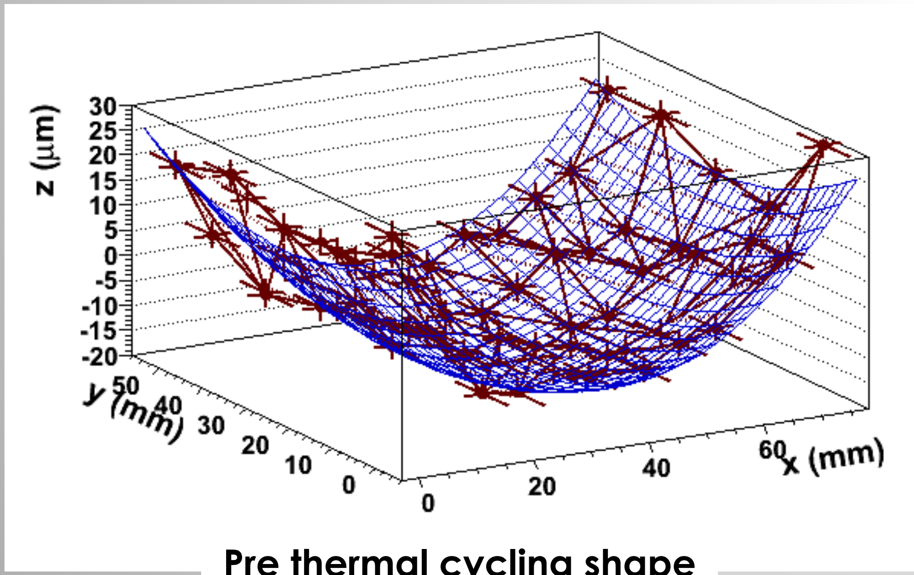
Landau distribution
1 & 2 strip residuals



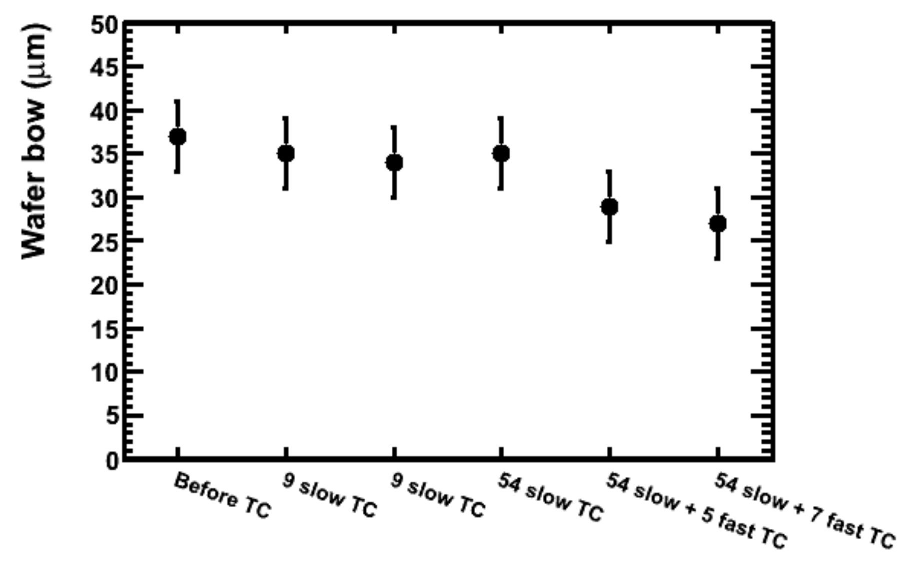


Mechanical Measurements

- Wafer flatness measured, interleaved with
  - 54 thermal cycles **(1-2 °C/min)**
  - 7 thermal chocks **(1 °C/s down, 4 °C up)**
- No sign of de-lamination



Pre thermal cycling shape

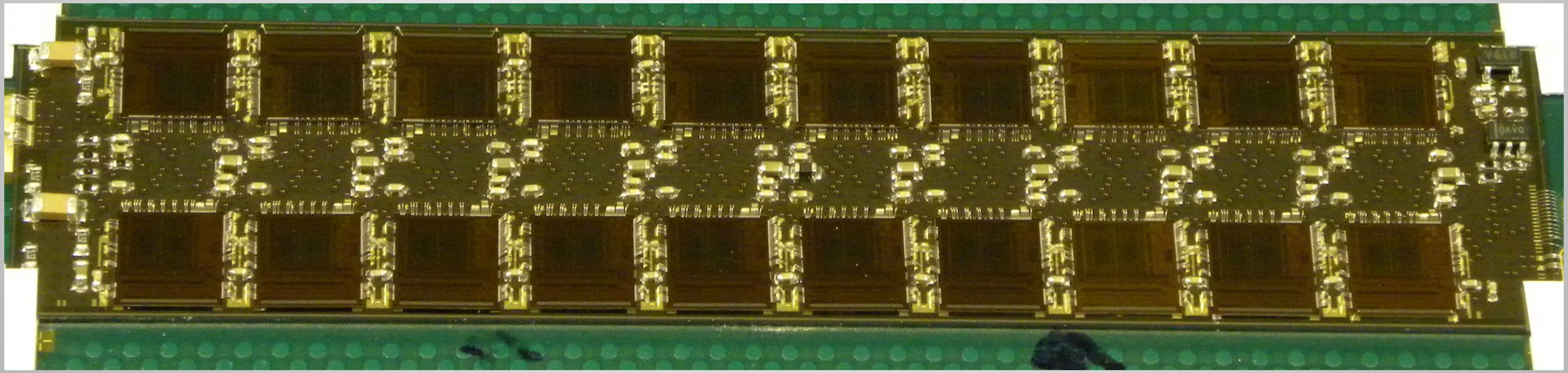


Second Prototype Run

Fully functional front-end hybrid on blank silicon wafers

Fully functional FE hybrid

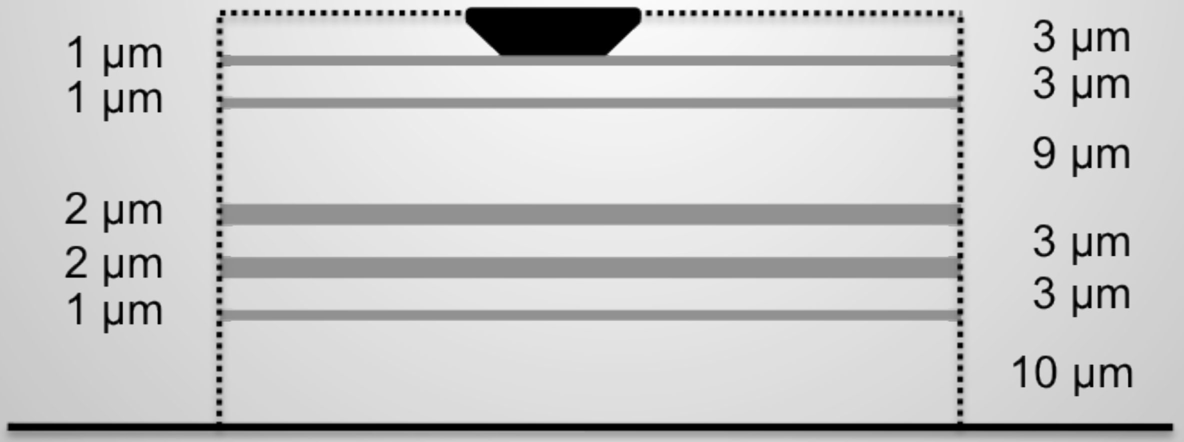
- Design based on Atlas SCT upgrade kapton hybrid
  - Hosts 20 ABCDN chips
  - Layout adjusted to MCM-D design rules
- Processed on blank silicon wafers
  - Design portable to sensor wafers



Layer Stack

- 5 metal layers (11 masks)
  - Shield, GND, VDD, Signal 1, Signal 2
  - Top metallisation for bonding and SMD
- Layer thicknesses carefully considered
  - Performance vs. yield

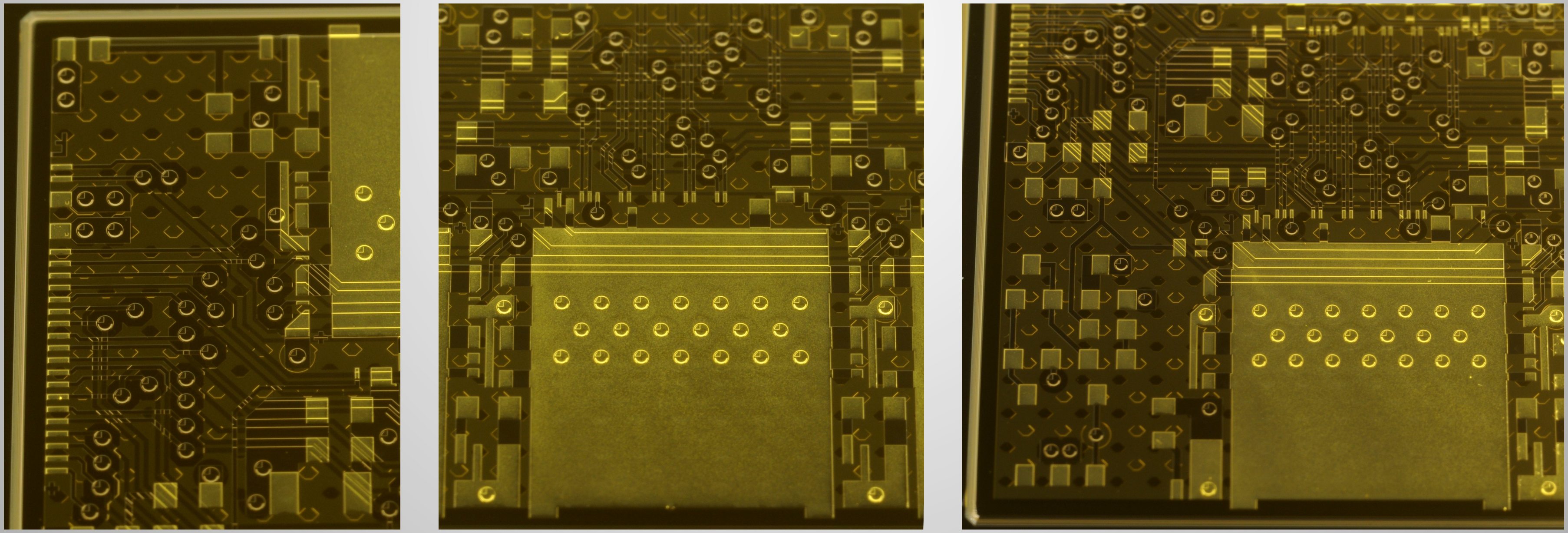
Cu layer thickness



BCB layer thickness (dielectric)

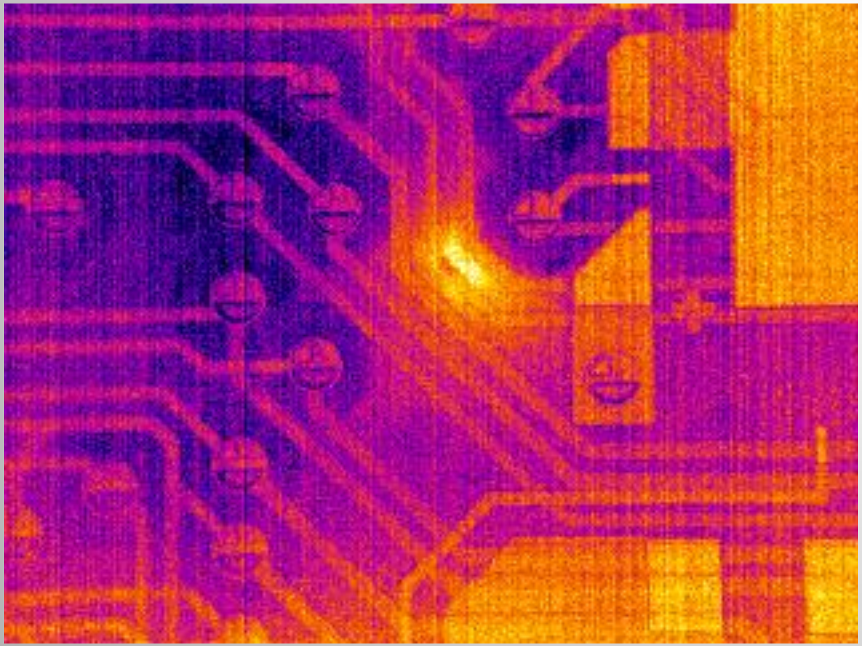
Initial tests & yield

- 4 wafers with 3 hybrids produced
  - OK apart from one common problem (see next slide)
- No de-lamination during production or testing

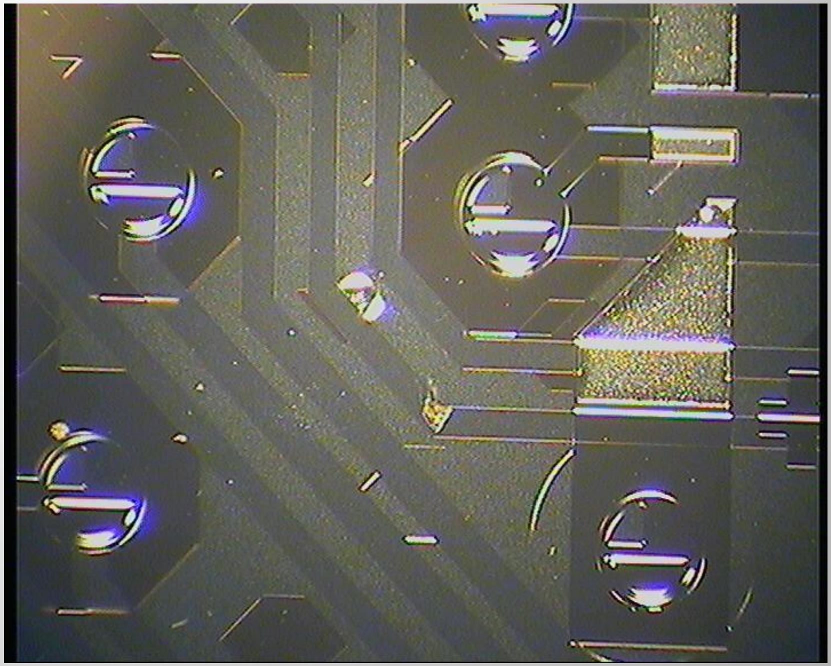


Power plane short

- VDD and GND planes shorted
  - Probably due to local defects
  - Requires process development
- All shorts 'cured': using power supply in CC-mode



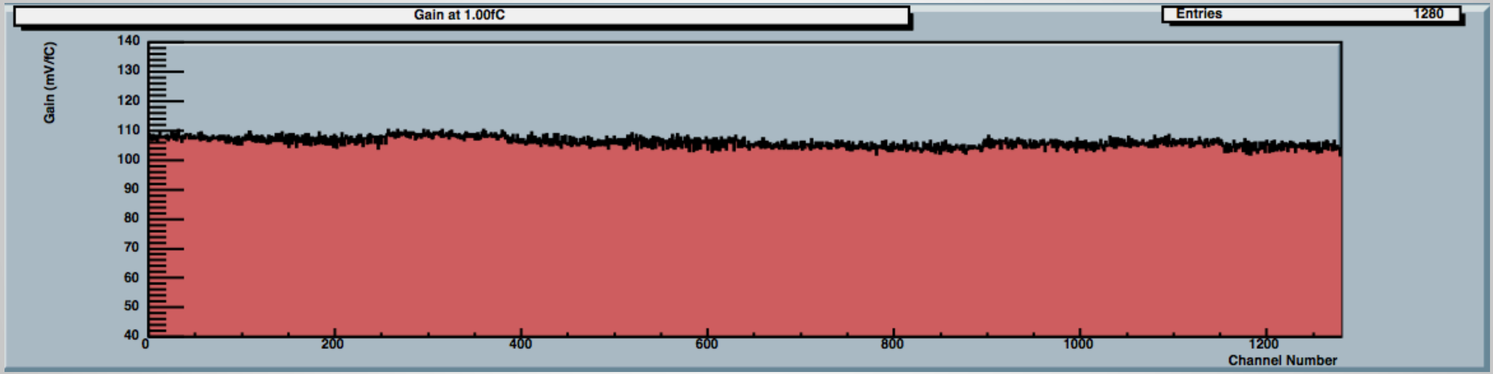
Thermal image @ 3A

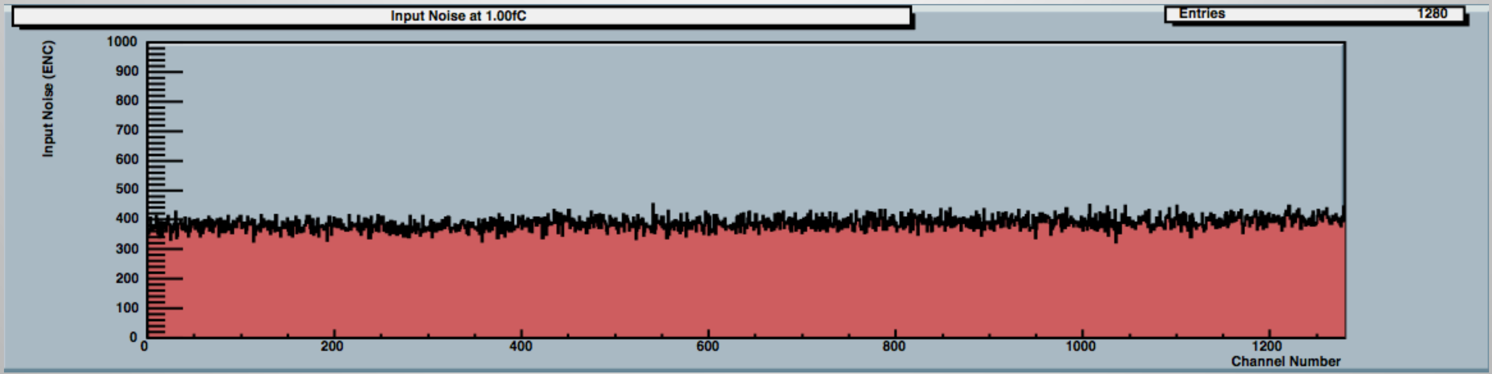


After 'curing' the short

Electrical measurements

- One hybrid fully mounted with SMDs & 20 FE chips
  - Digitally fully functional
  - Noise and Gain same as the ‘standard’ kapton hybrid





Summary

- MCM-D makes it possible to build front-end hybrids directly on the silicon sensor

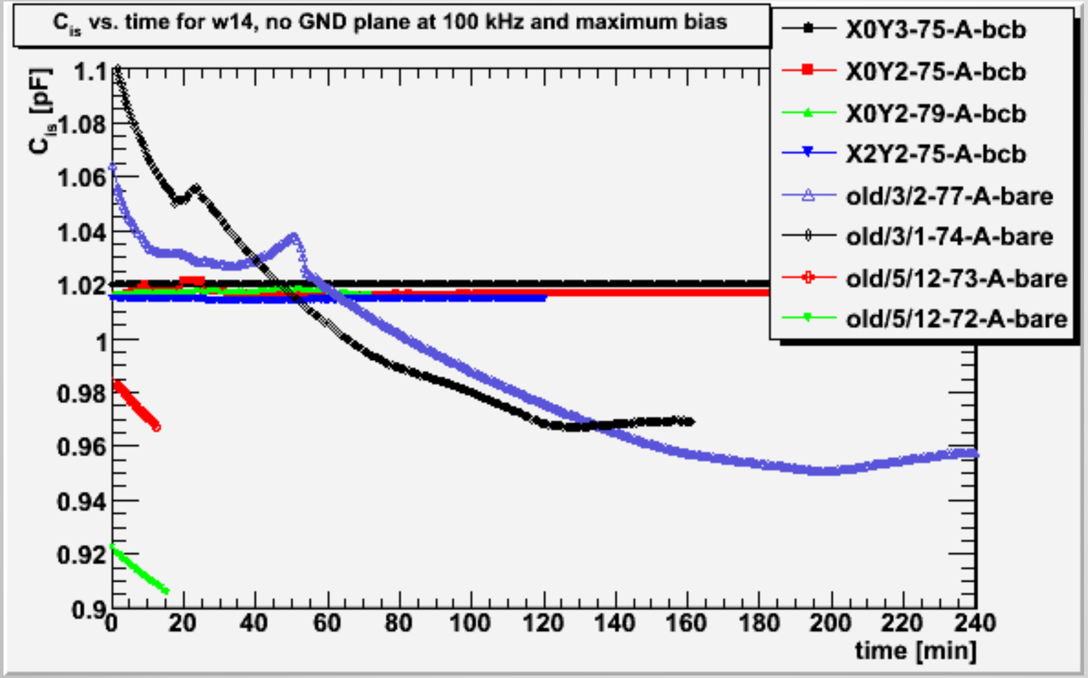
- The first prototype evaluated the influence on the sensor
  - Increased FE load: as expected
  - No other differences observed
  - Radiation hardness verified

- The second prototype implements a fully functional hybrid
  - Performance identical to kapton hybrid
  - Power plane short requires process development

Back-up slides

Inter-strip capacitance (C_{IS}) – bare & BCB covered

- Bare sensors show decrease in C_{IS} over time due to surface charge-up
  - Compensates for trapped charges
  - Need high voltage and long time to reach final value
  - Environmentally dependent

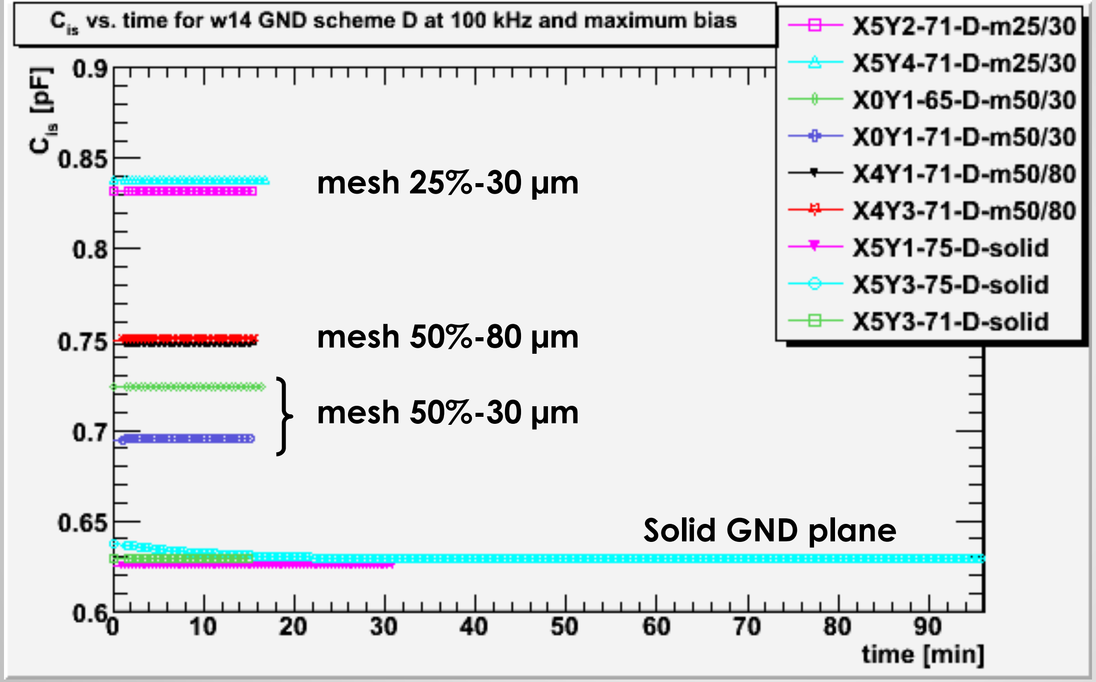


C_{IS} vs. time for bare and BCB covered (9 µm) sensors at 100 kHz

- BCB is a very good insulator: no charge compensation

Inter-strip capacitance (C_{IS}) – adding the GND plane

- Four different GND plane configurations covering the sensor
  - Solid and meshed with 25% or 50% fill, 30 or 80 µm line width



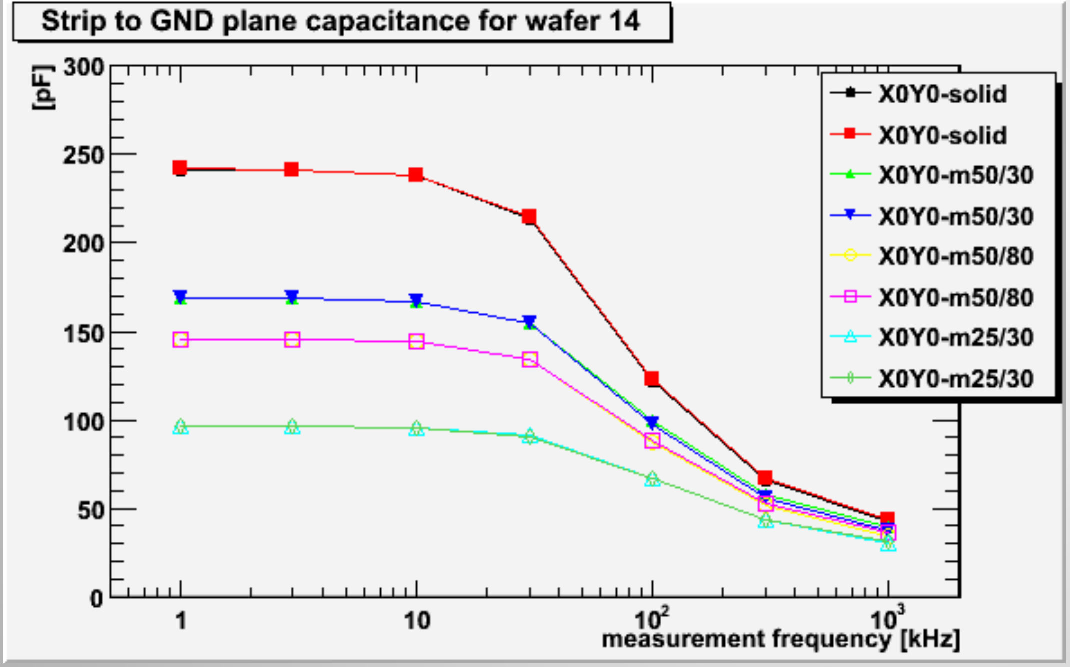
Cf. value from no metal

- C_{IS}(bare) < 0.9 pF
- C_{IS}(BCB) = 1.02 pF

- Adding the GND plane decrease the ‘pure’ C_{IS}
  - The metal plane facilitates the compensation of interface charges
  - Solid GND plane compensates better than meshed planes

Capacitance to GND plane - C_{sG}

- Capacitance from strip to GND plane measured separately
  - Measure between bias rail and GND plane in R_S-C_S mode
  - $R_S = R_{bias} / N_{strips}$, $C_S = C_{sG} * N_{strips}$



Total capacitance between bias rail and GND plane vs. frequency

GND plane type	C_{sG}
Solid	**1.85 pF**
50% fill, 30 um line	**1.30 pF**
50% fill, 80 um line	**1.15 pF**
25% fill, 30 um line	**0.76 pF**

Parallel plate capacitor estimate

$1.06 < C_{sG} < 2.65$

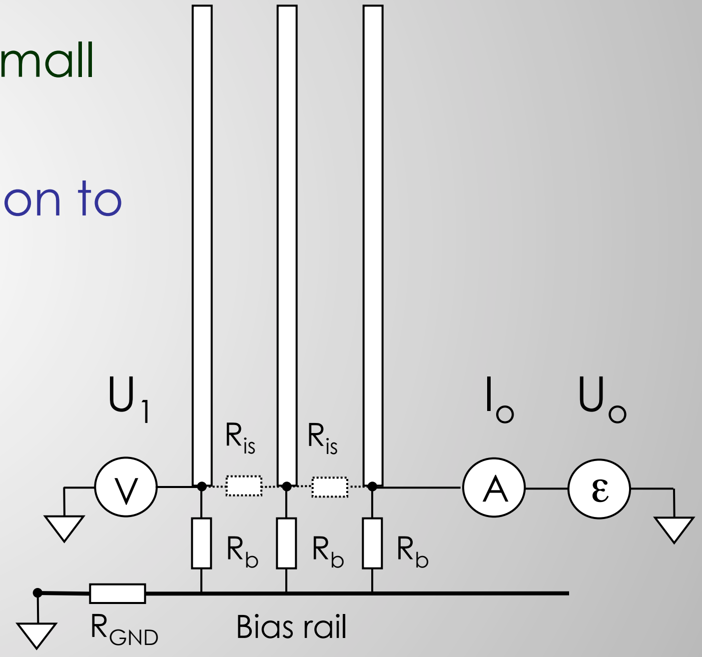
strip width = 32 µm

strip pitch = 80 µm

Inter-strip resistance

- Measure R_{is} by applying a voltage on one implant: U_0
  - dU_0/dI_0 gives bias resistance: R_b
  - Assuming all R_b identical and R_{GND} is small
    - ➢ solve for R_{is}
- Layout constraints only allowed connection to every second implant
  - R_{GND} limits the measurement
  - R_{is} only visible if:

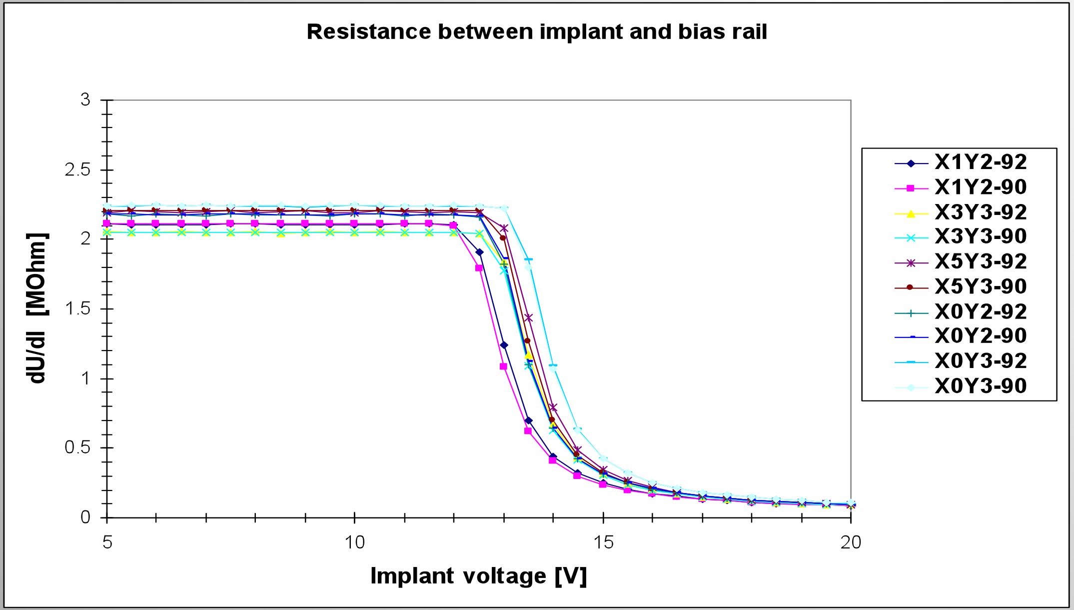
$$R_{is} << \sqrt{R_b^3 / R_{GND}} \approx 10^9\ \Omega$$



Measured inter-strip resistance sets a limit of R_{is} > 250 MΩ

Punch-through voltage

- Relevant in case of large charge deposition in the sensor
  - Implant shorts to the back-plane
  - Potentially catastrophic for the front-end
- Punch-through from strip-end to bias rail
  - Built in protection from this effect
- Apply a voltage between implant and bias rail
  - Measure dV/dI: sudden drop at onset of punch-through



Measured punch-through onset at 12-14 V.

Similar to values for non-processed sensors

Punch-through voltage: post-irradiation

- Degradation with irradiation
  - Increase in onset voltage
  - Increase in channel resistance
- No special punch-through structure implemented for these devices
  - Perhaps needed if feature required in high radiation