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MCM-D Technology for Silicon Strip Frontend Hybrids

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Multi-chip Modules - Deposited (MCM-D) technology can be applied to silicon strip modules and promises advantages in terms of integration complexity and material budget. The principle is to deposit alternating dielectric and metal layers directly on the silicon sensor, building up a PCB like structure. With lithographic techniques traces and vias are etched with high resolution creating a circuit replacing the pitch adaptor, wire bonds and electronics hybrid.

This paper reports on a feasibility study performed in the context of the Atlas Upgrade. The technology was evaluated in two prototype processing runs. The first prototypes had a single dielectric and metal layer deposited on a silicon strip sensor, with the purpose of evaluating the change in performance due to the post-processing and the presence of a ground plane. Sensor parameters were measured before and after irradiation up to $10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$ and charge collection efficiency was measured for several doses. A non-irradiated sensor was measured in a beam test yielding signal height and resolution for regions with and without ground plane. The second prototype was a fully functional 20-chip front-end hybrid with five metal layers build on a blank silicon sensor. The hybrid has the same performance as an identical circuit built in kapton technology.

Summary

The next generation silicon tracking detectors are tending to a higher density of read-out channels over a large area. Hence an increased level of integration of the detector modules is desirable. Multi-chip Modules - Deposited (MCM-D) technology applied to silicon strip modules and promises advantages in terms of integration complexity and material budget. The principle is to deposit alternating dielectric and metal layers directly on the silicon sensor, building up a PCB like structure. With lithographic techniques traces and vias are etched with high resolution creating a circuit replacing the pitch adaptor, wire bonds and electronics hybrid.

The features sizes possible are smaller compared to traditional PCB technologies. Minimum track width and spacing is in the order of 10-30 μm and vias are in the order of 50 μm . Layer thicknesses are typically 3-15 μm for dielectric layers and 1-3 μm for metal layers.

This paper reports on a feasibility study performed in the context of the Atlas Upgrade. The technology was evaluated in two prototype processing runs performed by a semi-industrial partner (Acreo,

Norrköping, Sweden). The first prototypes had a single dielectric and metal layer deposited on a silicon strip sensor, with the purpose of evaluating the change in performance due to the post-processing. The design had via-connections to the strip pads and different types of ground planes covering the sensor area. This corresponds to the first layer of processing in a full design, hence giving the bulk of the change in performance of the sensor.

Sensor parameters such as I/V , C/V , C_{is} and R_{is} were measured for non-irradiated samples and for an array of doses up to 10^{16} n_{eq}/cm^2 . Charge collection efficiency was also measured for the same doses. A non-irradiated sensor was measured in a beam test yielding signal height and resolution for regions with and without ground plane.

The second prototype was a fully functional 20-chip front-end hybrid with five metal layers build on a blank silicon sensor. The hybrid is digitally fully functional and shows the same analogue performance parameters (noise, gain, stability) as an identical circuit built in kapton technology.

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