

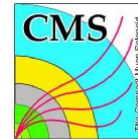
# ***A Level-1 Tracking Trigger for the CMS Upgrade using stacked silicon strip detectors and advanced pattern recognition technologies***

Gaëlle Boudoul

IPN-Lyon

On behalf of the CMS Collaboration

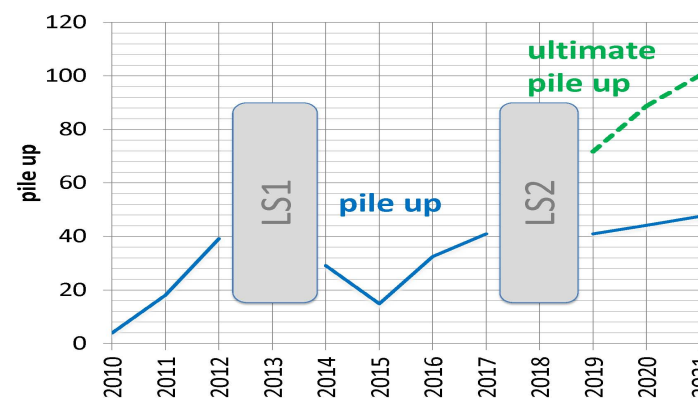
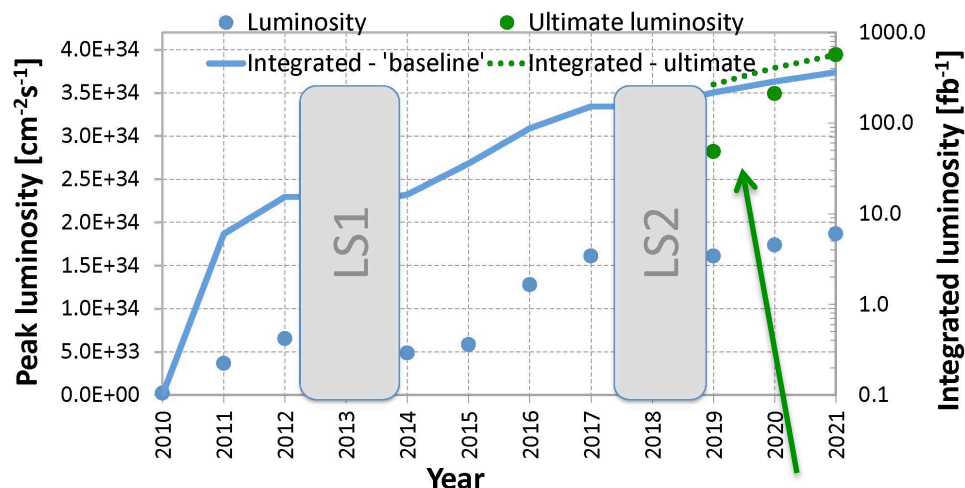
***WIT2012 – Workshop on Intelligent Trackers (Pisa-Italy)***



# *Outline*

- Motivation for upgrade
- Motivation for L1 Tracking Trigger for CMS Tracker Upgrade
- Tracker Reduced Readout
- Tracker Layouts and L1 Tracking concepts
- Performance and Triggering capabilities: First Results on Barrel-Endcap Geometry
- Conclusions

# Motivation for upgrade: LHC luminosity and Pile-up



M. Zimmerman Fermilab workshop Nov 2011

Possibly higher luminosity with 50ns bunch spacing after injection upgrade

## 2022: Long Shutdown 3 → High luminosity project (HL-LHC)

Prepare for operation at  $5 \cdot 10^{34} \text{ cm}^{-2} \text{ sec}^{-1}$

Prepare for an integrated luminosity of  $3000 \text{ fb}^{-1}$  ( $200 \text{ fb}^{-1}$  to  $300 \text{ fb}^{-1} / \text{yr}$ )

50 vs 25ns operation offers flexibility, but pile-up affect performance and upgrade detector designs,

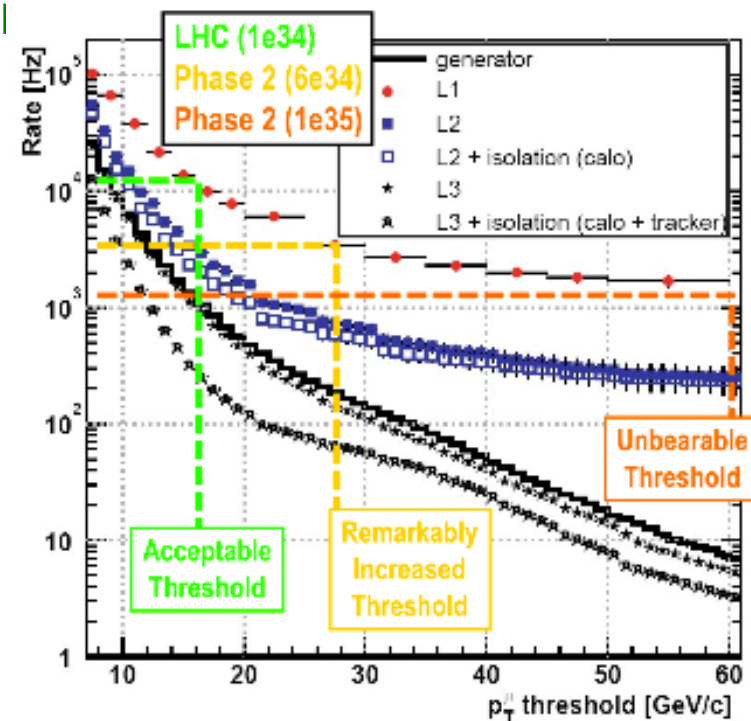
**200 PU in phase2 if  $5 \cdot 10^{34} \text{ Hz/cm}^2$  at 50ns spacing**

Increase of the LHC luminosity well above  $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$  requires substantial upgrade of the CMS Tracking:

- Physics potential require full performance detector
- Higher radiation resistance (instantaneous and integrated level)
- Higher readout granularity (keep channel occupancy at an adequate level)
- Ability to contribute information for the L1 trigger

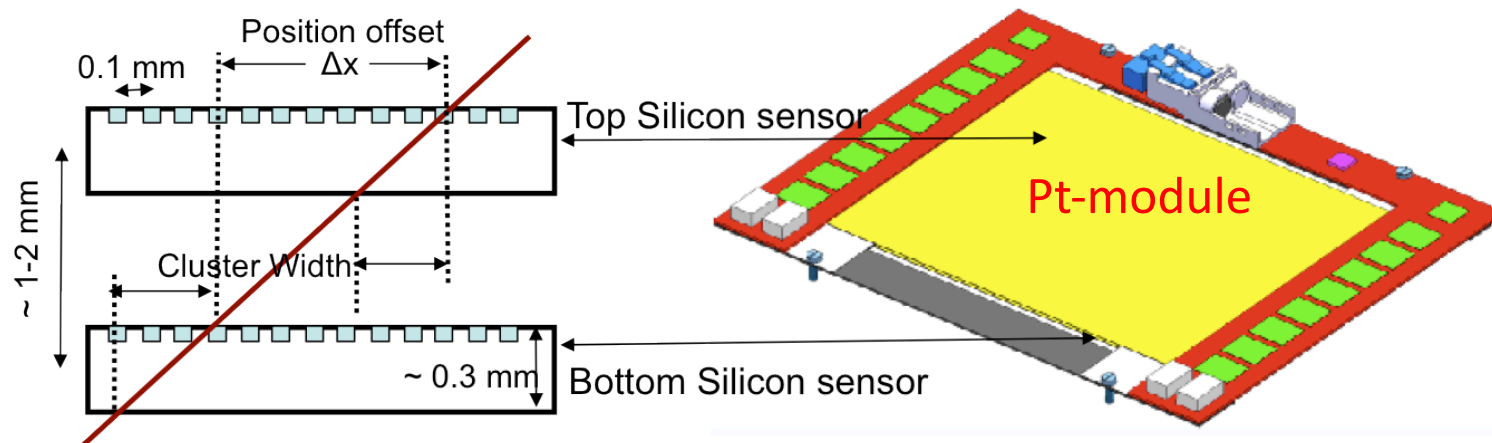
## Motivation for a L1 Tracking Trigger

- Trigger system needs to maintain an output rate at 100kHz (despite the factor 5 increase in luminosity and the 5 to 10 times larger pile-up)
  - Impossible to achieve using only information from the detectors
  - Flattening of the L1 rates as a function of the  $p_T$ 
    - Increasing the thresholds will not help
- The tracker data will have to provide trigger tracks used at the L1 stage to allow:
  - Precise transverse momentum measurement of muons for application of a sharp threshold around 10-20 GeV/c.
  - Matching and isolation for electron and tau identification and veto for photons.
  - Association to proper interaction vertices to reduce rate of accidentals due to pile-up.



# Tracker-Trigger: how to reduce data volume

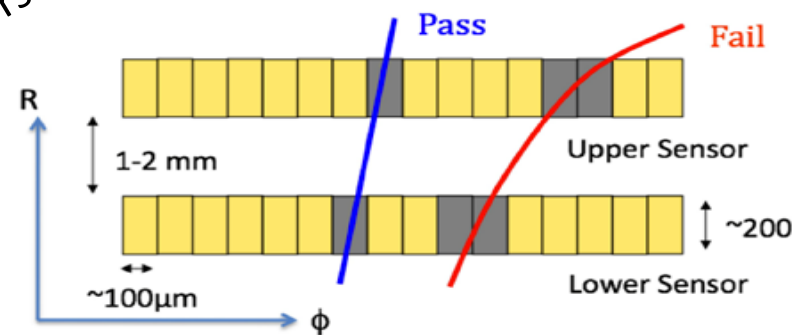
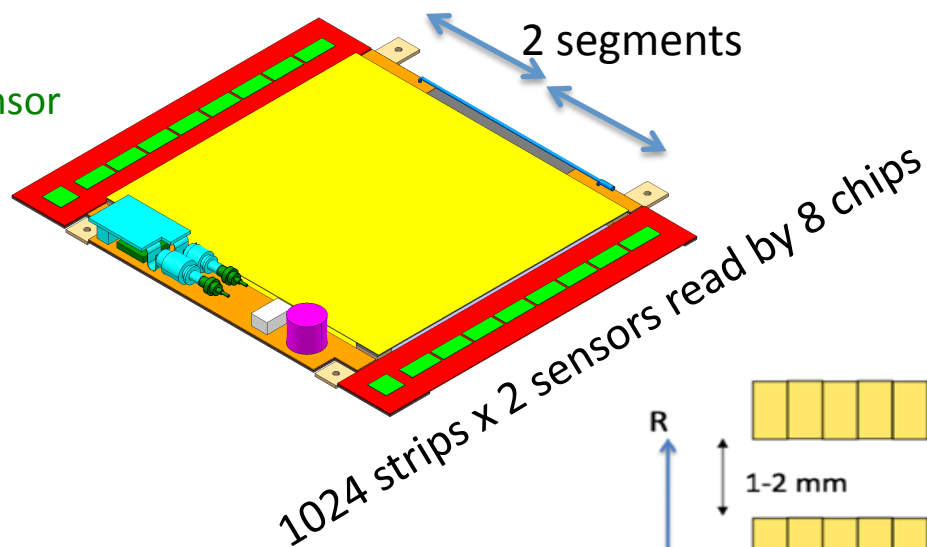
- About 90% of the charged particles produced in minimumBias collisions have  $P_t < 1 \text{ GeV}/c^2$  and  $\sim 97\%$  have  $P_t < 2 \text{ GeV}/c^2$ 
  - **Reduced readout of hits associated with tracks above  $\sim 2 \text{ GeV}/c^2$**
- Two complementary steps to reduce data volume (both based on the track deviation in the plan perpendicular to the CMS magnetic field):
  - **STEP1: Cluster width approach**
    - Preselection of hits according to their cluster width (CW)
      - CW is proportional to the radial distance of the sensor from the IP and inversely proportional to the  $P_t$
  - **STEP2: Stacked tracker:** correlation between preselected hits in nearby sensors
    - Exploit track direction of flight measurement to reconstruct 'track stubs' above a given  $P_t$  threshold.



# Detector Modules

## 2Strip Pt Module

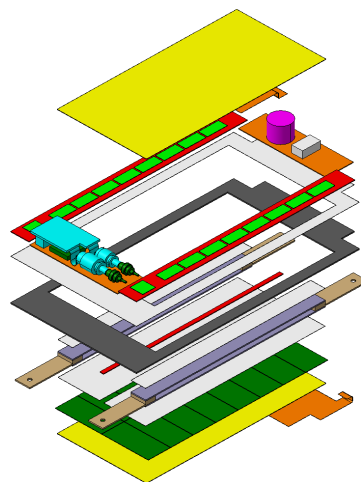
- 2 closely spaced strip sensors
- Pitch 90  $\mu\text{m}$
- Strip length: 46.3 mm
- Pt information (trigger)



**correlate selected hits in two closely separated sensors to discriminate between high and low Pt tracks**

## Pixel+Strip Pt module

- Pitch 99  $\mu\text{m}$
- Strip length 21 mm
- Pt information (trigger)
- z information



# Two complementary Tracker layouts

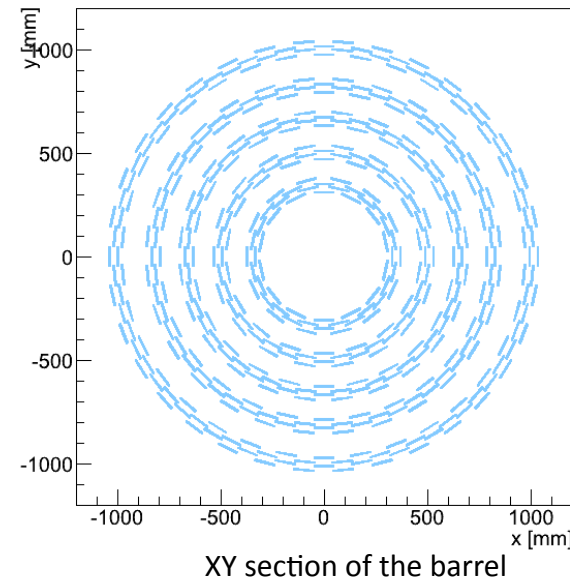
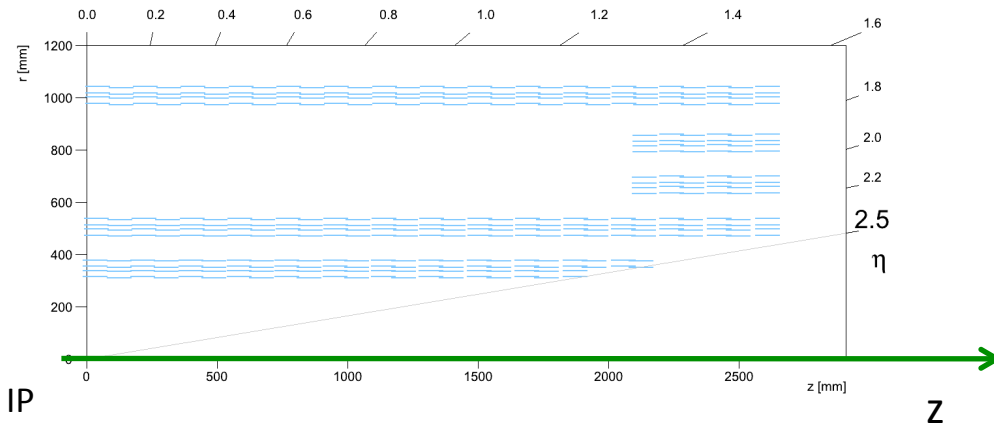
## I) Long Barrel geometry



Dedicated talk (E. Salvati)  
this conference

Long closely spaced layers of Pt Modules arranged in Double Stacks separated by ~4 cm

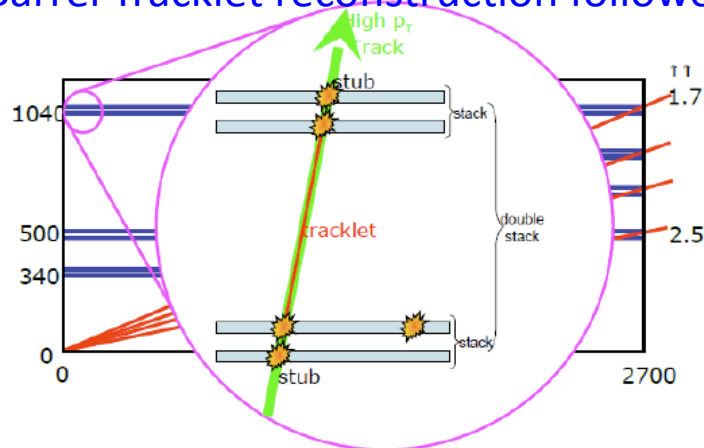
(Full long Barrel outer tracker of stacked triggering layers)  
Cluster positions in z direction provided (pixelated modules).



### From Hits to L1 Tracks:

Super Layers => Stubs -> Tracklets -> L1 Tracks

Long Barrel Tracklet reconstruction followed by propagation to next super layer



L1 tracking precision potential

$p_T$  resolution 2% @ 10 GeV in forward

Tracking precision

$p_T$  resolution 2.1% @ 10 GeV

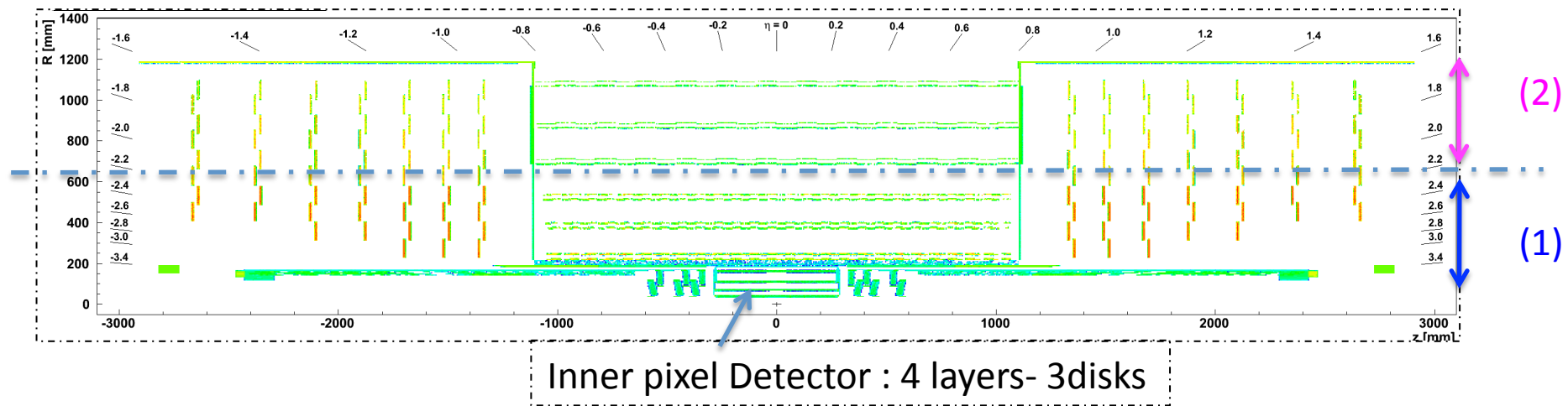
$p_T$  resolution 5% @ 100 GeV

# Two complementary Tracker layouts

## II) Barrel-EndCap Geometry



The “Barrel-EndCap” design comprises 6 barrel layers and 7 endcap disks composed of rings.



The inner part (1) is populated by Pixel-Strip stacked (PS) modules .

The outer part (2) is populated by Strip stacked (2S) modules.

The number of endcap disk is optimized for tracking performance.

Different spacings between the two sensors of the Pt modules:

0.8mm in the outer barrel (2S)

1.6 and 2.6mm in the inner barrel (PS)

4.0, 2.6 and 1.2mm in the outer end-cap (2S)

4.0mm in the inner end-cap (PS)

L1 tracking precision potential

pT resolution 4% @ 10 GeV in forward

Tracking precision

pT resolution 1.4% @ 10 GeV

pT resolution 3% @ 100 GeV



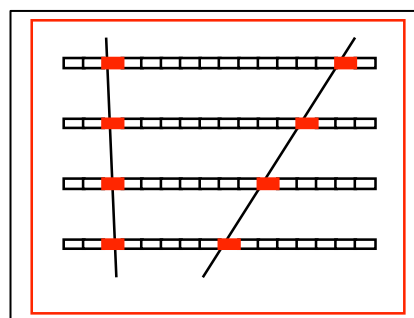
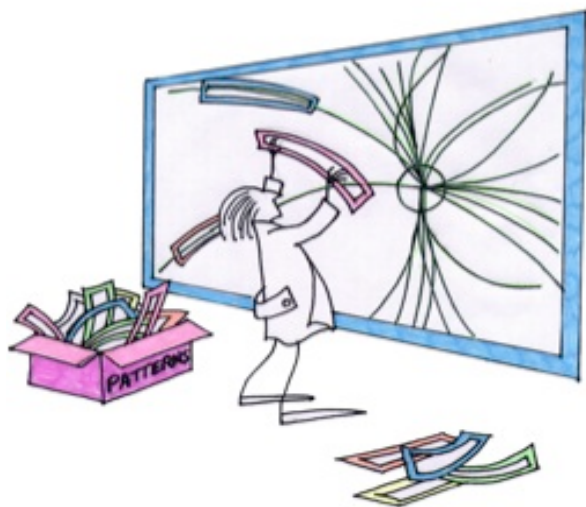
# From Hits to L1 Tracks (Barrel-EndCap geometry)

Independent Pt layers => Stubs -> L1 Tracks

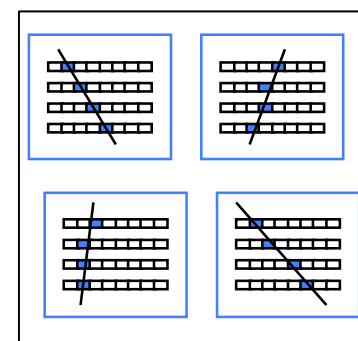
Barrel -EndCap track reconstruction from pattern comparison using Associative Memories

Pattern Matching using Associative memory  
(M.Dell' Orso and L. Ristori: initial idea in 1985)

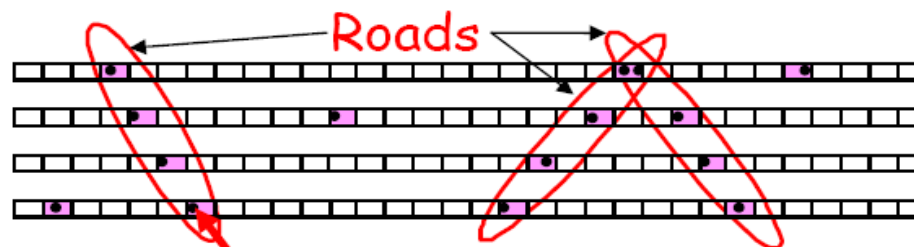
Hardware-based pattern recognition for fast track triggering has been very successful for HEP (CDF SVT)  
**Enormous** challenges in implementing pattern recognition for tracking trigger at HL-LHC, due to much higher occupancy (pile up), event rates and high granularity



The Event

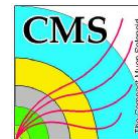


The Pattern Bank



Find low resolution track candidates first (roads)

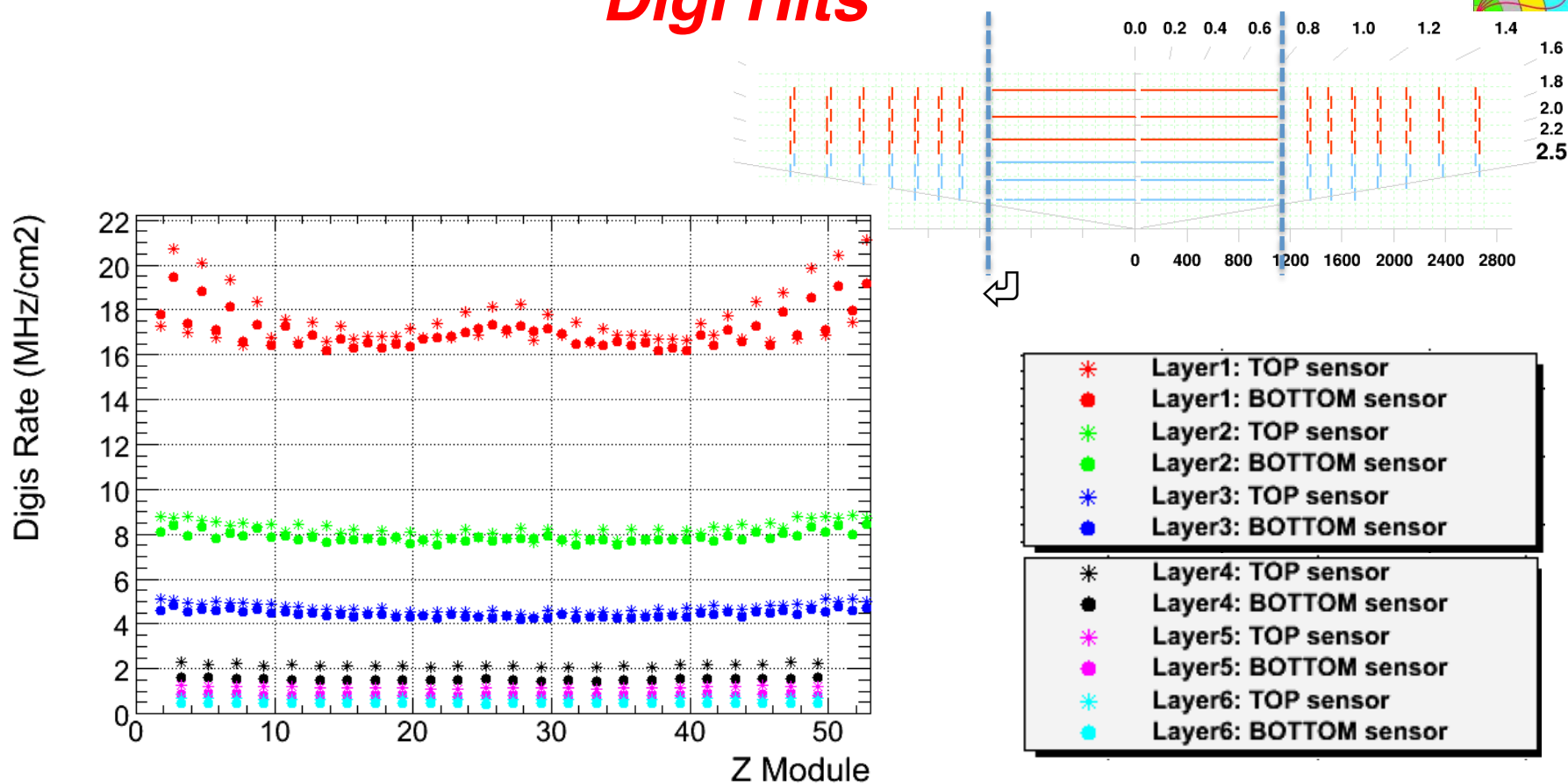
Then perform track fitting downstream



## *Performance and Triggering capabilities First Results on Barrel-Endcap Geometry*

- Full Simulation of the Barrel-EndCap Geometry with Material Budget (**Only the BARREL part is considered for the moment**)
- MinimumBias sample @14TeV - 200 PU events - 50 ns bunch spacing (20MHz)
- First Results will be presented for
  - Digi hits
  - Clusters (selective readout step1)
  - Track Stubs (selective readout step2)
  - Turn-on Curves (efficiency)
  - Tracks at L1 using using Associative Memories

# Digi Hits

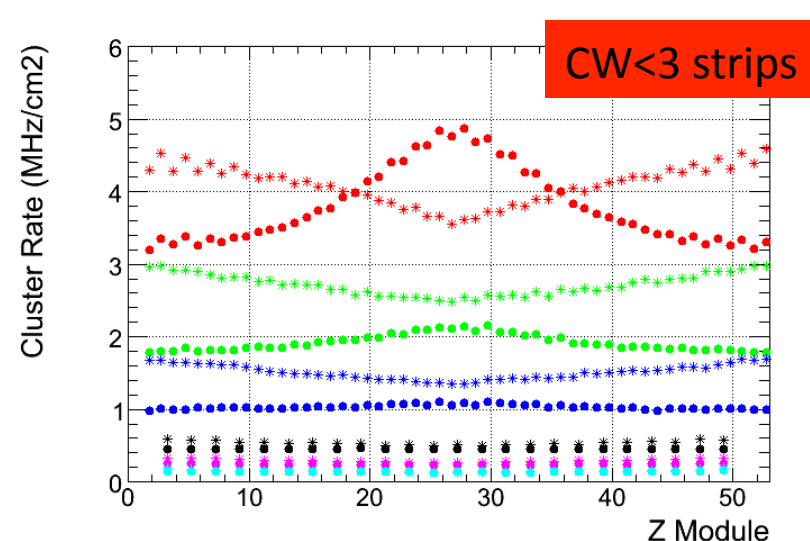
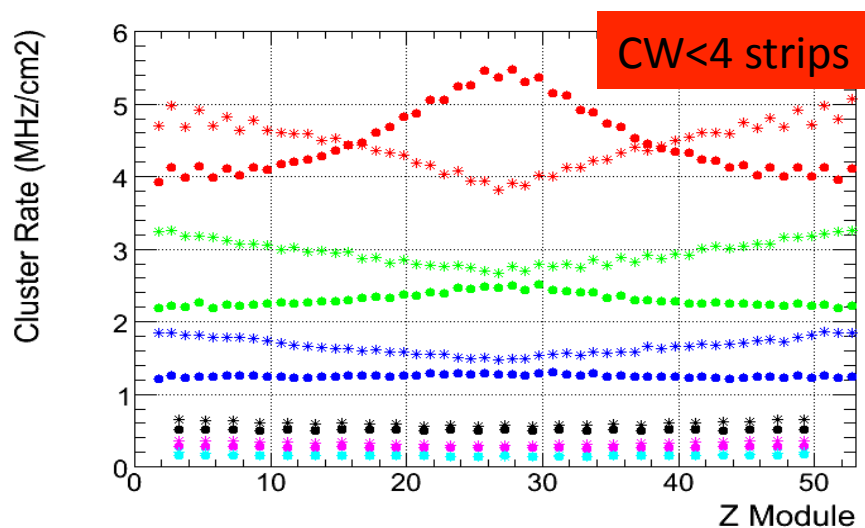


The rates (MHz/cm<sup>2</sup>) are given as a function of the position of the modules along z axis for bottom and top sensors separately.

Rates are decreasing with radius as expected

Rates on the top sensor are higher compared to the bottom rates -> Hits coming from secondaries particles produced in between.

# Reduced Readout Step1: Cluster Rates

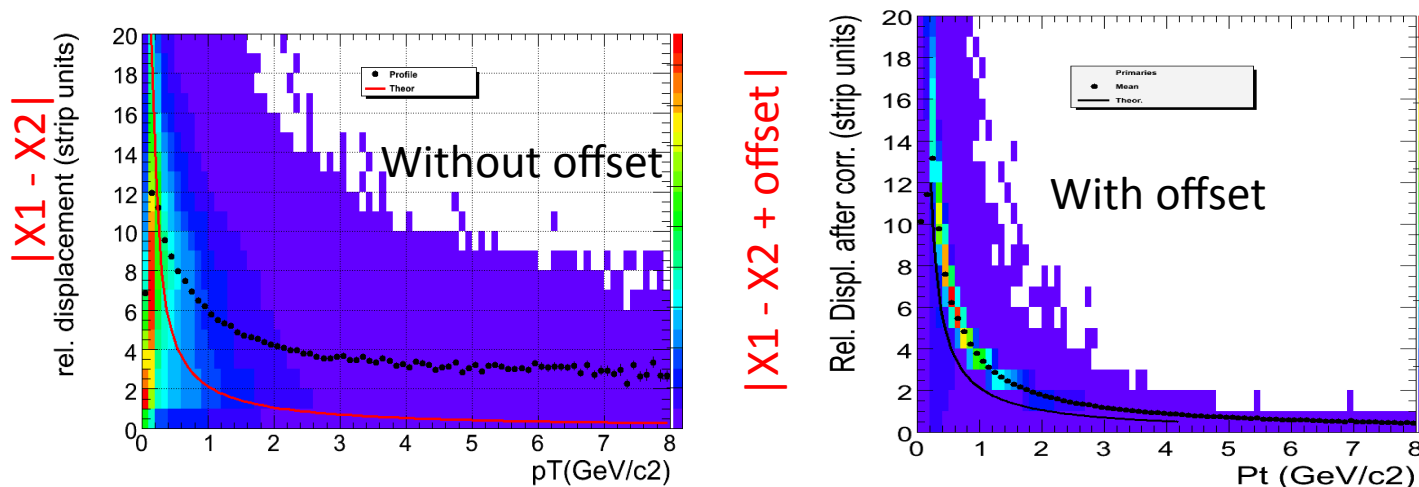


Two different cuts on cluster width (CW) lead to a significant impact on the initial cluster rates:  
 Cut1 : CW < 4 -> cluster data reduction = 14-16% (depending on the layer)  
 Cut2 : CW < 3 -> cluster data reduction = 27-28% (depending on the layer)

These cuts should be optimized to reduce the rates without affecting the final efficiency when applying the 2<sup>nd</sup> step (stub building)

# Reduced Readout Step2: Track Stubs

- The position of the preselected clusters is defined by the center of the cluster with half strip resolution
- Correlated hits in nearby sensors are stubs ( $X1$ =position of the bottom sensor /  $X2$  = position of the top sensor).
- Cluster Position Correction (offset) according to their location on the bottom sensor is needed in order to take into account the flatness of sensors:



**Position correlation in a Pt-module**

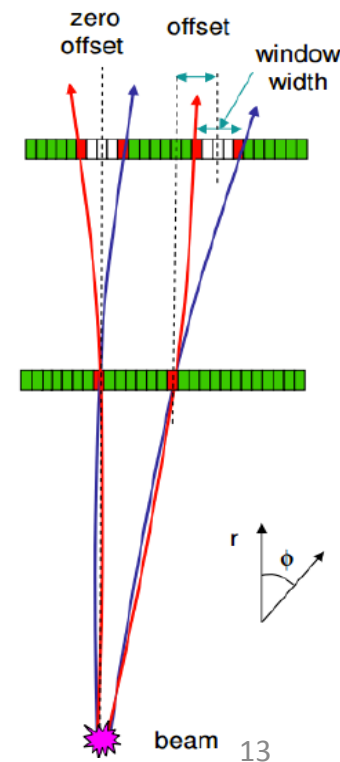
-For each cluster on the bottom sensor, a matching window centered on its position (+offset) is defined on the top sensor.

$$|X1 - X2 + \text{offset}| < \text{Diffmax}$$

Diffmax corresponds to the threshold (window size according to the expected Pt cut

-A stub is produced if a cluster position is found in the window

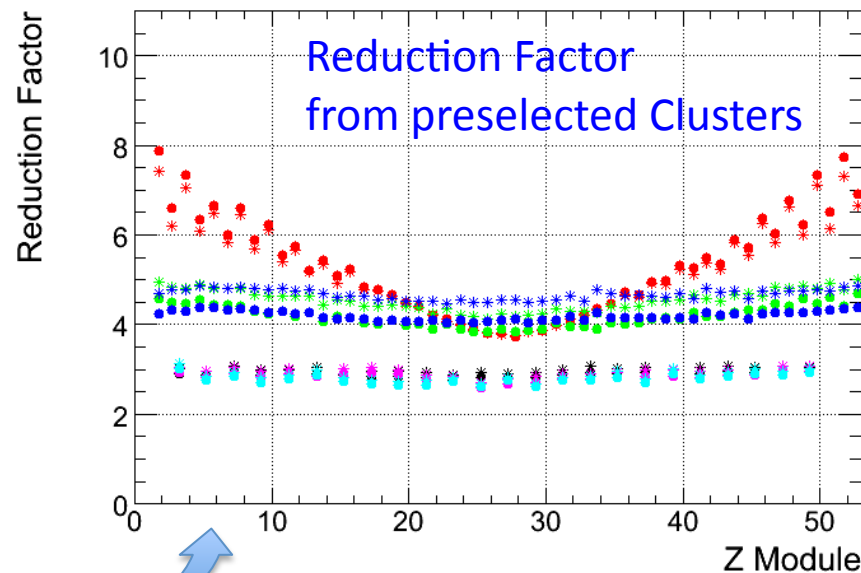
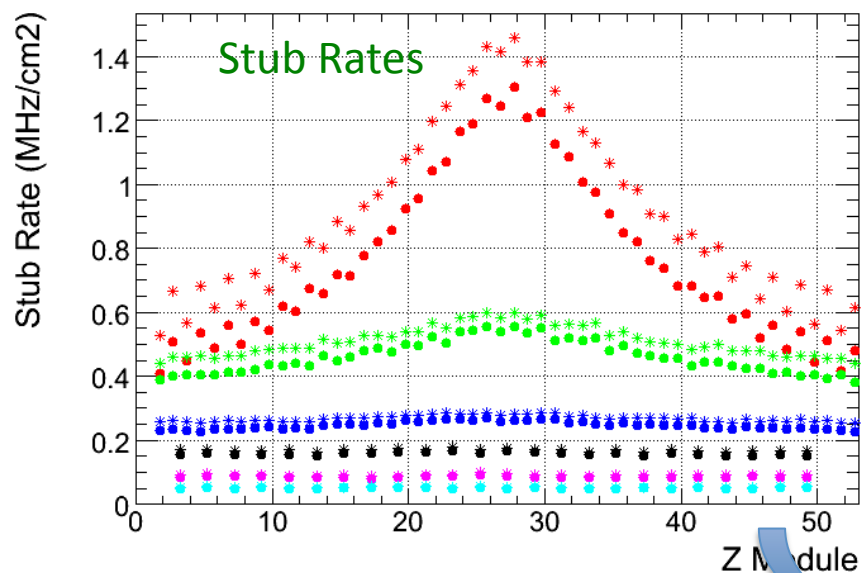
-A cluster can form ONE stub at maximum.



# Track Stubs Rates and Reduction factor

* Layer1: CW<4	● Layer4: CW<3
● Layer1: CW<3	* Layer4: CW<4
* Layer2: CW<4	● Layer5: CW<3
● Layer2: CW<3	* Layer5: CW<4
* Layer3: CW<4	● Layer6: CW<3
● Layer3: CW<3	* Layer6: CW<4

Window width=6 strips

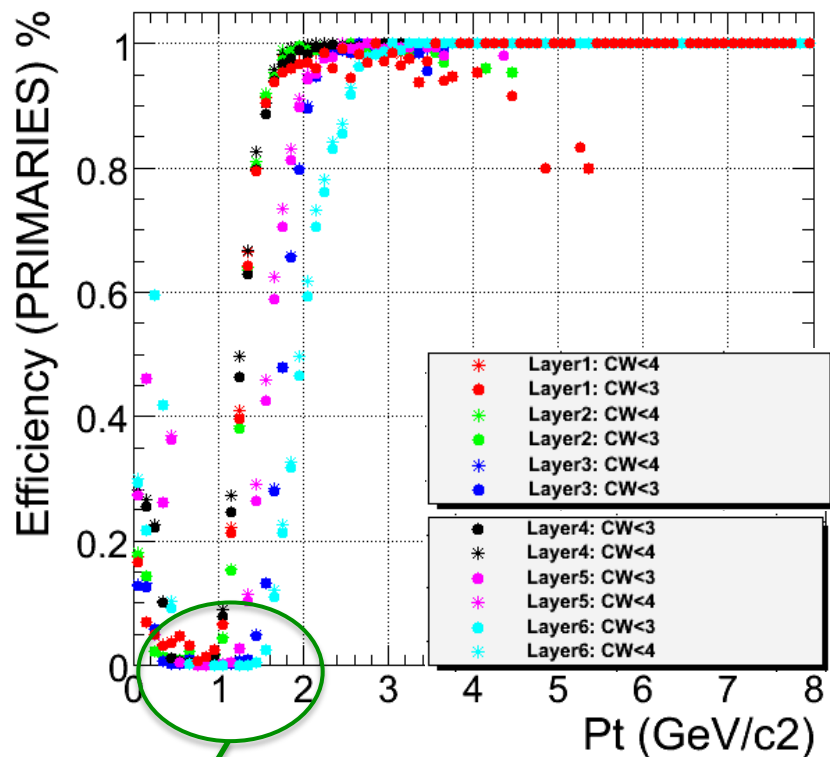


Like clusters, the rates are reduced when applying a tighter cut on the CW

The reduction factor from preselected clusters is higher for inner layers  
 The cut (Ww width) is the same on every layers:  
 It should certainly be optimized according to the radius and sensor spacing.

# Track Stubs: Turn on curves

Stub production efficiency (physical processes associated to primary vertices only)



Same window cut -> different thresholds depending on the radius

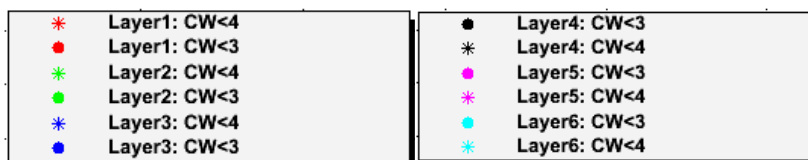
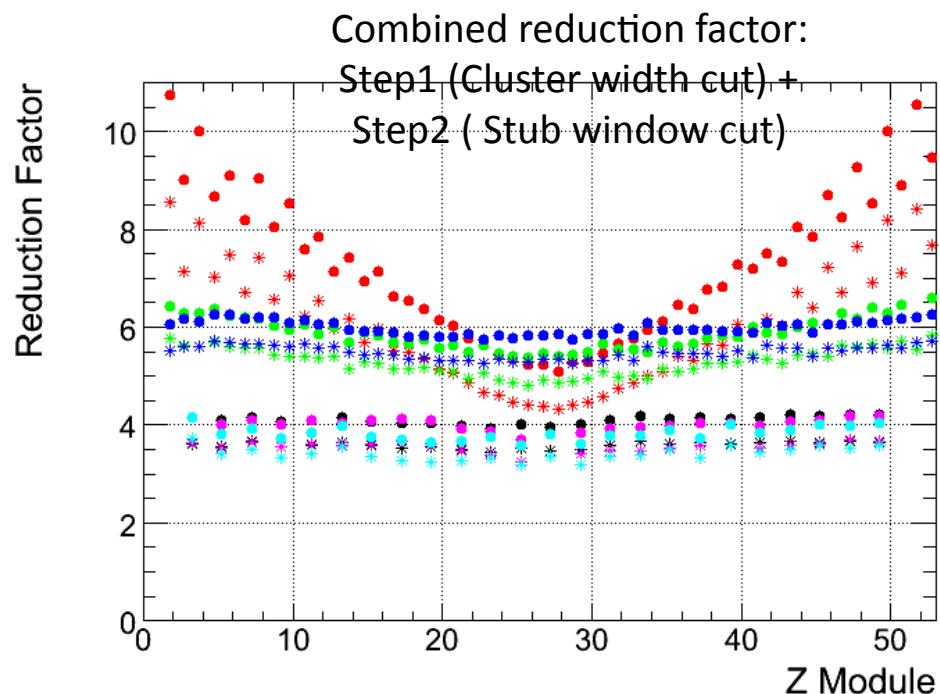
Effect of the cut (window size) is clearly visible, the efficiency is dropping dramatically below 1-2.5GeV depending on the layer.

The cluster width cut is reducing the rates without affecting noticeably the primary stubs production efficiency.

The window size should now be optimized for each layer separately, in order to maximize the reduction factor while keeping a high efficiency above the cut

The shape at very low Pt (<200MeV) is not fully understood, yet. Most likely due to primary looper tracks

# Reduced Readout: Combined Reduction Factor



Several issues for each layer (work in progress):

-78% of tracks are coming from secondary particles (nuclear interactions,...). Secondary vertices can be far from the interaction region which lead to a bad correlation between two clusters

-Impact of secondaries should be carefully evaluated

-The sensor spacing might be refined (currently L1:2.6mm, L2-L3:1.6mm, L4-L5-L6: 0.8mm)

-An appropriate pt cut (i.e Window size) depending on the layer should be defined

In summary: in addition to the track behaviour understanding (loopers, primaries/ secondaries), the optimal set of {sensor spacing / Pt cut} should be derived in order to get the best compromise between a high data reduction factor and a high efficiency above the Pt cut



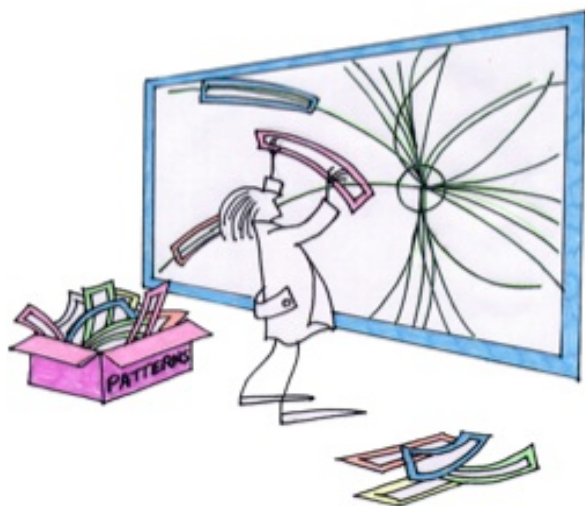
# From Stubs to Tracks at L1 using Associative Memories

## Current status for the barrel-EndCap Geometry (INFN-Pisa/IN2P3-Lyon)

- Study the feasibility of a track trigger at L1, based on the same idea than the ATLAS FTK:
  - Rough pattern recognition (*compare active regions with prestored patterns*)
  - Fast track fit (*using hits contained in the matching patterns*)

→ Feasibility studies made by **Giuseppe Broccolo** in 2011 for first version of a barrel-endcap tracker layout (presented at [TIPP 2011](#))

- Develop a flexible software emulation in order to test the feasibility/scaling of such a system with the different tracker geometries foreseen.
- Study in parallel the hardware part of the problem (*ATLAS is working at the HLT, we want to work at L1: 40MHz!*).



# **Bank Pattern:**

## **First step: dividing the Tracker into sector**

**Sector size (in  $r/\varphi$ ) is geometrically constrained by the minimal Pt of the track one wants to recover (2GeV/c in our case)**

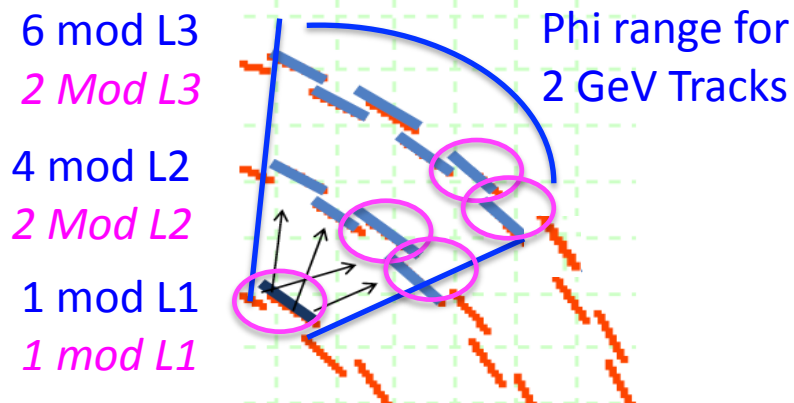
**The sector size is also technically constrained by the maximum number of hits which might be fed into the AM card at L1**

**For the moment we considered only the barrel part (3 outer layers)**

*-From a given hitted module on the first considered layer, one can derive the phi range in terms of number of modules on the next 2 layers  
(A super Sector contains 11 modules)*

*-In order to keep the dimensions of the system as small as possible, (i. e 5 modules per sector) one can divide the combinatorics of possible modules from the supersector into three sectors of 5 modules in  $r/\varphi$*

### **Super-Sector and Sector (schematic representation)**



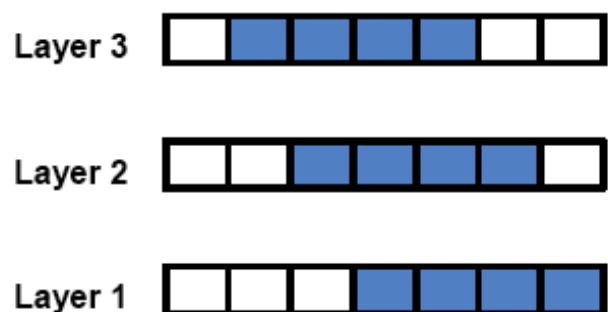
→The size of the reduced sector (5 modules) might involve depending on the technical constraints

→Considering the relative symmetry of the system, it is straightforward, from there, to get the sectors for all the Tracker

# Bank Pattern: SuperStrips and Data Format

A pattern is a set of super-strips (one per layer) defining a road into the tracker

The SuperStrip is the main parameter of the system



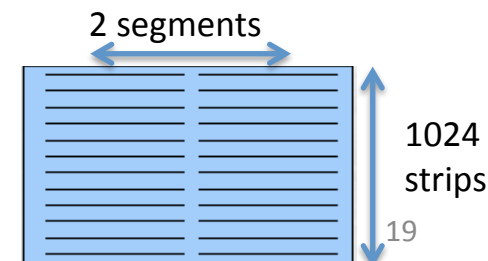
Pattern 1

Geometrically, the super strip is nothing else than a low granularity tracker strip  
 Technically, what is sent to the AM card is the address of the super-strip in the considered sector

The pattern is then defined with 3 x 12 bits  
 (3 outer layers considered for the moment)

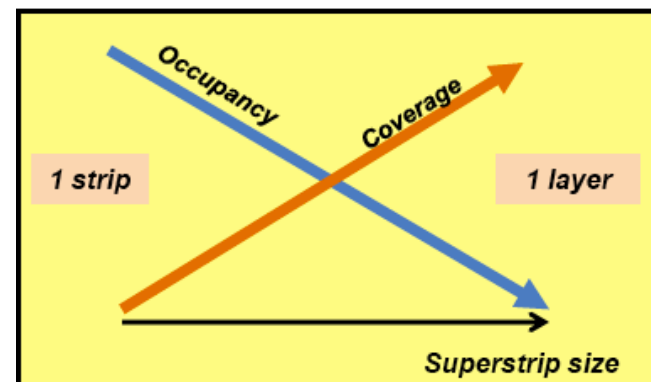
12 bits to code the super strip :  
 Z module position : 4 bits  
 Phi position : 1 bit  
 Segment(\*) : 1 bit  
 Super strip position : 6 bits (64 possibilities :  
 allows a pitch of ~1.6 mm)

(\*) A sensor on a module is divided into 2 segments of 1024 strips



# Bank Pattern Generation

Find the balance between the best coverage (*ensure that all interesting tracks are contained into at least one pattern*) and the best occupancy (*minimize the number of tracks/hits per pattern*).

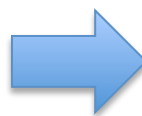
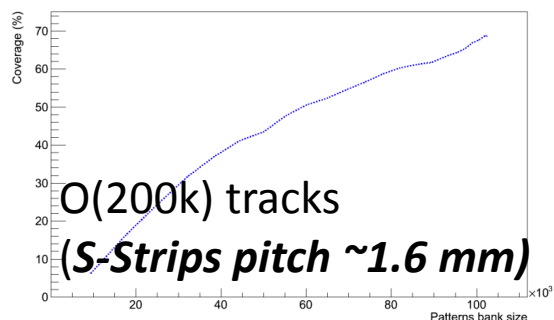
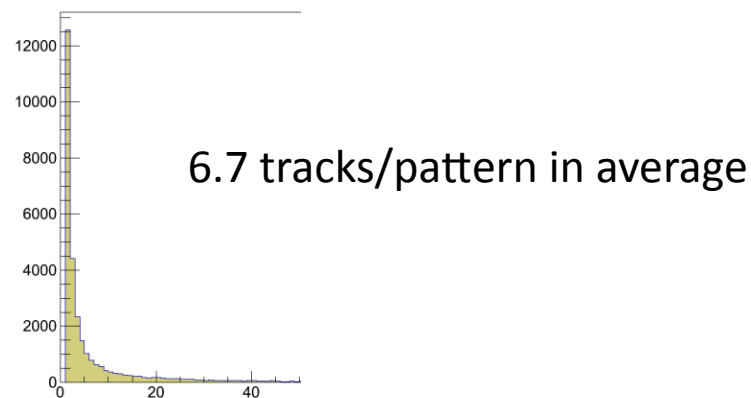
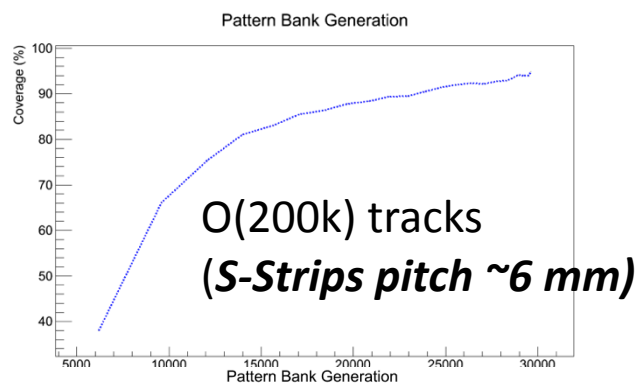


Iterative method: every step (bunch of 10k muon tracks)

Generate patterns and add them in the bank

Compare the number of patterns at iteration  $i$  with the one at iteration  $i-1$

Keep going until the number of patterns is reaching a maximum (full coverage)



Not enough tracks to fill the bank...  
Use a larger events set to create the 1.6 mm pattern bank (*in progress*)

# Next Steps and Hardware developments

- Optimize AM bank size and sector dimensioning
  - study bank size as a function of the minimum pT and cluster position resolution
  - Cabling possibilities (configuration should fit hardware constraints)
- Test the patterns banks with Minimum Bias events (including high pile-up) with a dedicated AM emulation software
- Study latency an feasibility with SW and HW setup (IN2P3Lyon-INFNPisa-Perugia)
  - Interface pt-modules with boards pre storing a fixed # of patterns which simultaneously see stubs leaving detector at full speed.
  - Test made on the CDF system using 5K patterns per AM chip with simulated data and that the HW returns the same tracks that pass the selection on simulated AM chip

## Pattern Bank and Hits Files

**Pattern bank file**

```
008000 0708 0819 7925 7075 0075 7075
008001 0a29 080b 7965 7075 0075 7075
008002 0008 080a 790a 7075 0075 7075
008003 070f 0815 7916 7075 0075 7075
008004 0734 0809 7952 7075 0075 7075
008005 084b 080f 7a9e 7075 0075 7075
008006 0222 0035 7a3c 7075 0075 7075
008007 0815 0820 7a24 7075 0075 7075
008008 0640 07e1 7789 7075 0075 7075
008009 061c 072b 7730 7075 0075 7075
00800a 0633 070c 778c 7075 0075 7075
00800b 063c 0706 779e 7075 0075 7075
00800c 0610 071f 7727 7075 0075 7075
00800d 059e 058f 75a9 7075 0075 7075
00800e 0513 053b 751e 7075 0075 7075
00800f 0125 0540 754e 7075 0075 7075
008010 0134 05d1 7568 7075 0075 7075
008011 0432 0708 7789 7075 0075 7075
008012 064a 0788 7792 7075 0075 7075
008013 042f 07e1 779a 7075 0075 7075
008014 0607 070e 7712 7075 0075 7075
008015 093b 08e0 778c 7075 0075 7075
008016 0514 0493 7446 7075 0075 7075
008017 0512 0412 740f 7075 0075 7075
008018 0521 0432 7439 7075 0075 7075
008019 0212 0422 742a 7075 0075 7075
00801a 0239 04e3 7493 7075 0075 7075
00801b 0041 0490 74a9 7075 0075 7075
00801c 0136 0406 7480 7075 0075 7075
00801d 0101 0418 7429 7075 0075 7075
00801e 012a 043c 7442 7075 0075 7075
00801f 083f 0a83 7894 7075 0075 7075
008020 0142 0490 7887 7075 0075 7075
008021 0111 0a18 781a 7075 0075 7075
008022 0441 0783 7792 7075 0075 7075
008023 0846 078e 77a2 7075 0075 7075
008024 0802 0705 7708 7075 0075 7075
008025 0826 0742 7750 7075 0075 7075
008026 0702 0805 7908 7075 0075 7075
008027 0716 0828 7932 7075 0075 7075
```

Pattern bank with 5000 pattern per chip

Are used only three input bus

**Hit file**

```
00843 00a11 00b2b 00075 00075 00075
00649 0071b 007aa 00075 00075 00075
00733 009a3 00917 00075 00075 00075
0084b 00b34 00b15 00075 00075 00075
0070a 008c9 0082b 00075 00075 00075
00842 00918 00aac 00075 00075 00075
00a44 00a3c 00b2a 00075 00075 00075
00a43 00a33 00a14 00075 00075 00075
00a40 0083f 0089a 00075 00075 00075
00902 00bce 00a81 00075 00075 00075
00843 0091f 00ab7 00075 00075 00075
00e10 009e7 00a07 00075 00075 00075
00a14 009e1 00a4b 00075 00075 00075
00a24 00991 00a06 00075 00075 00075
00a51 00937 00915 00075 00075 00075
00a43 00a17 00a68 00075 00075 00075
0071c 009a4 00930 00075 00075 00075
0090e 00be1 00a50 00075 00075 00075
00737 0080a 0082b 00075 00075 00075
00b2c 00a6f 00a69 00075 00075 00075
00639 00636 00691 00075 00075 00075
00724 00996 00984 00075 00075 00075
00824 00909 00a3a 00075 00075 00075
00948 00a2e 00a88 00075 00075 00075
00919 00b0b 00805 00075 00075 00075
```

The hit file is loaded in the input FIFO

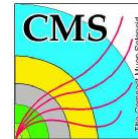
**Reference File**

```
858e053
858d401
850b2bb
850b1f2
850c046
840f9fc
840c333
840c332
840b45b
38000001
840a33f
38000002
858cb5c
858c1c0
858abfa
8589b86
850d05b
850c946
```

Output road split by event

**TEST OK**  
The AMBSiim board has matched all the expected roads

See talk from Daniel Magalotti this conference



## *Conclusions*

- To exploit HL-LHC project potential, a new generation of tracking devices will be needed, able to provide high-resolution particle trajectories in real time and under unequalled experimental constraints as of today.
  - Providing Tracking data for the L1 stands out as a formidable challenge
  - The CMS Tracker next generation is still to be designed
    - The knowledge of the expected rates from realistic simulations are essential to design readout circuits and develop pattern recognition hardware.
    - The first simulation results presented today are already exploited as input for selective readout designs and pattern recognition technologies
- > Strong and combined efforts on R&D and simulations