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## A Low Mass On-chip Readout Scheme for Double-sided Silicon Strip Detectors

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B-factories like the KEK-B in Tsukuba, Japan, operate at relatively low energies and thus require detectors with very low material budget inside the sensitive volume in order to minimize multiple scattering. On the other hand, front-end chips with short shaping time like the APV25 have to be placed as close to the sensor strips as possible to avoid excessive noise, which is mainly caused by the capacitive load of the input amplifiers.

In order to achieve both - minimal material budget and low noise - we developed a readout scheme for double-sided silicon detectors, where the APV25 chips are placed on a single flexible circuit, which is glued onto the sensor. While the top-side strips are directly connected to the chips by wire-bonding and a small pitch adapter, those of the bottom-side are attached by two flexible circuits, which are bent around the edge of the sensor.

This so-called "Origami" design will be utilized to build the Silicon Vertex Detector of the future Belle II experiment, which will consist of 4 layers made from ladders with up to five double-sided silicon strip sensors in a row. Each ladder will be supported by two carbon fiber reinforced ribs, with a very light-weight Airex styrofoam core.

Placing the readout chip onto the sensor also requires sufficient cooling, which will be done by a highly efficient two-phase CO<sub>2</sub> system. Thanks to the Origami concept, all APV chips inside the active Volume are aligned in a row and thus can be cooled by a single thin cooling pipe per ladder.

We will present the concept and the assembly procedure of the Origami chip-on-sensor modules, and show results of beam tests which were performed at CERN on prototype modules.

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