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Development of high performance tracking layers as a sandwich of optimised CMOS pixel sensors

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We propose to enhance the performances of tracking layers by building a sandwich of low power time-integrating CMOS pixel sensors. Sensors equipping one side of the layer offer a high spatial resolution (few μm), while the sensors on the other side focus on the time resolution (few μs). The whole device targets a material budget lower than 0.5 % of X0.
We will present the in-beam test results of a double-sided ladder featuring 8 millions of pixels (18.4 × 18.4 μm2) read-out in 110 μs and an equivalent thickness of 0.6 % of X0, build by the PLUME collaboration. Plans to reach 0.3 % of X0 will also be discussed.
We will then review the development of CMOS pixel sensors with various optimisations with respect to the spatial or time resolution. Especially the road to reach a few microseconds read-out time, while maintaining the power budget at the few μW per pixel level will be described.
The conclusion will show possible implementation of these double-sided tracking layers.

Summary

See attached file.

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