Radiation-Hard/High-Speed Parallel Optical Engine

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Outline

- Introduction: compact solution for data transmission
- What has been achieved with 5 Gb/s VCSEL array driver
- Preliminary design for 10 Gb/s VCSEL array driver
- Can we do more intelligent things with 40 Gb/s VCSEL array driver?
- Summary

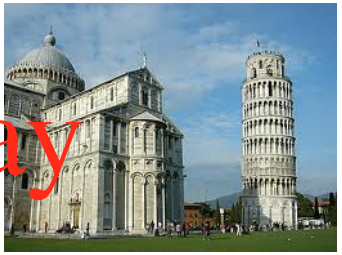
Vertical Cavity Surface Emitting Laser

- VCSELs are widely used in data transmission
  - available mostly with multi-mode transmission (850 nm)
  - available in 1, 4, or 12 channels
    - computer mouse uses single-channel VCSEL
  - array VCSELs in use for over ten years

Use of VCSEL Arrays in HEP

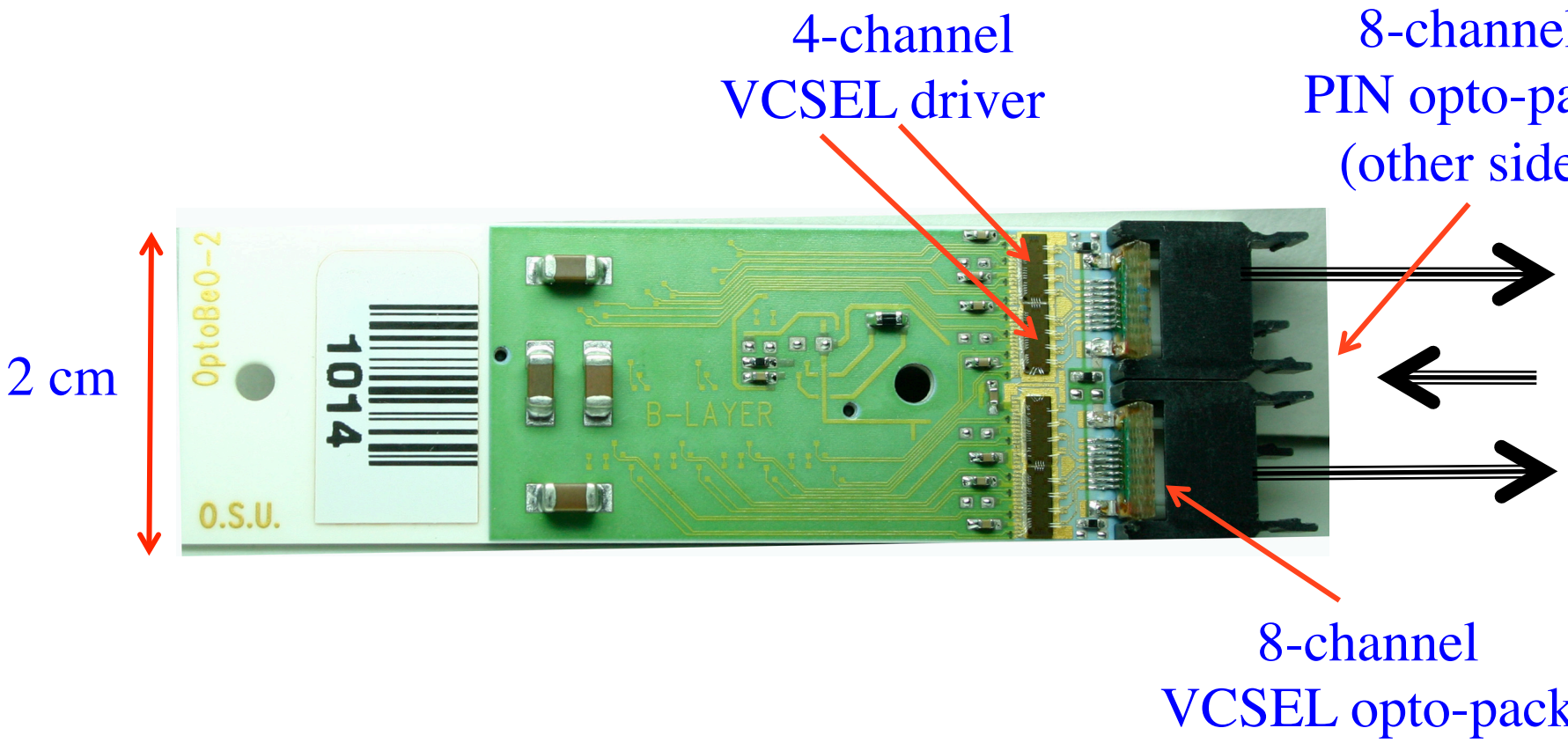
- Widely used in off-detector data transmission
- First on-detector implementation in ATLAS pixel detector
  - experience has been positive
    - VCSELs used are humidity sensitive but they are installed in very low humidity location
    - modern VCSELs are humidity tolerant
    - ⇨ will use arrays for next pixel detector upgrade (IBL)

Advantage of VCSEL Array



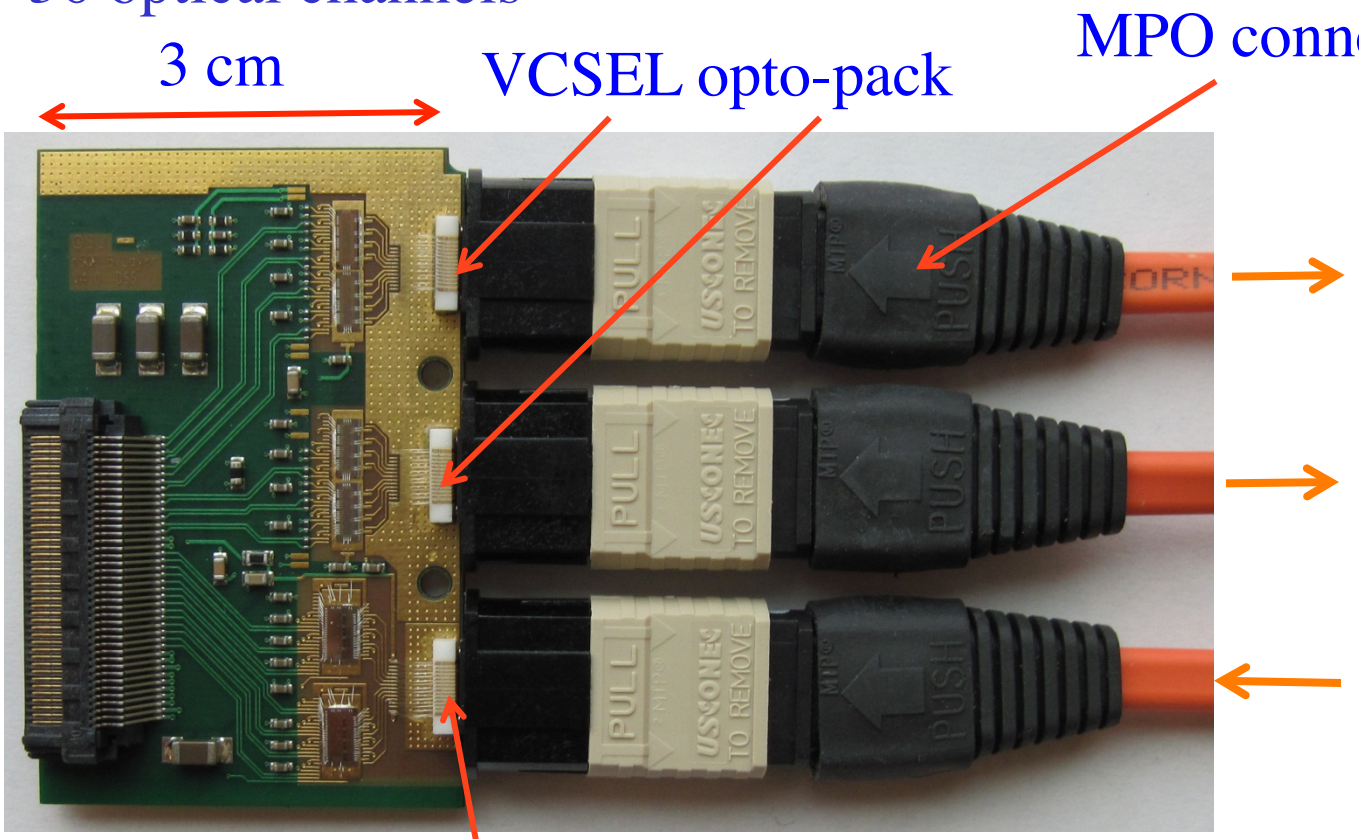
- highly compact with 250 μm between channels
- allow high-efficient implementation of redundancy
  - reserve 1 in 12 channels for redundancy instead of doubling the number of channels for single-channel device
- reduced service with one power supply to bias each array
  - single power supply for each PIN array
- fiber ribbon reduces the number of fibers to handle
  - fiber ribbon is less fragile than single-channel fiber
- greatly simplify production, testing, and installation
  - ATLAS: fabricated 272 opto-boards vs 2,000 opto modules
    - ⇨ will use arrays for next pixel detector upgrade (IBL)

Opto-Board (Parallel Optical Engine)



New Parallel Optical Engine

- Improved design for new pixel layer of ATLAS
  - use 12-channel VCSEL and PIN arrays
  - ⇨ 36 optical channels

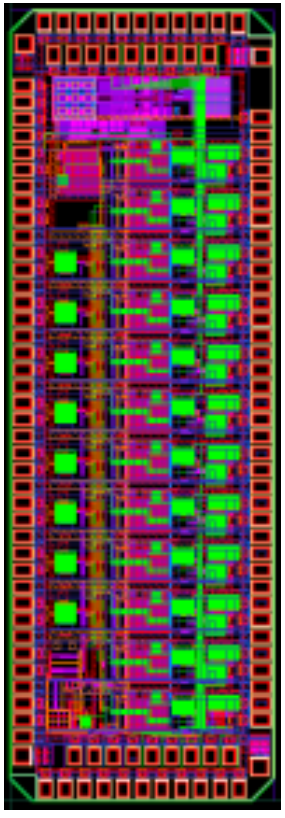


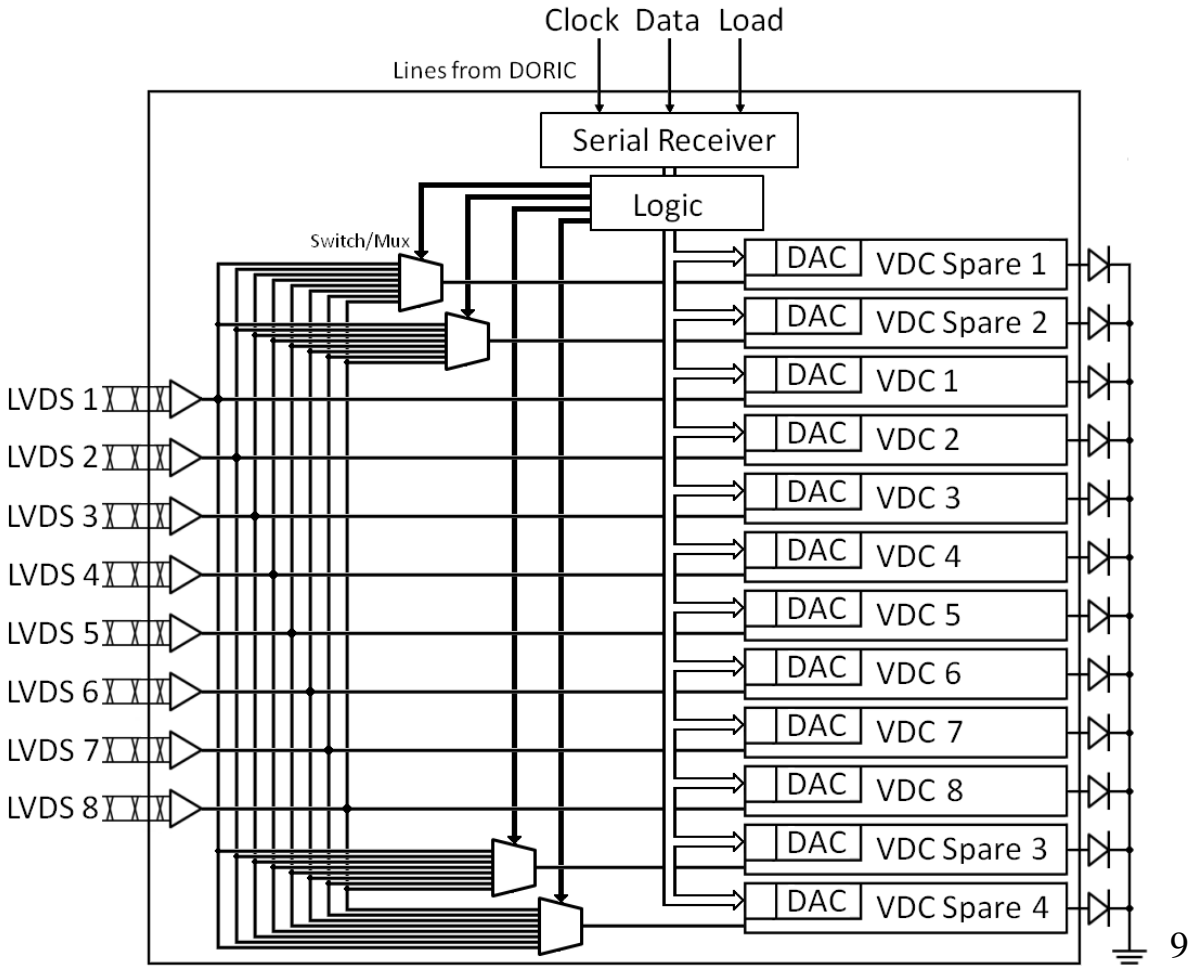
New 12-Channel VCSEL Driver

- New ASIC designed using 130 nm CMOS
- Incorporate improvements taking advantage of experience from 1st generation parallel optical engine:
  - redundancy to bypass a broken VCSEL
    - special thanks to FE-I4 group (Roberto Beccherle et al.) for command decoder circuit
  - power-on reset in case of communication failure:
    - no signal steering
    - 10 mA modulation current (on current)
    - 1 mA bias current (off current)
- Will only operate at 160 Mb/s for new pixel layer but design ASIC to operate at much higher speed (5 Gb/s) to gain experience in designing high-speed parallel driver
- Array R&D compatible w/GBT is an approved ATLAS R&D project

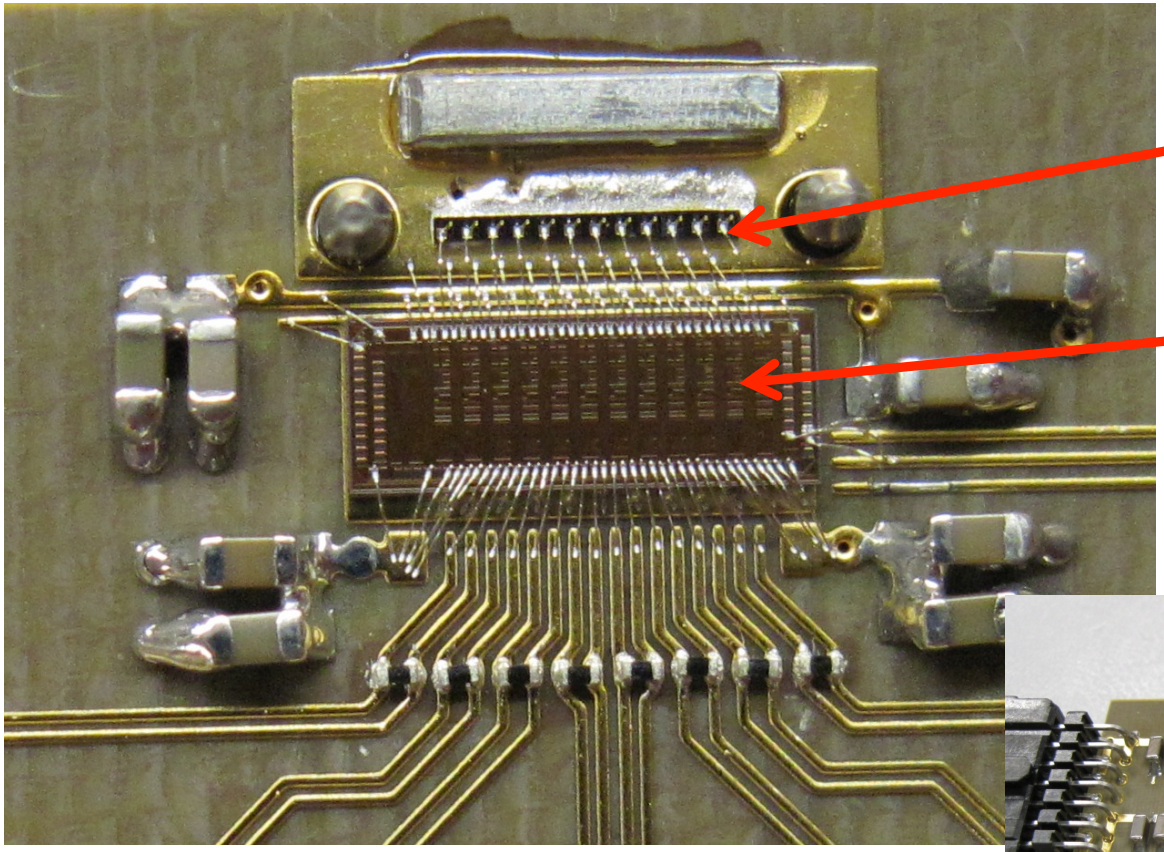
New VCSEL Array Driver

- Only inner 8 channels connected to new pixel modules
  - future driver should reserve only one channel for redundancy





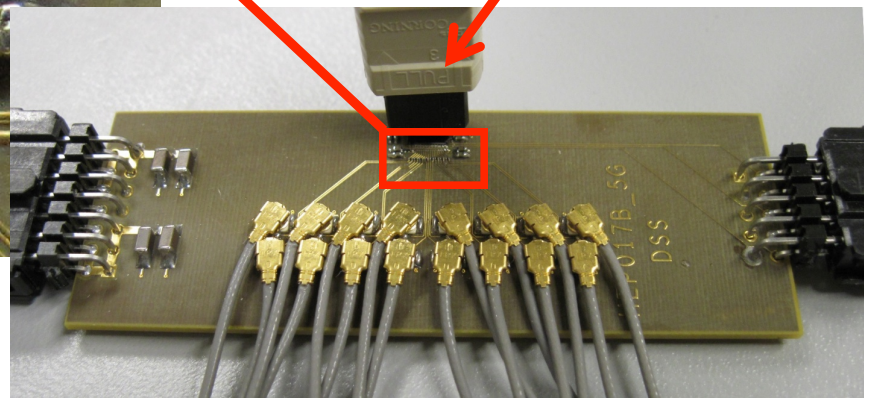
High-Speed Test Configuration



10 Gb/s ULM
VCSEL array

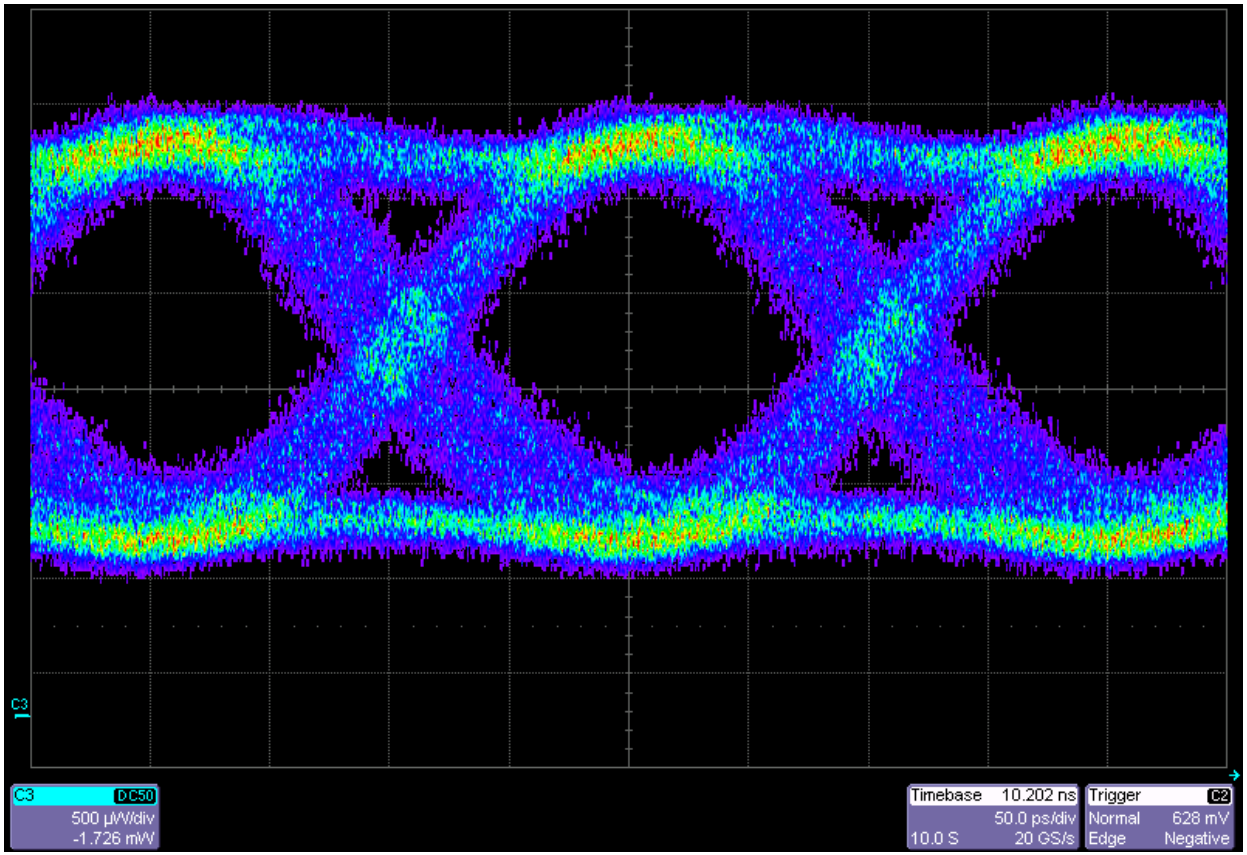
VCSEL
array driver

MPO connector

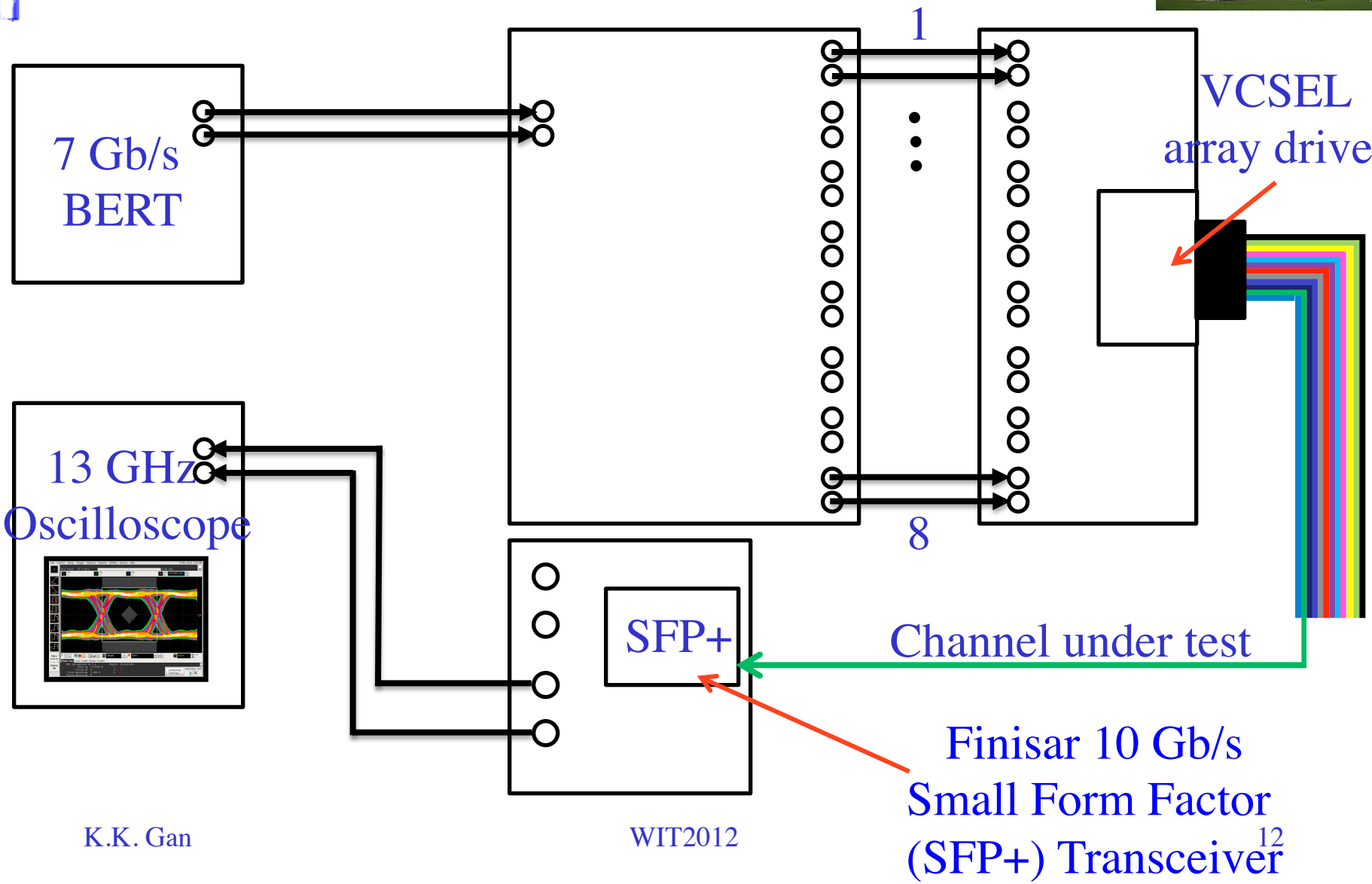


Optical Eye Diagram

- Difficult to judge eye diagram with 4.5 GHz optical probe…

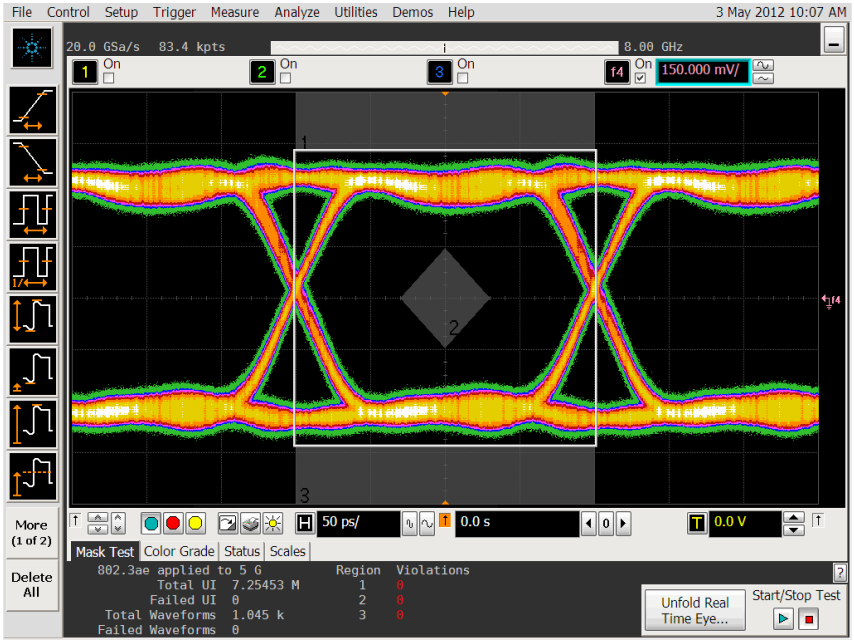


SFP+ as Optical Probe

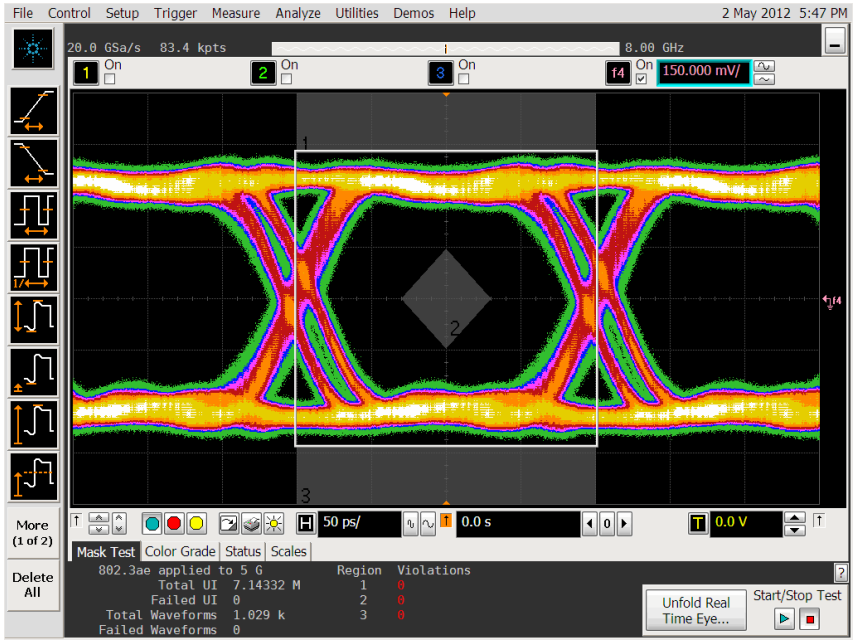


SFP+ Loopback vs VCSEL Driver

10 Gb/s SFP+ transceiver @ 5 Gb/s
with optical loopback

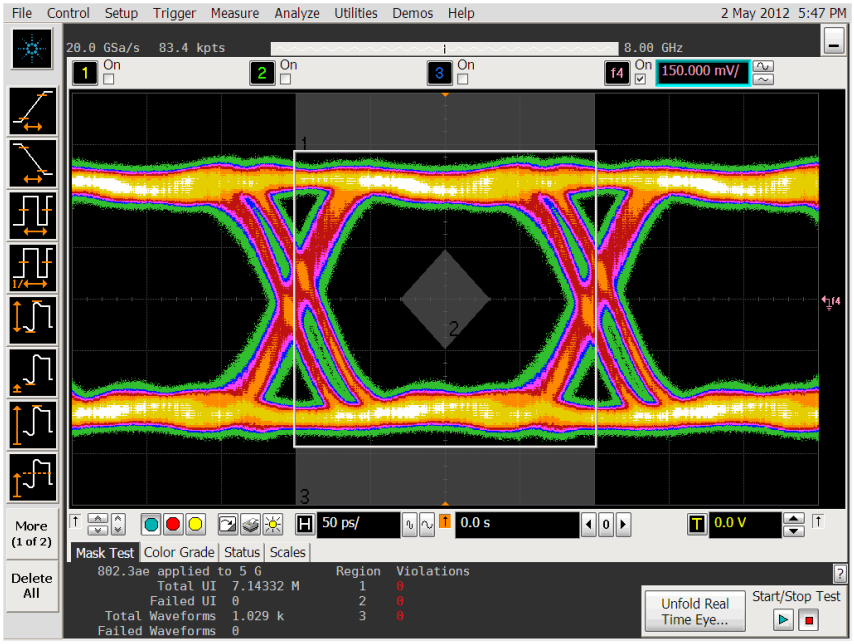


VCSEL driver @ 5 Gb/s
after 10 Gb/s SFP+ receiver

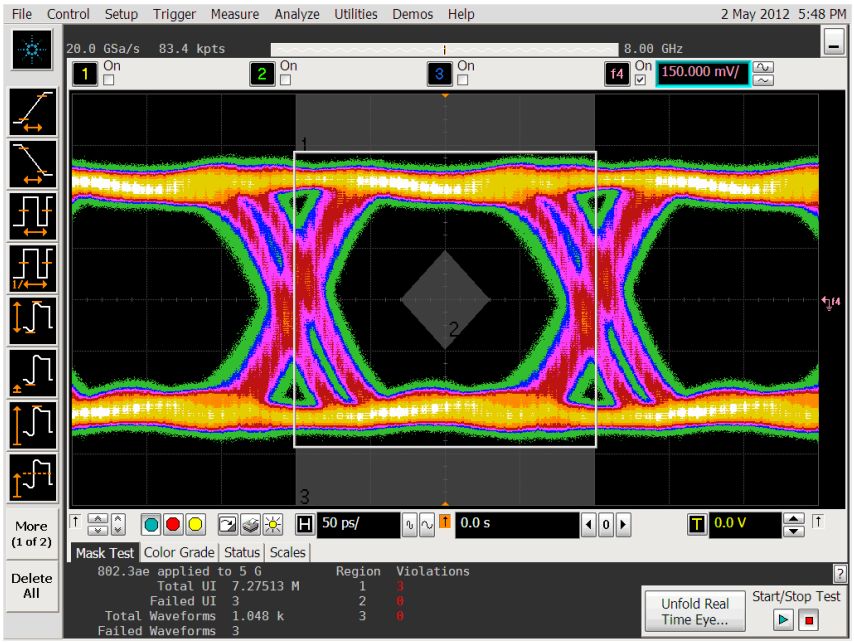


Eye with One/All Channels Active

One channel active



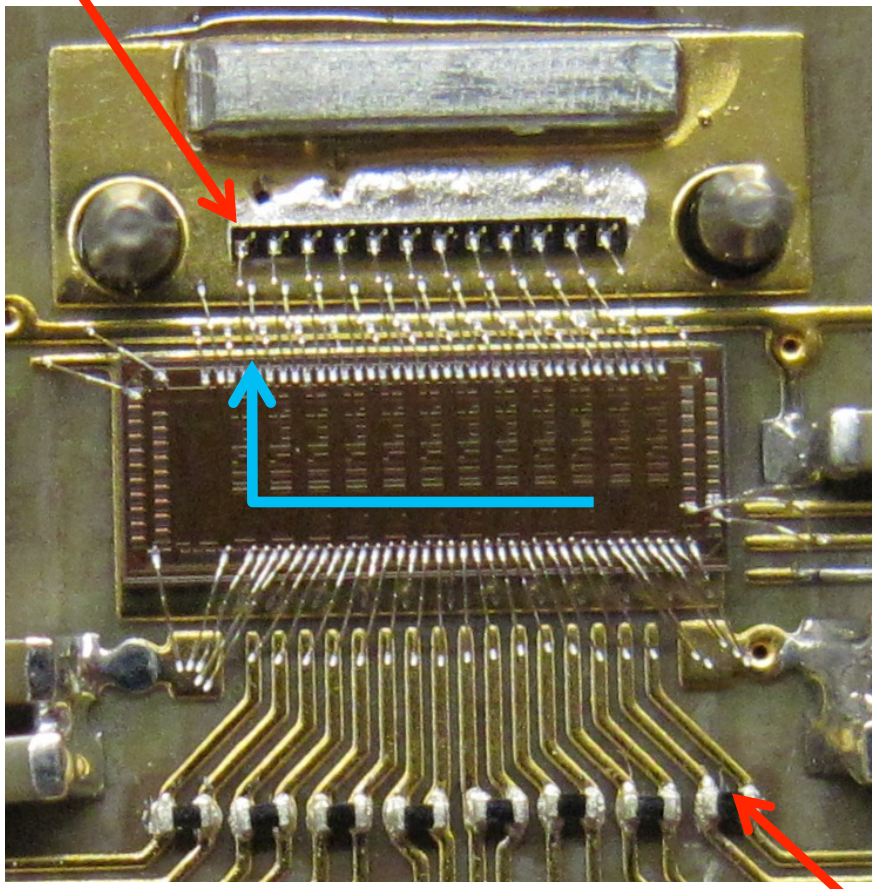
All channels active



- all channels work @ 5 Gb/s with bit error rate < 5×10^{-13} for all channels active
- jitter increases with all channels active but still passes the mask test

Effect of Steering on Eye

VCSEL spare 1

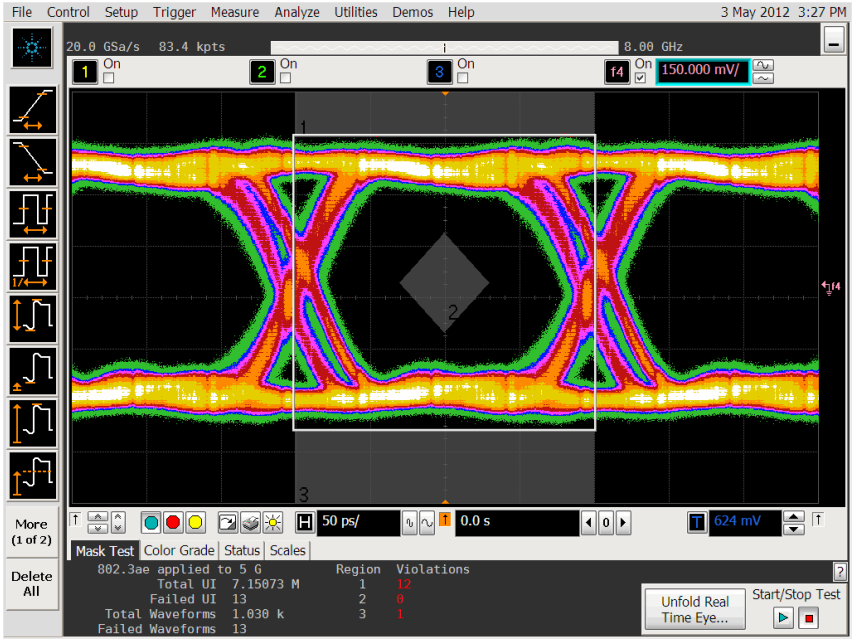


Receiving LVDS signal from channel 8, steering to VCSEL spare 1

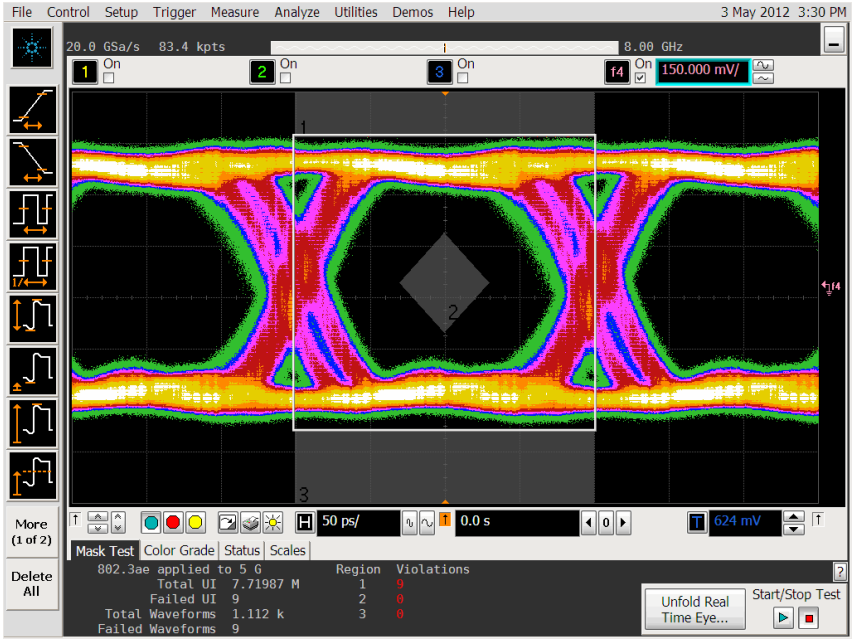
LVDS in channel 8

Effect of Steering on Eye

Spare 1 output with other channels off



Spare 1 output with all channels active

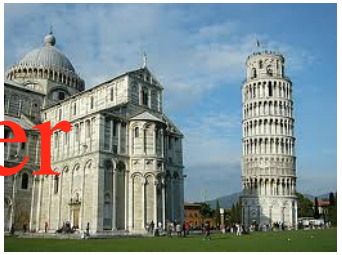


- steered channel still passes the mask test
  - jitter increases with all channels active

Radiation Hardness

- 10 Gb/s VCSEL arrays have been proven to be radiation hard to tens of Mrad
  - send signal on ~1 m micro co-ax cables to less radiation and more serviceable location
- Radiation hardness of VCSEL array driver will be verified in the summer

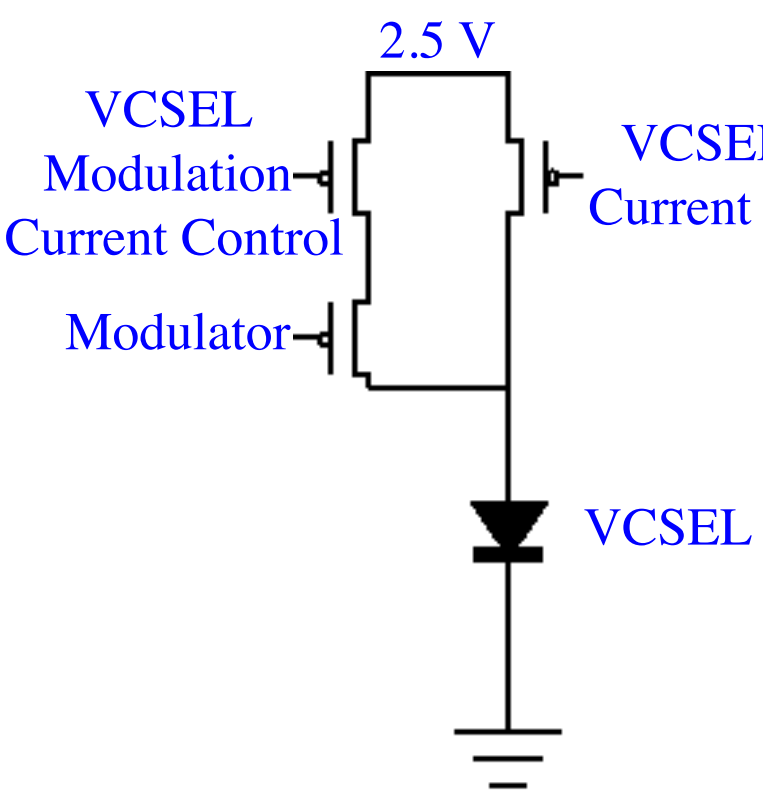
Toward 10 Gb/s Array Driver



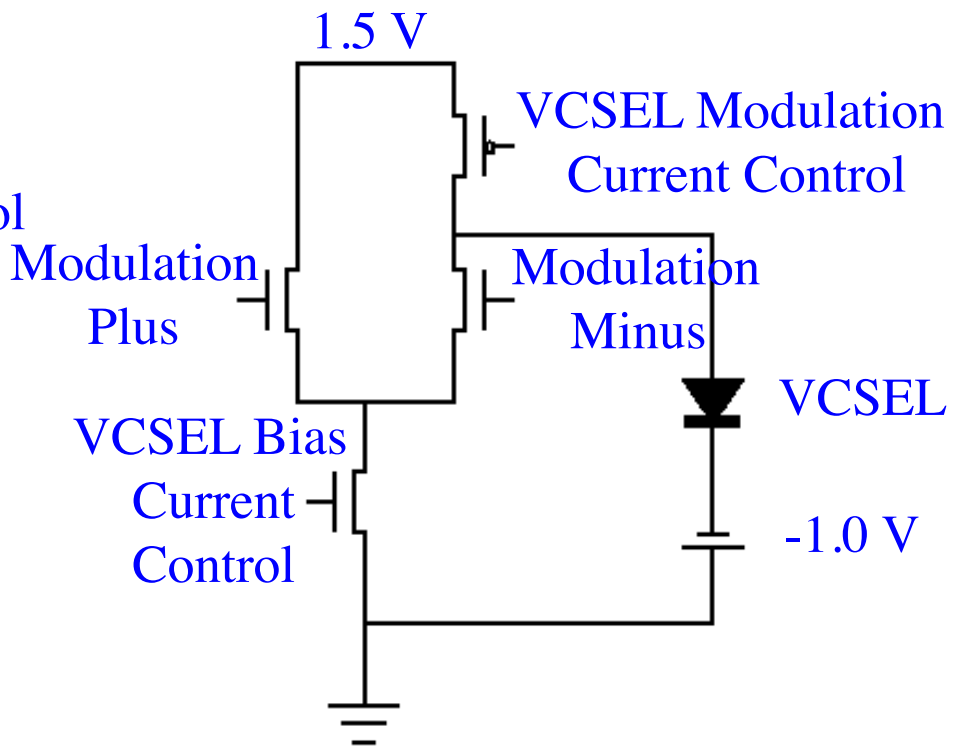
- 10 Gb/s transmission needed
  for ATLAS inner pixel layer and LAr readout upgrades
- joint ATLAS/CMS proposal funded
  via US DOE generic R&D program

Improved 130 nm VCSEL Array Driver

Existing design
(thick oxide FETs)



New preliminary design
(thin oxide FETs)



10 Gb/s Simulation Results

Use VCSEL model with bond pads + parasitics

- new design works better but need more simulations + layout
- plan to work with 65 nm CMOS/130 nm BiCMOS if 130 nm CMOS proves to be too marginal

40 Gb/s VCSEL Array Driver?

- Vertical Integration Systems now offers 40 Gb/s VCSEL array
  - ⇨ 0.5 Tb/s in 12-channel fiber ribbon
  - ⇨ what kind of more intelligent things can we do with this much higher bandwidth?

Summary

- VCSEL array offers compact solution to data transmission
- 5 Gb/s VCSEL array driver successfully prototyped
- have preliminary design for 10 Gb/s VCSEL array driver
  - much faster VCSEL array now available