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Radiation-Hard and High-Speed Parallel Optical Engine

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Parallel optical engine allows a compact design for high-speed data transmission. The design is enabled by the readily available high-speed VCSEL arrays. With the use of a 12-channel array operating at 10 Gb/s per channel, a parallel optical engine can deliver an aggregated bandwidth of 120 Gb/s. With the spacing of 250 mm between two VCSELs, the width of a VCSEL array is only 3 mm. This allows the fabrication of rather compact parallel optical engine for installation at a location where space is at a premium. We have designed an ASIC for use in a parallel optical engine for a new layer of the ATLAS pixel detector for the initial phase of the LHC luminosity upgrade. The ASIC is a 12-channel driver of a VCSEL array for operation up to 5 Gb/s. The ASIC is designed using a 130 nm CMOS process to enhance the radiation-hardness. A redundancy scheme has also been implemented to allow the bypass of a broken VCSEL. We have received the ASIC and the performance up to 5 Gb/s is satisfactory. We are able to program the ASIC to bypass a broken VCSEL. The power-on reset circuit is also successfully implemented which sets the ASIC to a default configuration with no signal steering. In addition, we are able to set the drive current in individual channels. We plan to port the design to the 130 nm SiGe BiCMOS process in order to operate at 10 Gb/s for an aggregated bandwidth of 120 Gb/s and some preliminary results of the design will be presented.

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