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Quadruple well CMOS MAPS for particle tracking with pixel-level analog processing, discrimination and time stamping

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In the last decade, the use of standard deep submicron CMOS technologies for the implementation of monolithic active pixel sensors for HEP experiments has been thoroughly investigated. One of the main issues with this approach is the fact that the charge collection efficiency may be negatively affected by the presence of competitive N-wells used to integrate PMOS transistors in the readout chain. These N-wells act as parasitics collecting electrodes subtracting part of the charge generated by a minimum ionizing particle (MIP) from the sensor. On the other hand, PMOS transistors are needed to design high performance, low power analog and digital blocks.
A novel approach for isolating the PMOS competitive N-wells is based on the use of a planar 180 nm CMOS process with quadruple well called INMAPS. By means of an additional processing step, an high energy deep P-well implant is deposited beneath the N-wells (except for the N-well diodes acting as collecting electrodes). This implant creates a barrier for the charge diffusing in the epitaxial layer, preventing it from being collected by the positively biased N-wells of the in-pixel circuits and allowing a theoretical charge collection efficiency of 100%. The NMOS transistors are designed in heavily doped P-wells located over a lightly P-doped epitaxial layer about 10 μm thick, which has been grown upon a relatively low resistivity substrate. The epitaxial layer, featuring a higher resistivity than both the deep P-well and the substrate, also plays an important role in the improvement of the charge collection properties: in fact, the presence of two small potential barriers (deep P-well/epitaxial layer or P-well/epitaxial layer and epitaxial layer/substrate) keeps the carriers within the epitaxial layer, preventing them from diffusing through the substrate. The foundry provides two different typologies of epitaxial layer: standard resistivity (about 50 Ω·cm) and high resistivity (1 kΩ·cm). Two lots of chips called Apsel4well differing for the resistivity of the epitaxial layer, have been fabricated (and delivered at the beginning of 2012). Comparing the charge collection efficiency of the two different approaches will be possible to further investigate the role played by the epitaxial layer resistivity on this performance.
The Apsel4well pixel features a 50 μm pitch, complying with the requirements of the SVT Layer0 of the SuperB experiment. The collecting electrode consists of 4 interconnected N-well square diodes each with a 1.5 μm side. The sensor is read out by a classical channel for capacitive detectors including a charge preamplifier, a shaper and a threshold discriminator, followed by the in-pixel readout logic. Other than analog smaller (3x3) pixel matrices and single channels, the Apsel4well chip also includes a 32x32 matrix which implements a sparsified readout architecture with time stamping in order to deal with the large amount of data expected in the experiments at the high luminosity colliders.

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