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# A Fast Hardware Tracker for the ATLAS Trigger System

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Selecting interesting events with triggering is very challenging at the LHC due to the busy hadronic environment. Starting in 2014 the LHC will run with an energy of 14TeV and instantaneous luminosities which could exceed 10^34 interactions per cm^2 per second. The triggering in the ATLAS detector is realized using a three level trigger approach, in which the first level (L1) is hardware based and the second (L2) and third (EF) stage are realized using large computing farms.

It is a crucial and non-trivial task for triggering to maintain a high efficiency for events of interest while suppressing effectively the very high rates of inclusive QCD processes, which constitute mainly background. At the same time the trigger system has to be robust and provide sufficient operational margins to adapt to changes in the running environment. In the current design, track reconstruction can be performed only in limited regions of interest at L2 and the CPU requirements may limit this even further at the highest instantaneous luminosities.

Providing high quality track reconstruction over the entire detector volume for the L2 trigger decision would allow gains in efficiency and background rejection for triggers on tau leptons, b-hadrons and help reduce the luminosity dependence of isolation requirements for electrons and muons. The Fast Track Trigger (FTK) is an ongoing upgrade project aimed at providing track reconstruction over the |eta|<2.5 region using the silicon microstrip and pixel detectors. Pattern recognition and track fitting are executed in a hardware system utilizing massive parallel processing and achieve a tracking performance close to that of the global track reconstruction. The FTK system's design, based on a mixture of advanced technologies (FPGAs, ASICs, Associative Memories), and expected physics performance will be presented.

## Summary

A track reconstruction system for the trigger of the ATLAS detector at the Large Hadron Collider is described. The Fast Tracker is a highly parallel hardware system designed to operate at the Level-1 trigger output rate. It will provide high-quality tracks reconstructed over the entire inner detector by the start of processing in the
Level-2 trigger. The system is based on associative memories for pattern recognition and fast FPGA's for track reconstruction. Its design and expected performance under instantaneous luminosities up to 3x10^34/cm2^/s are discussed.

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