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The new variable resolution Associative Memory for Fast Track finding

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We describe a VLSI processor for pattern recognition based on Content Addressable Memory (CAM) architecture,
optimized for on-line track finding in high-energy physics experiments.
We have developed this device using 65 nm technology combining a full custom CAM cell with standard-cell control logic.
The customized design maximizes the pattern density, minimizes the power consumption and implements the functionalities needed for the planned Fast Tracker, an ATLAS trigger upgrade project at LHC.
We introduce a new variable resolution pattern matching technique using "don't care"bits to set the pattern-matching
window for each pattern and each layer can be independently.

Authors: ANNOVI, Alberto (Istituto Nazionale Fisica Nucleare (IT)); STABILE, Alberto (Università degli Studi e INFN Milano (IT)); CRESCIOLI, Francesco (Sezione di Pisa (IT)); Dr VOLPI, Guido (Istituto Nazionale Fisica Nucleare (IT)); SACCO, Ilaria (University of Heidelberg); BERETTA, Matteo Mario (Istituto Nazionale Fisica Nucleare (IT)); DELL'ORSO, Mauro (Dipartimento di Fisica); GIANNETTI, Paola (Sezione di Pisa (IT)); Prof. LIBERALI, Valentino (Università degli Studi di Milano)

Presenter: ANNOVI, Alberto (Istituto Nazionale Fisica Nucleare (IT))

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