CBC2: a strip readout ASIC with coincidence logic for trigger primitives at HL-LHC

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Outline

-Module and data readout for Phase-II upgrade of CMS Outer Tracker

-From CBC to CBC2

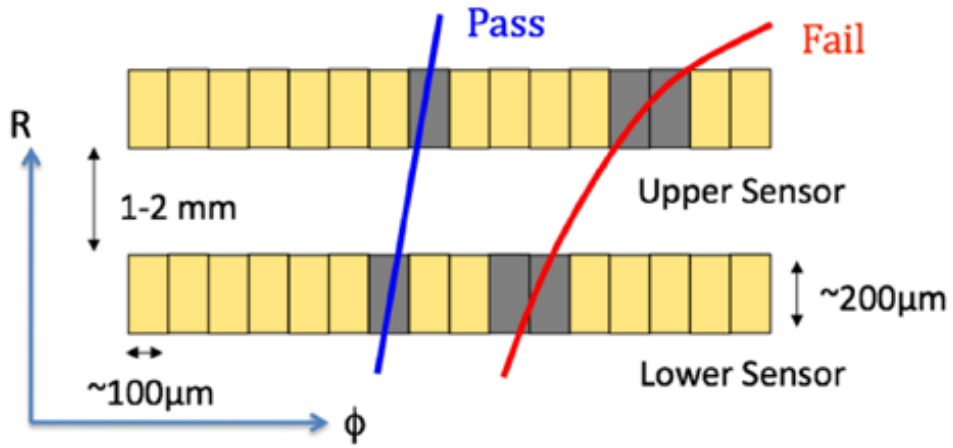
-CBC2 architecture

-CBC2 Stub-finding logic

-Status of the design

-Future plans and conclusions

P_T Discrimination in Outer Tracker



CBC2 to correlate hits on two closely separated sensors to discriminate between high and low PT tracks

-no t*racklets*, only *stubs*!

-works in φ (not z)

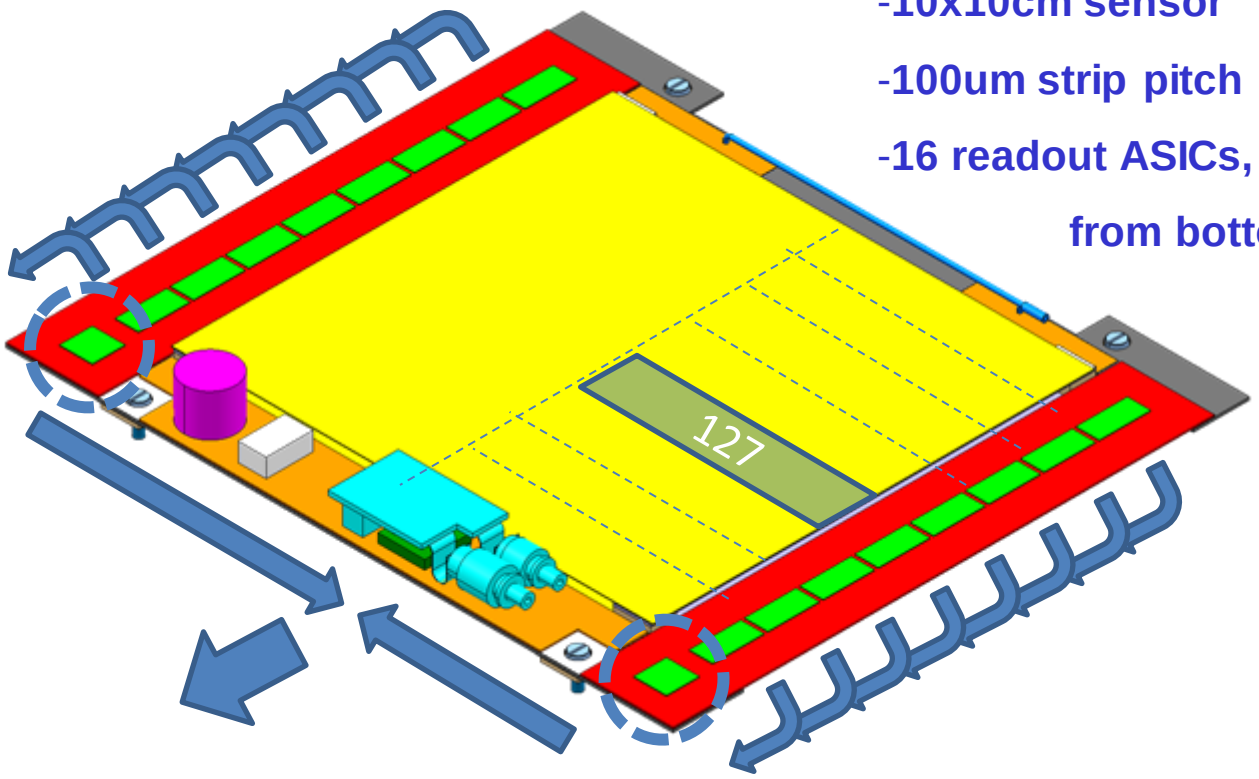
-Simple algorithm:

1- clustering on top and bottom sensors (1D clustering)

2- after clusterization, for every hit on inner sensor look for a valid hit\cluster on a coincidence window on outer sensor

3- if there is any, then the inner sensor hit is considered a *stub*

2S (Strip-Strip) Module



2S (Strips-Strips) module for outer tracker:

-10x10cm sensor

-100um strip pitch

-16 readout ASICs, each reading 127 strips from bottom sensor and 127 from top sensor

-2 "Concentrator" ASIC

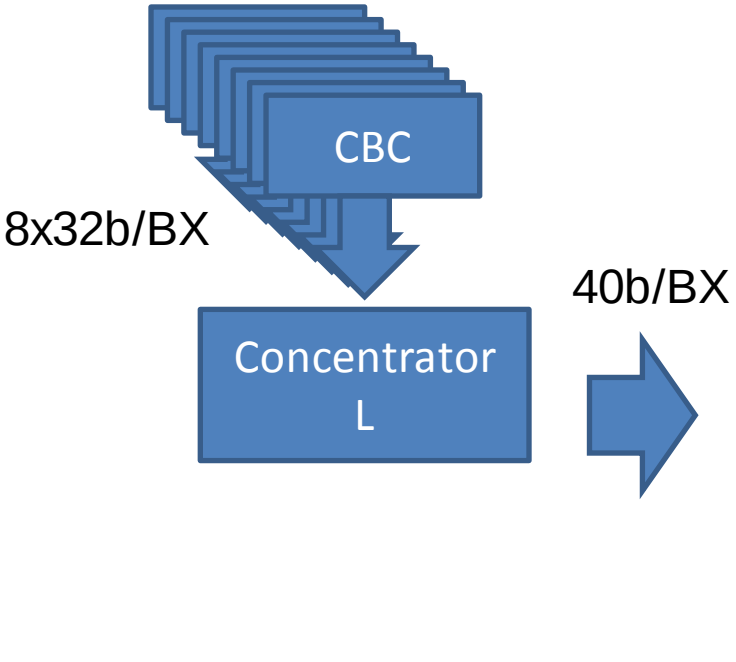
-1 low-power GBT

Compare to Strip-Pixel module for inner tracker - D.Abbaneo:

"A hybrid module architecture for a prompt momentum discriminating tracker at HL-LHC"

Module Readout

Final readout scheme still under investigation (e.g. sparsified vs unsparsified)



One proposal:

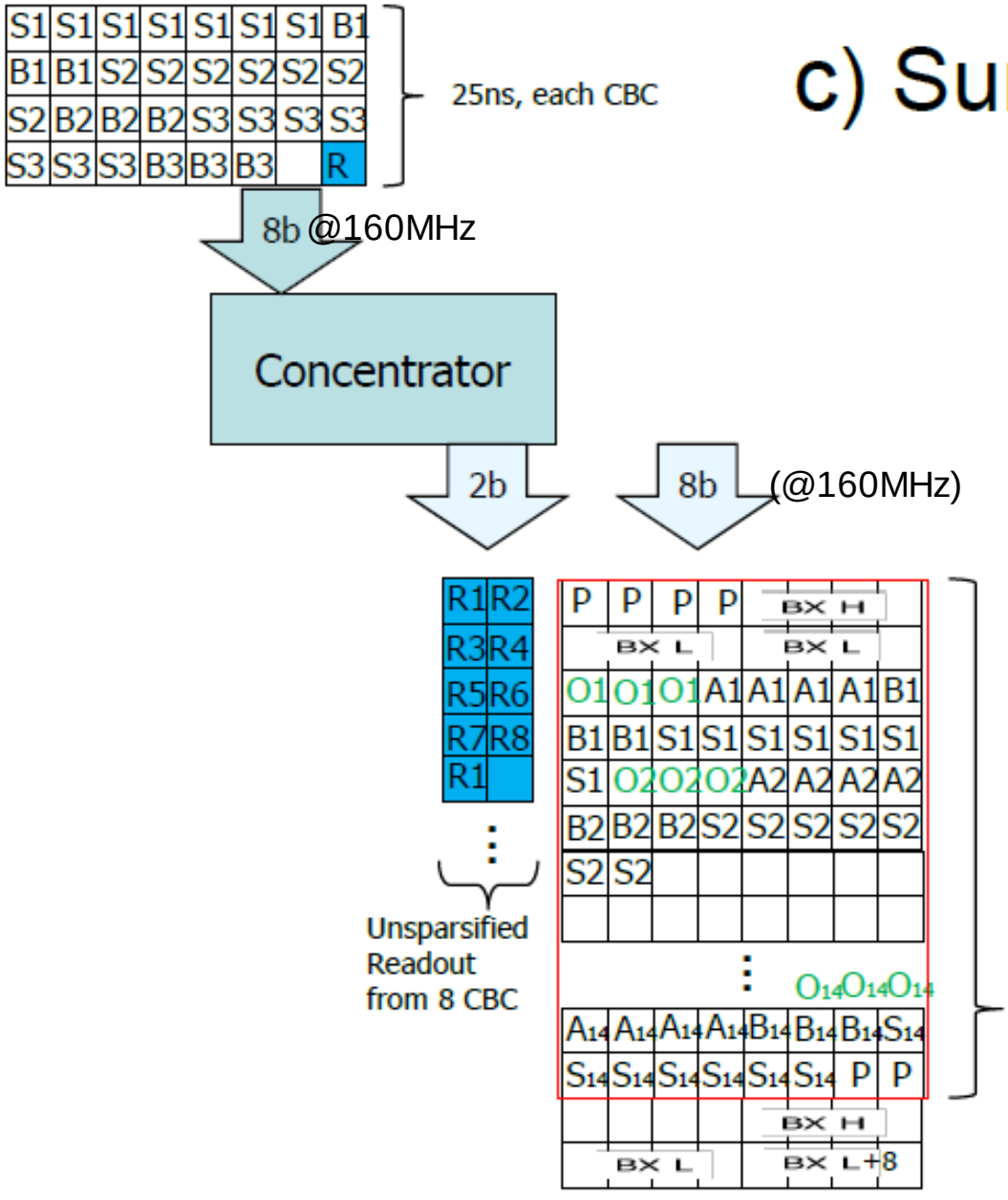
- unsparsified readout
- up to 3 track-stubs per Bx per CBC

- Block synchronous transfer of trigger data
- Block size: 8Bx = 256 bits
- Capable of transmitting up to 14 stubs per 8 Bx per half module
- Synchronicity is maintained
- Latency remains fixed

L1 readout binary data: fully synchronous unsparsified.

Trigger data: coincidence hits are transferred to a shift register and read out at 1b/BX as a test feature for the coincidence logic.

c) Summary

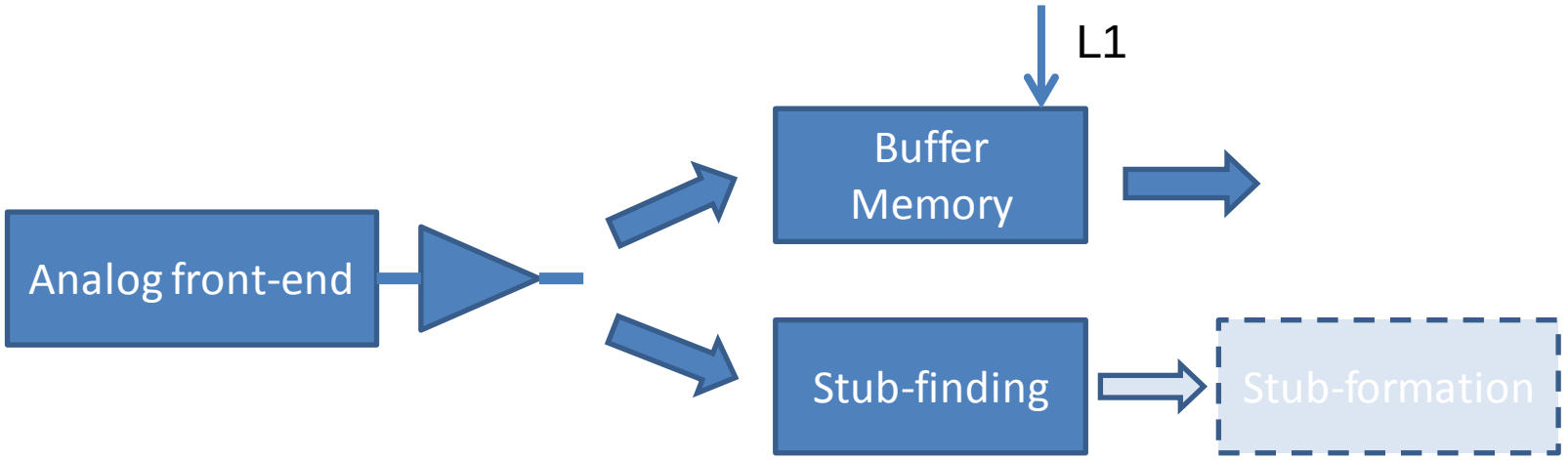


Bit field	Symbol	#b
L1 Readout	R	1b
CBC Address	A	4b
Strip Address	S	7b
Bend	B	3b
Bunch Crossing	BX	12
BX offset	O	3b
Parity and Synchronization	P	

		Trigger	L1 Readout
CBC output	Sync	3stub/BX	Unsparsified
Concentrator output	Block sync	1.9stubs/BX sustained	Unsparsified
		14stubs/8BX Max	

From F.Vasey:
Electronic System for 2S-Pt modules System Architecture and Data Formats, CMS Tk Week

CBC2 Readout



Data readout still an open issue (and with it the Concentrator ASIC)

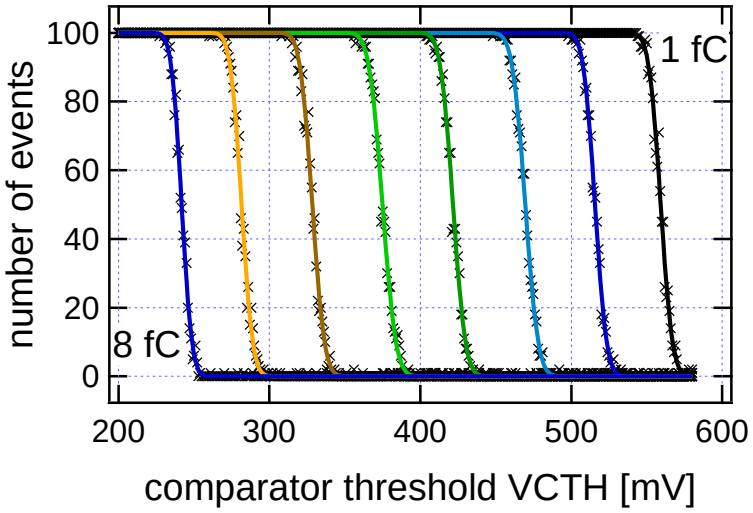
To make progress with prototype development CBC2 addresses stub finding logic and other hardware issues and leaves stubs-encoding and readout.

L1 readout binary data: fully synchronous unsparsified.

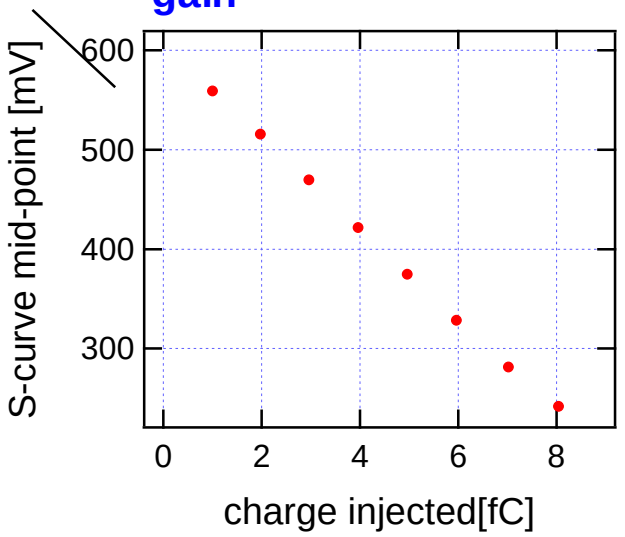
Trigger data: coincidence hits are transferred to a shift register and read out at 40MHz as a test feature for the coincidence logic.

CBC (1) Test Results

s- curves for range 1 - 8 fC : 1 fC steps



gain

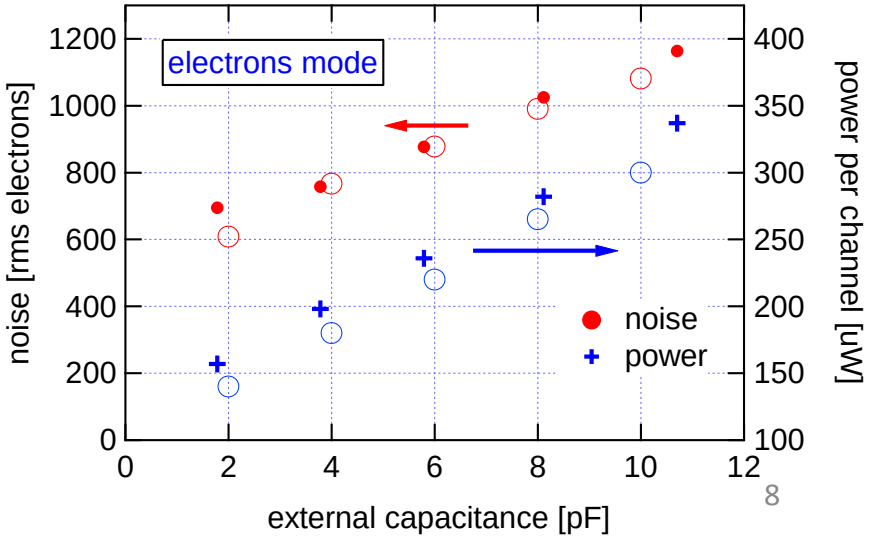


e.g. for 5pF input capacitance:

noise: ~ 800 e_{RMS}

total power: < 300 µW/channel

Noise and power



see M.Pesaresi:

"The CBC microstrip readout chip for LHC phase II"

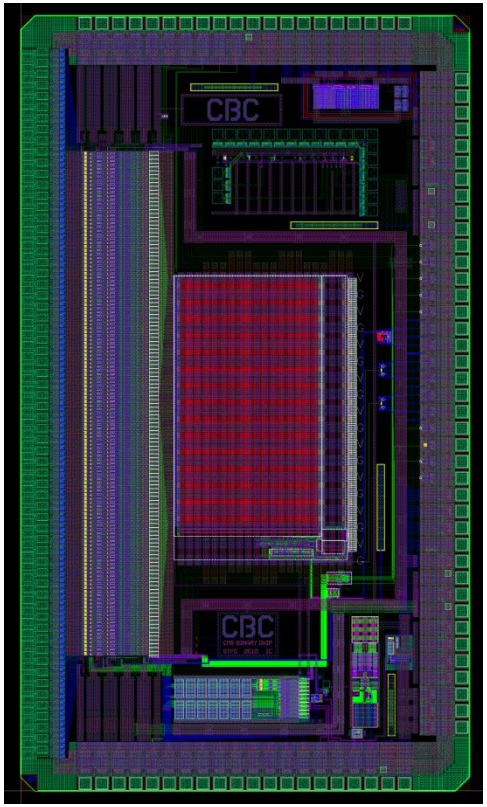
CBC(1) -> CBC2

Features kept:

- L1 triggered readout
- Powering features (DC-DC and LDO)

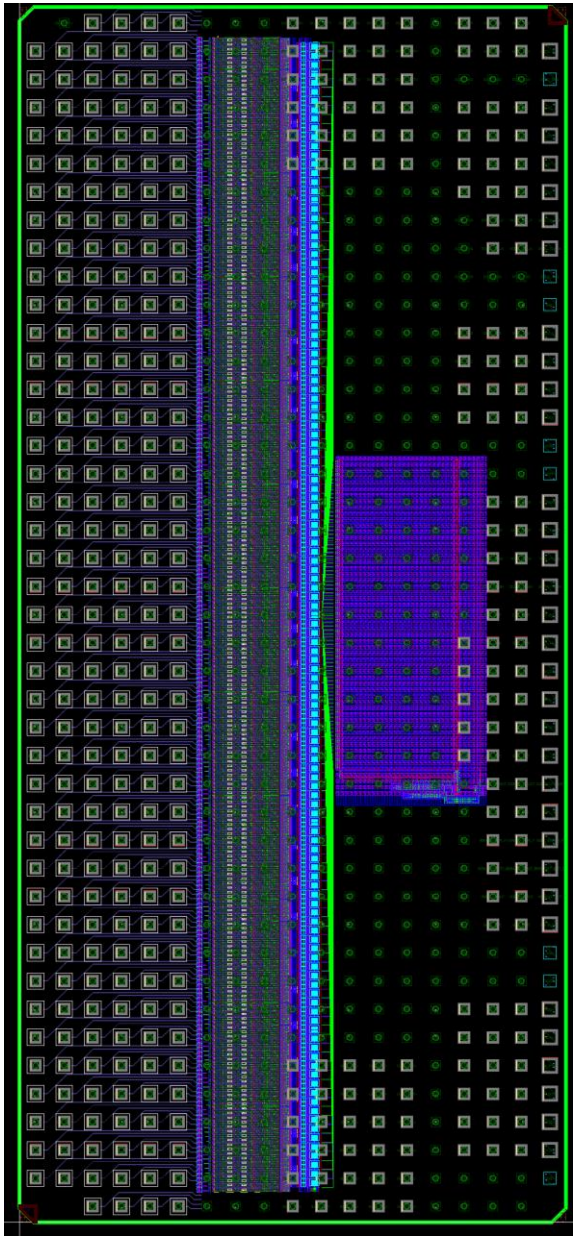
New features:

- 250um C4 bump-bonding
- 254 channels (not 256): allows correlation between 127 strips on top and bottom sensors (one spare code for no-hit)
- Correlation logic for stub formation
- Test pulse circuit
- Works for consecutives triggers

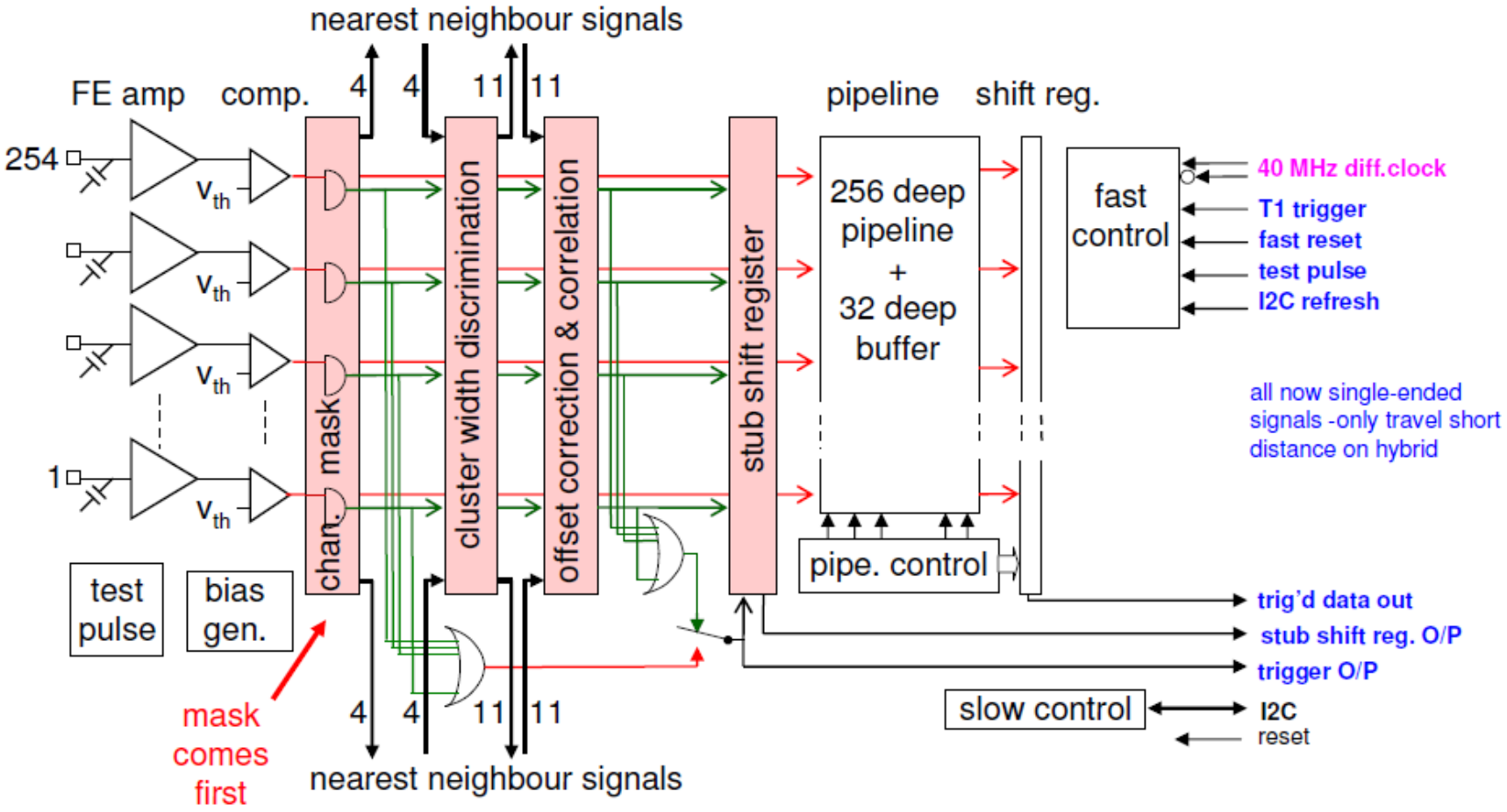


CBC
128 channels
wirebond: 50 um pitch
7mm x 4mm

CBC2
254 channels
C4 bump-bond: 250 um pitch
10.75mm x 4.75mm



CBC2 Architecture



blocks associated with Pt stub generation

channel mask: block noisy channels (but not from pipeline)

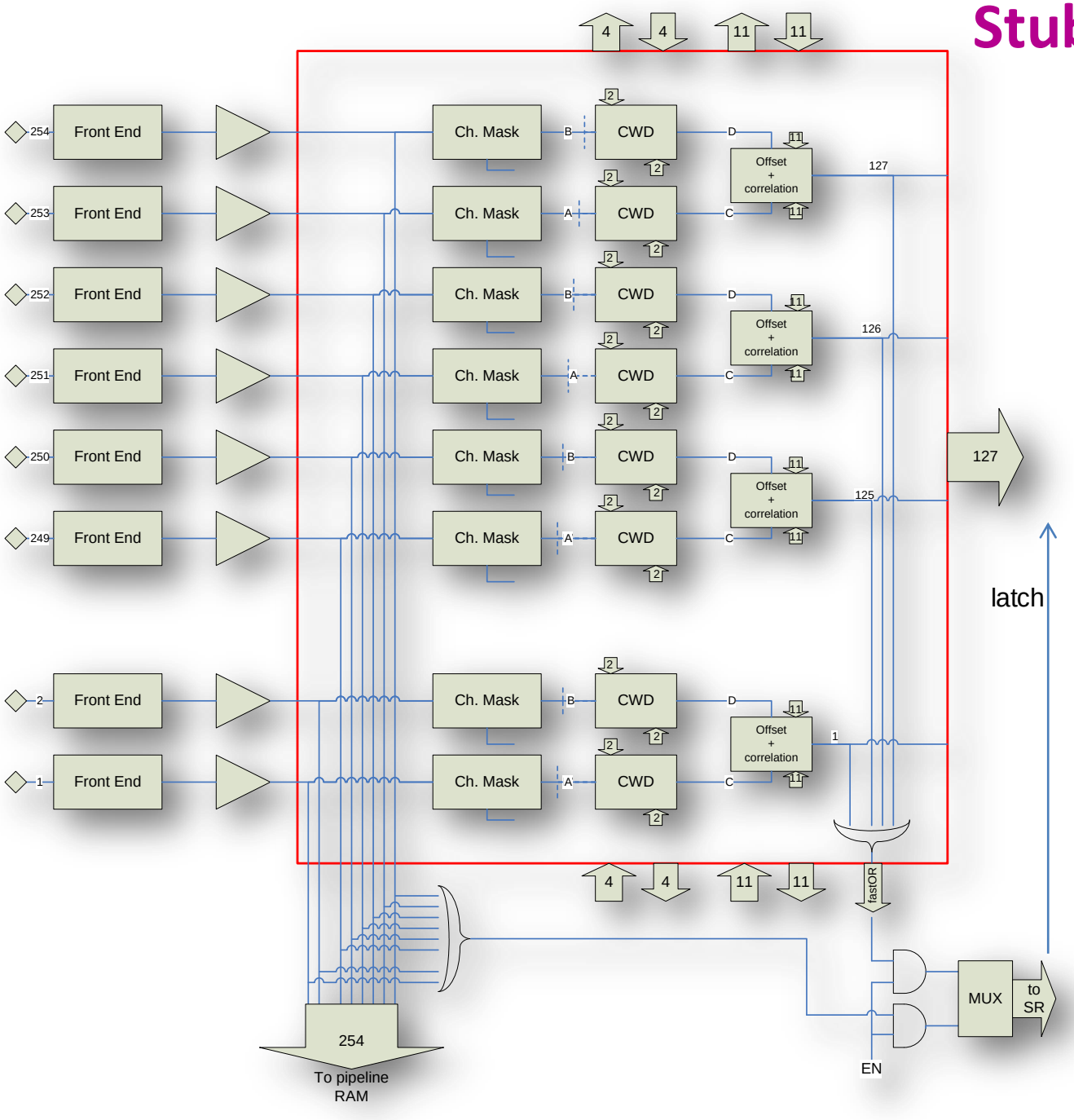
cluster width discrimination: exclude wide clusters

offset correction and correlation: correct for phi offset across module and correlate between layers

stub shift register: test feature - shift out result of correlation operation at 40 MHz

fast OR at comp. O/P and correlation O/P: - can select either to transmit off-chip for normal operation choose correlation O/P

Stub finding Logic



Individual mask for noisy channels
→254b from I2C reg.
(can be also used to inhibit coincidence logic)

Need to be able to inhibit stub shift register operation
→1b EN from I2C reg.

254-OR of channel outputs to signal any activity on chip

127-OR of stubs to control the stubs SR readout

neighbour chip signals - CWD O/Ps

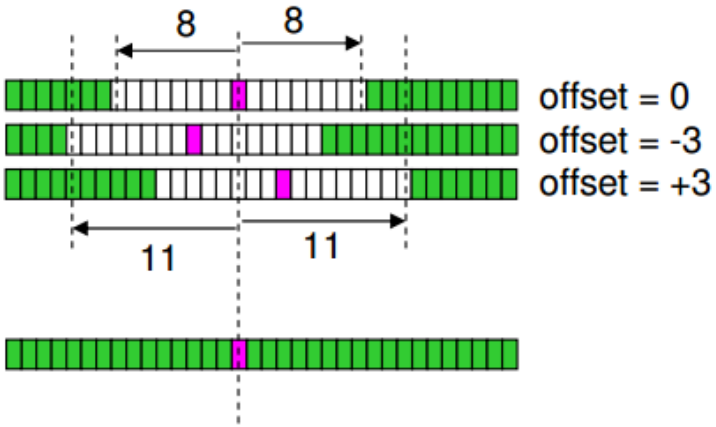
need programmability of **offset** and **window** width for upper layer channels to correlate with hit in inner layer

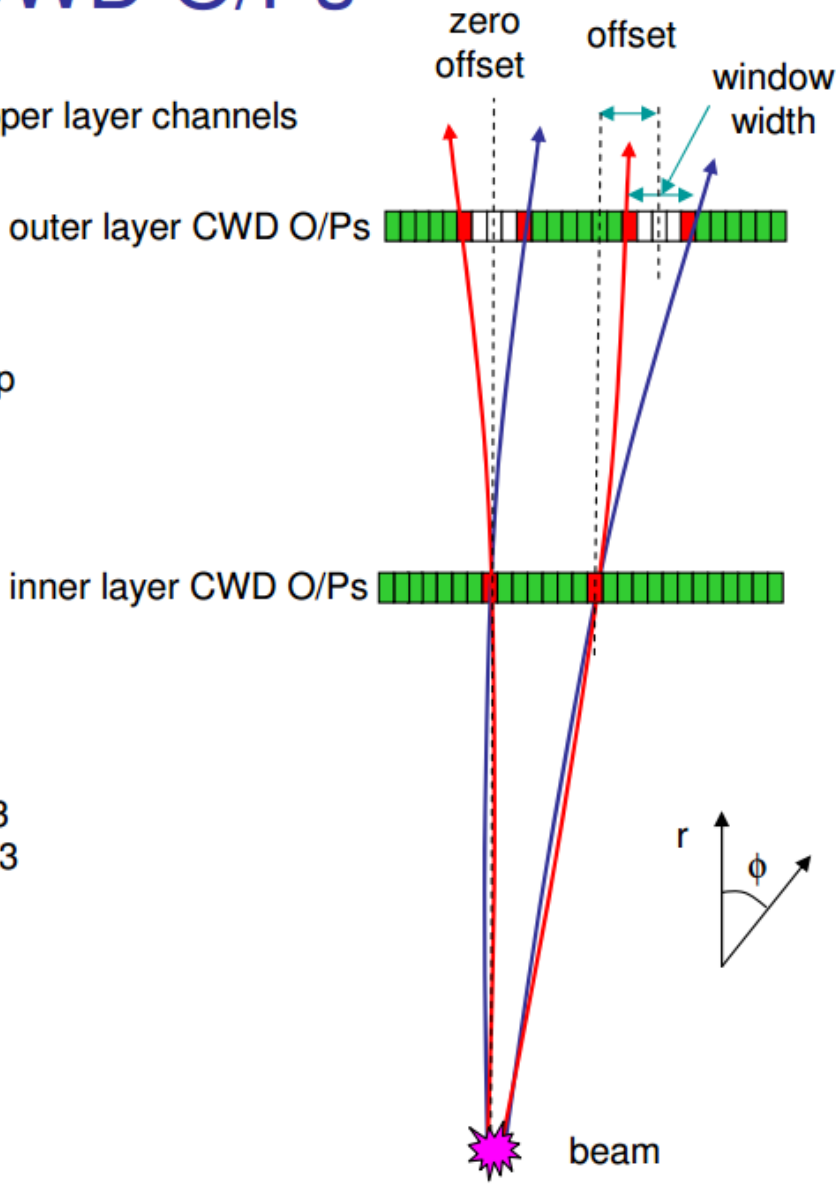
window defines Pt cut
width programmable up to **+/- 8** channels

offset defines lateral displacement of window across chip
programmable up to **+/- 3** channels

=> 11 signals to transmit to neighbouring chip
11 to receive from neighbouring chip

= 22 signals



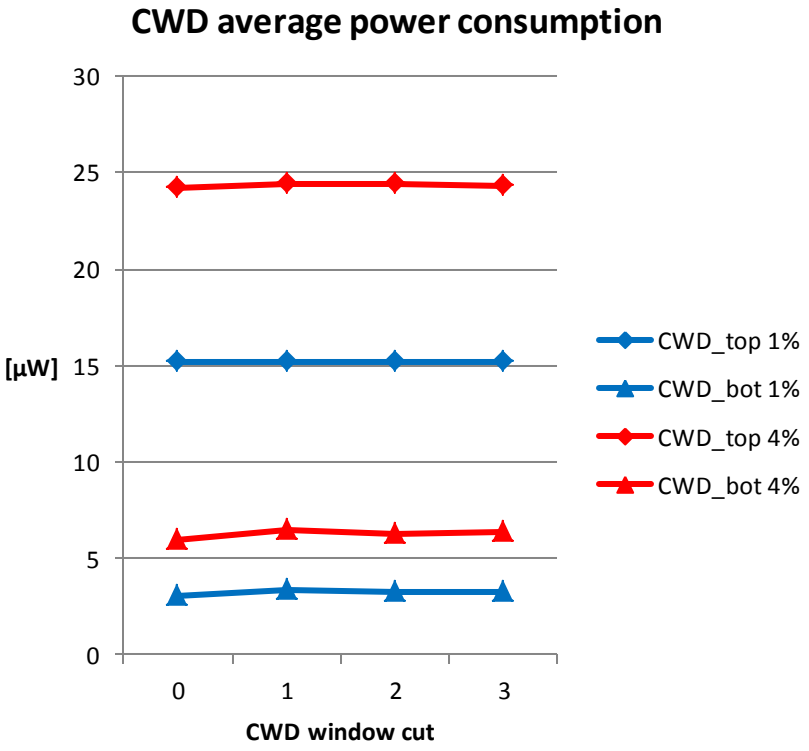


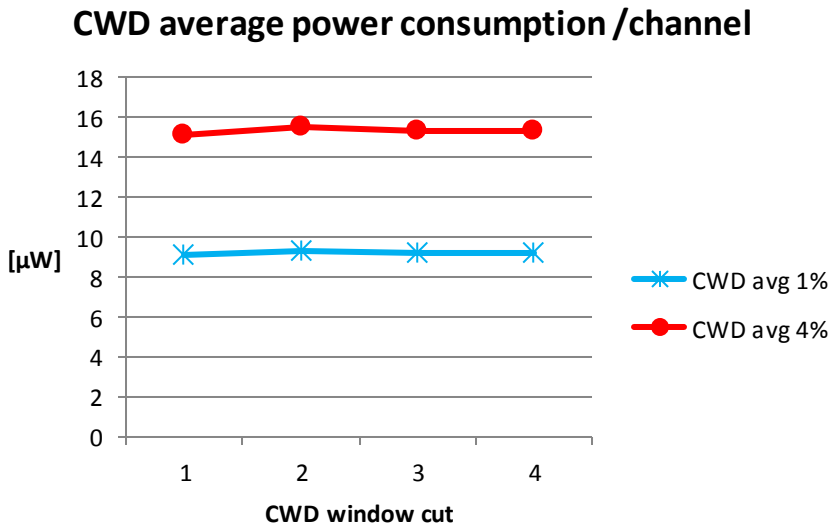
adding comp O/Ps -> 30 signals altogether, top and bottom of chip

Logic power consumption

NB: small study (~600 stubs). Occupancy:

- Inner sensor uncorrelated=0.8%
- Outer layer uncorrelated=0.8%
- Stubs in +-10 strips window=1.6%
-"hard" stubs +-3 coincidence window=1.6%

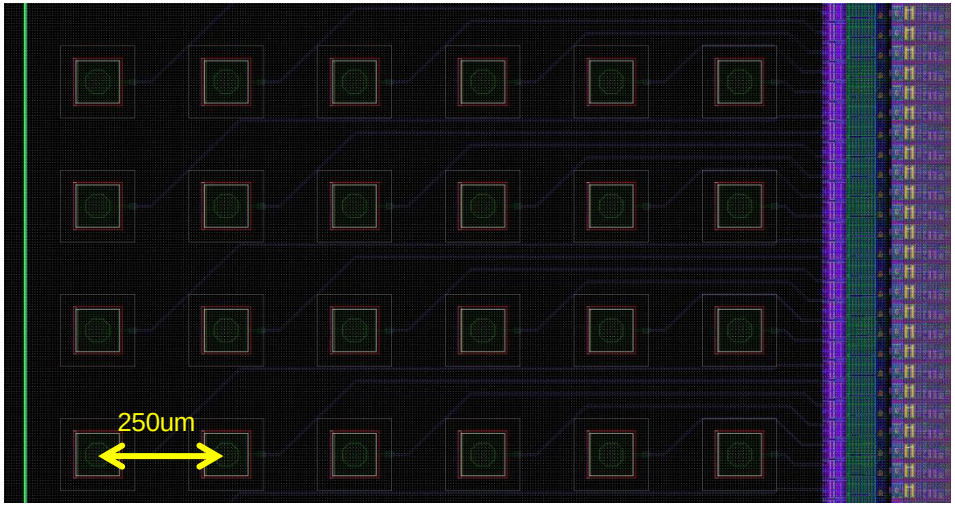




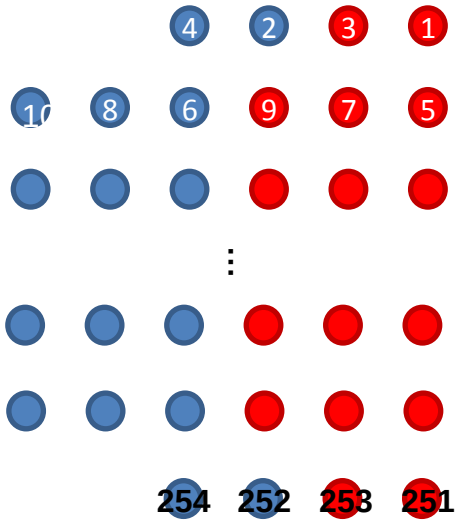
Coincidence logic and φ-shift correction: ~10uW/channel

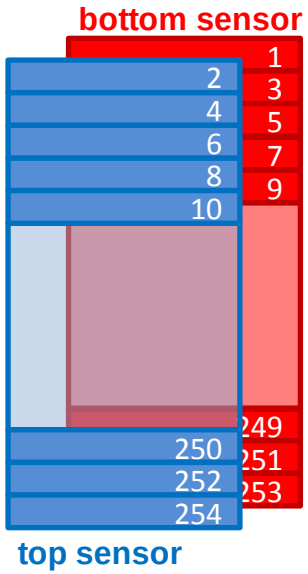
Total additional power: <50uW/channel

Input Pads



Input pads arranged in rows of 6 because of constraint in the routing of tracks on the hybrid



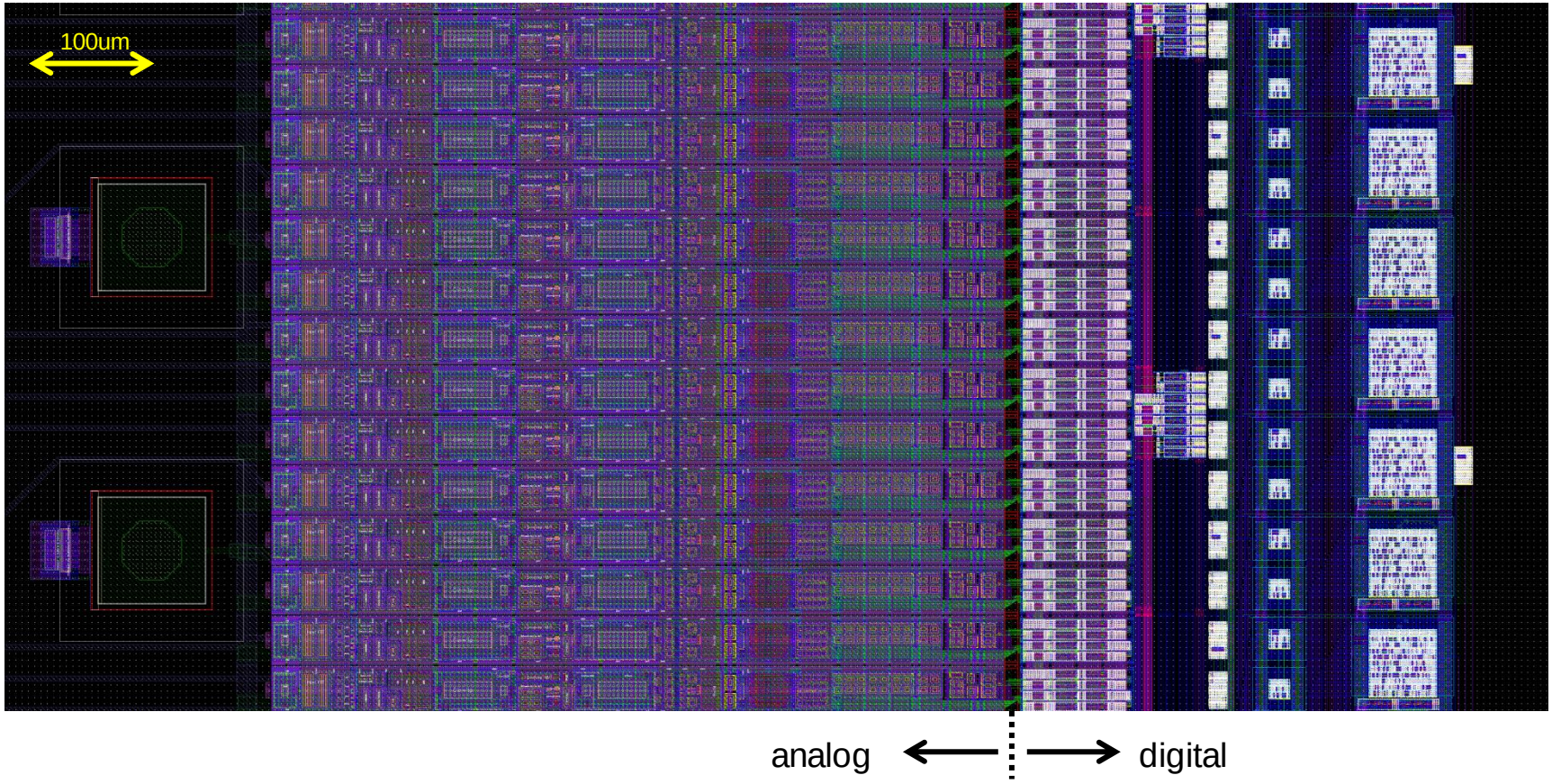


Hybrid footprint:

Inputs from top sensor

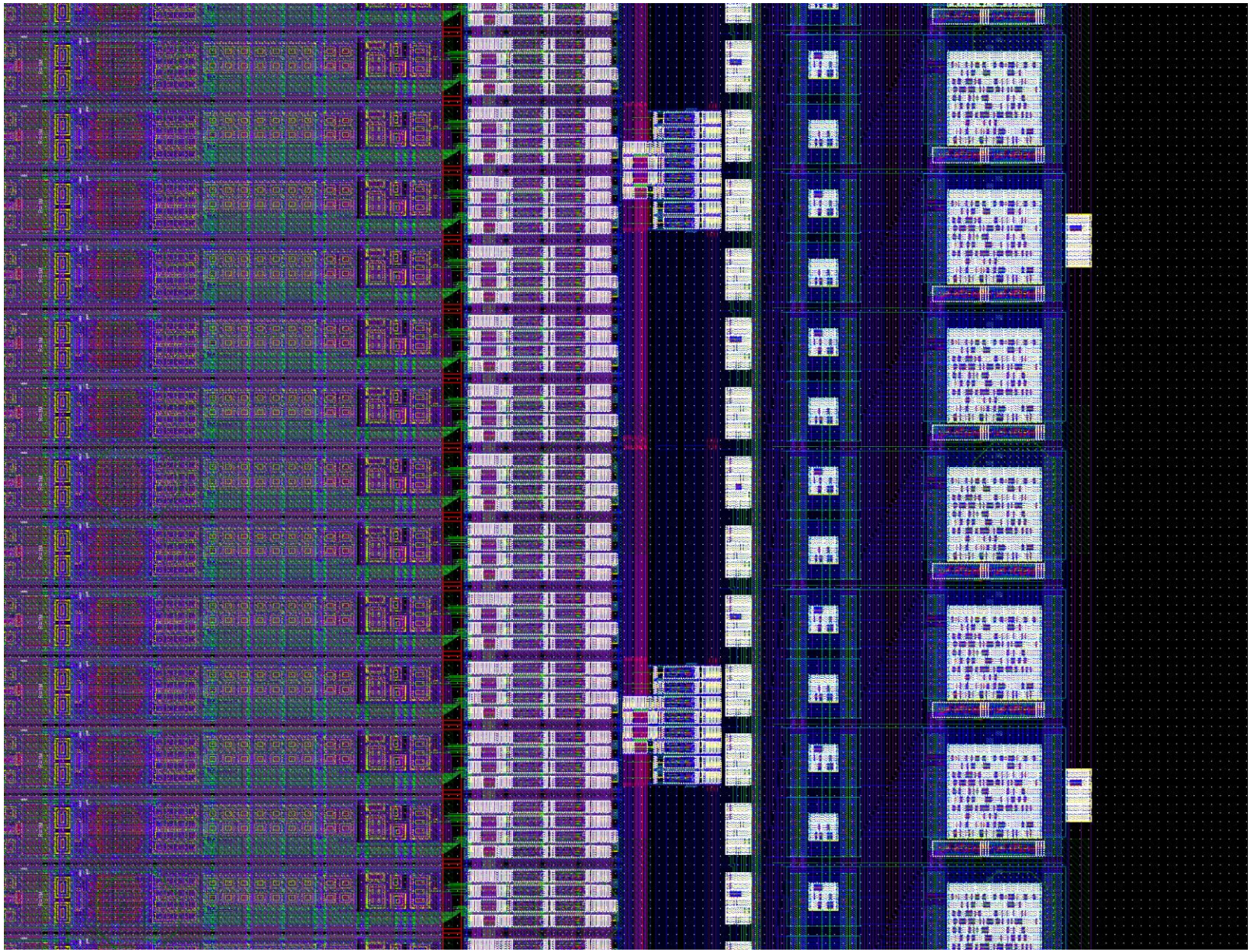
Inputs from bottom sensor

Channel layout



- **Power distribution optimized (made use of wider pitch)**
- **Postamplifier feedback network bias: local buffer to avoid effect of CM shift (additional ~5uW/channel)**
- **Comparator: internal hysteresis to solve drive issue of previous resistive network**

Digital part - Detail



Digital part - Detail

• Comparator offset register:
use refreshed registers

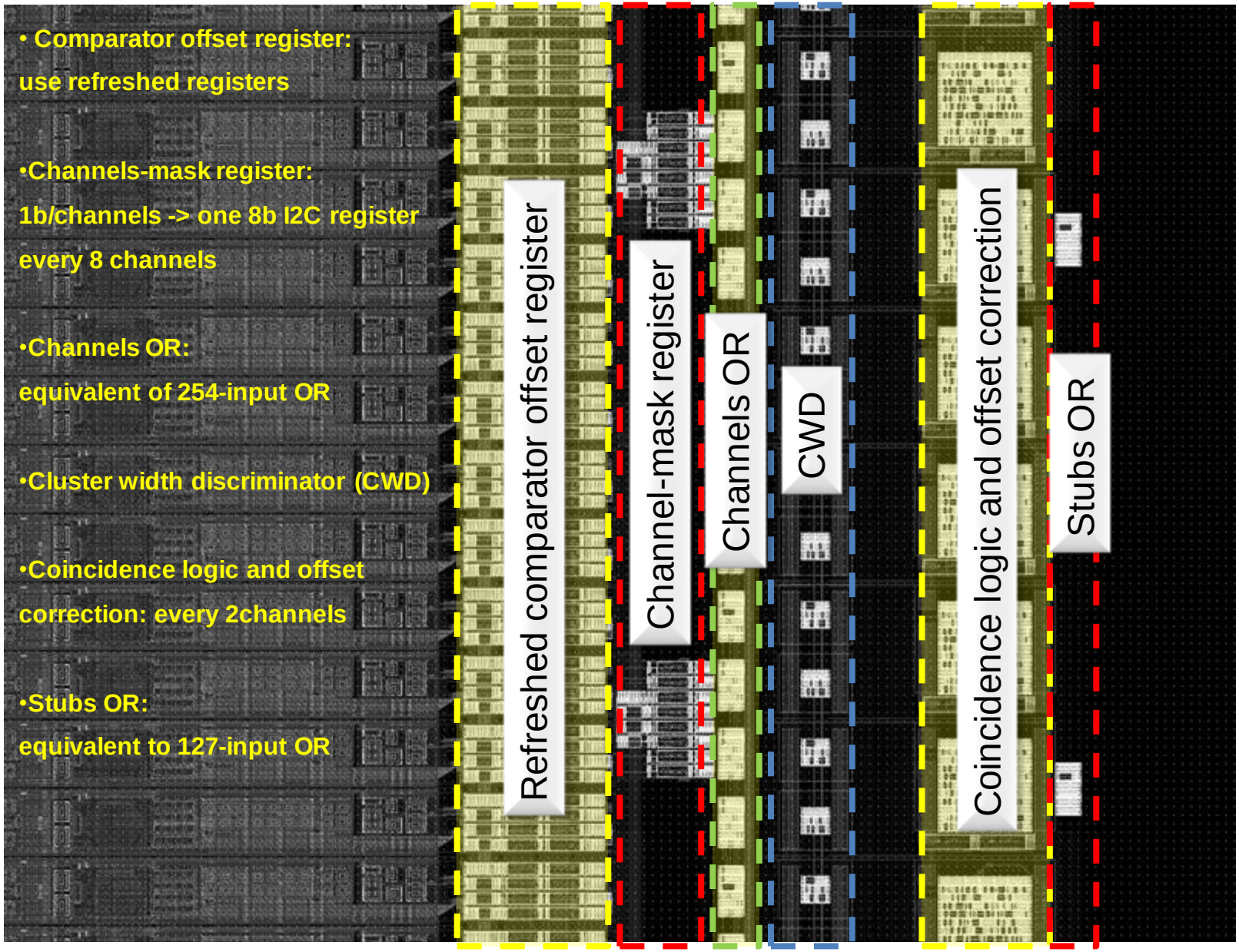
•Channels-mask register:
1b/channels -> one 8b I2C register
every 8 channels

•Channels OR:
equivalent of 254-input OR

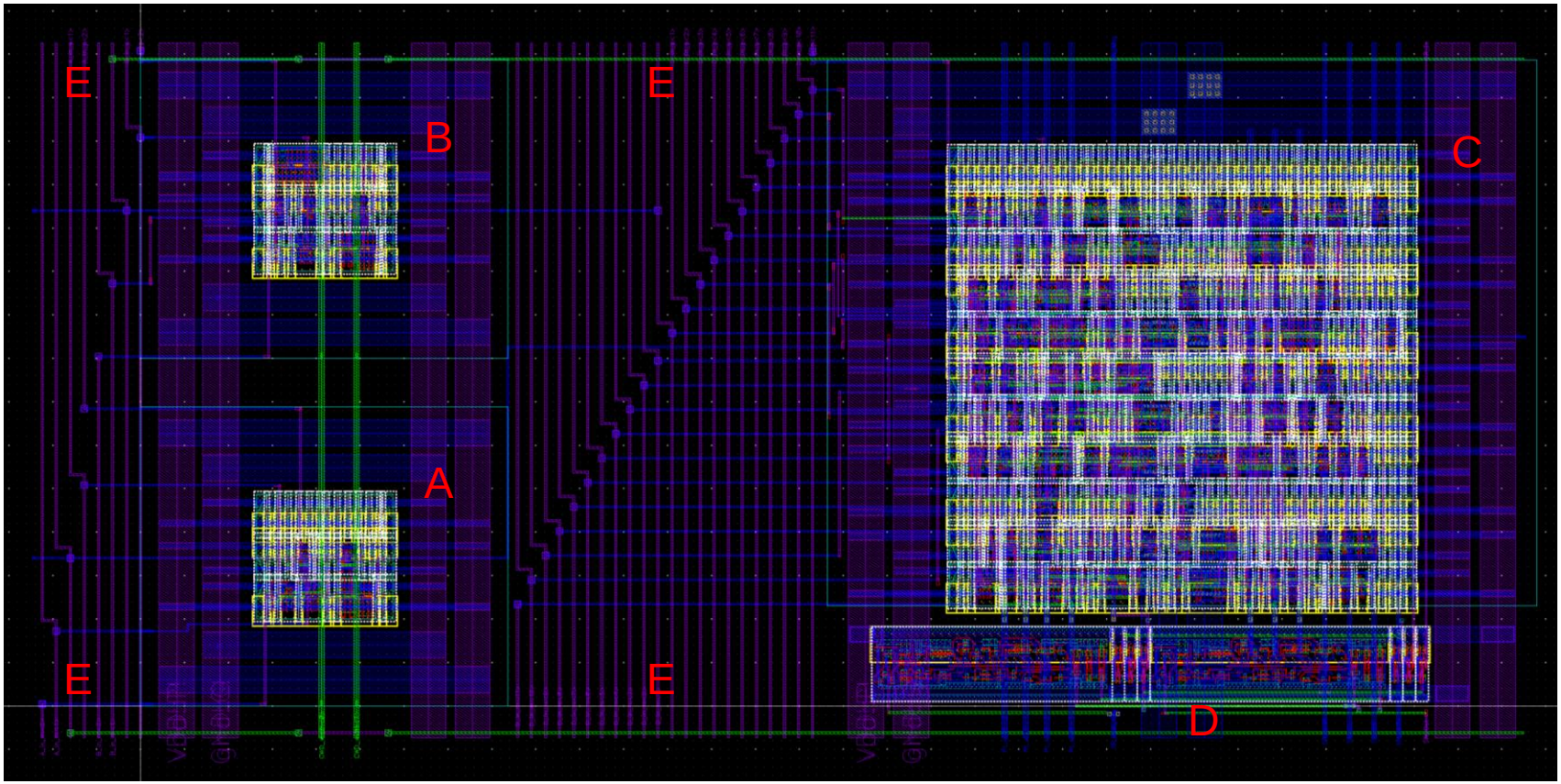
•Cluster width discriminator (CWD)

•Coincidence logic and offset
correction: every 2channels

•Stubs OR:
equivalent to 127-input OR



Coincidence logic - Detail



A: Cluster width discrimination for bottom sensor hits

B: Cluster width discrimination for top sensor hits

C: Coincidence logic (with programmable window and offset correction)

D: Shift register for stubs readout and shadow SR for readout control

E: lines to/from previous/next channels (propagate for ~1mm (11*80um))

Design status

Analog channels

Coincidence logic

Pipeline memory

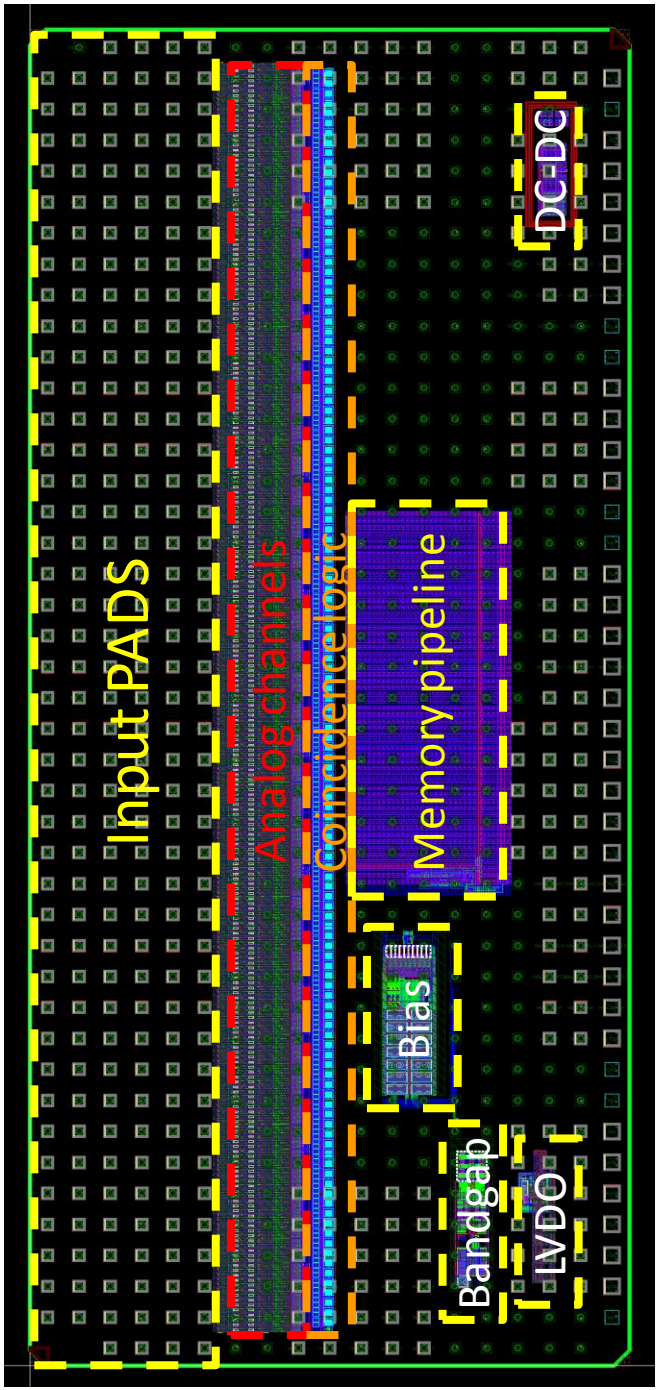
Bandgap reference

DCDC converter **supplied by CERN**

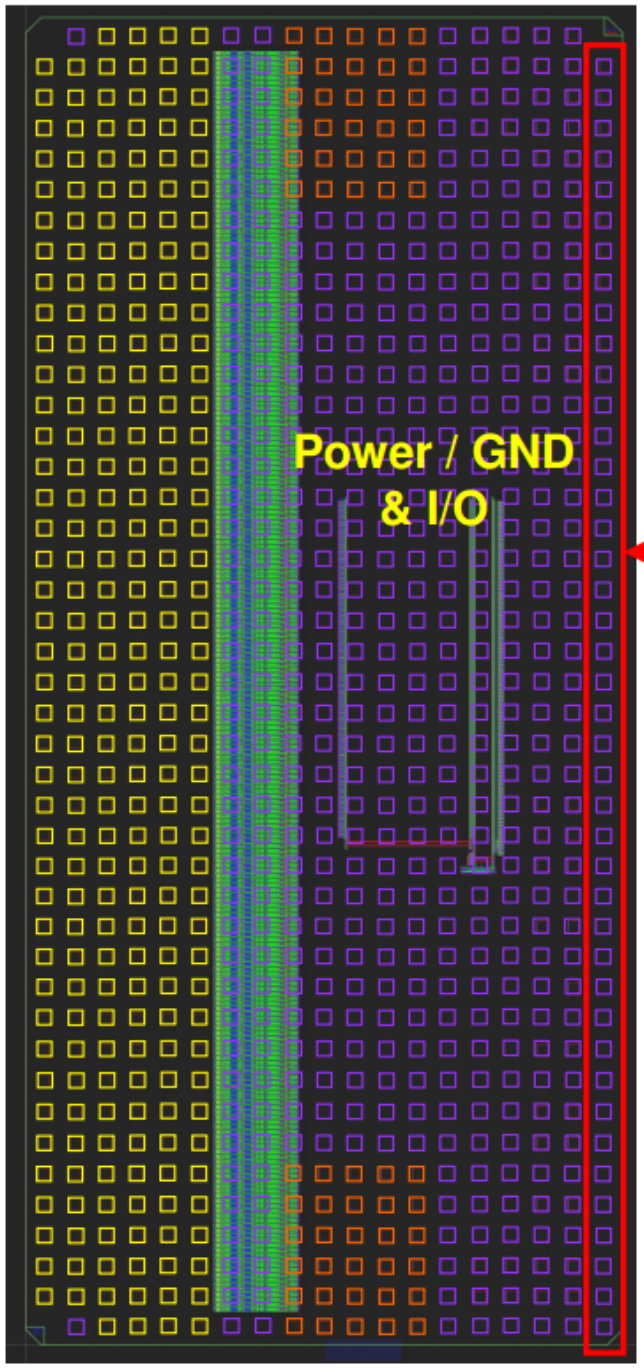
Low Voltage Dropout Regulator

Bias block

Test Pulse circuit



I/O scheme



43 rows x 19 cols = ~ 800 bumps

10.75 x 4.75 mm²

inputs

outputs to / inputs from neighbours

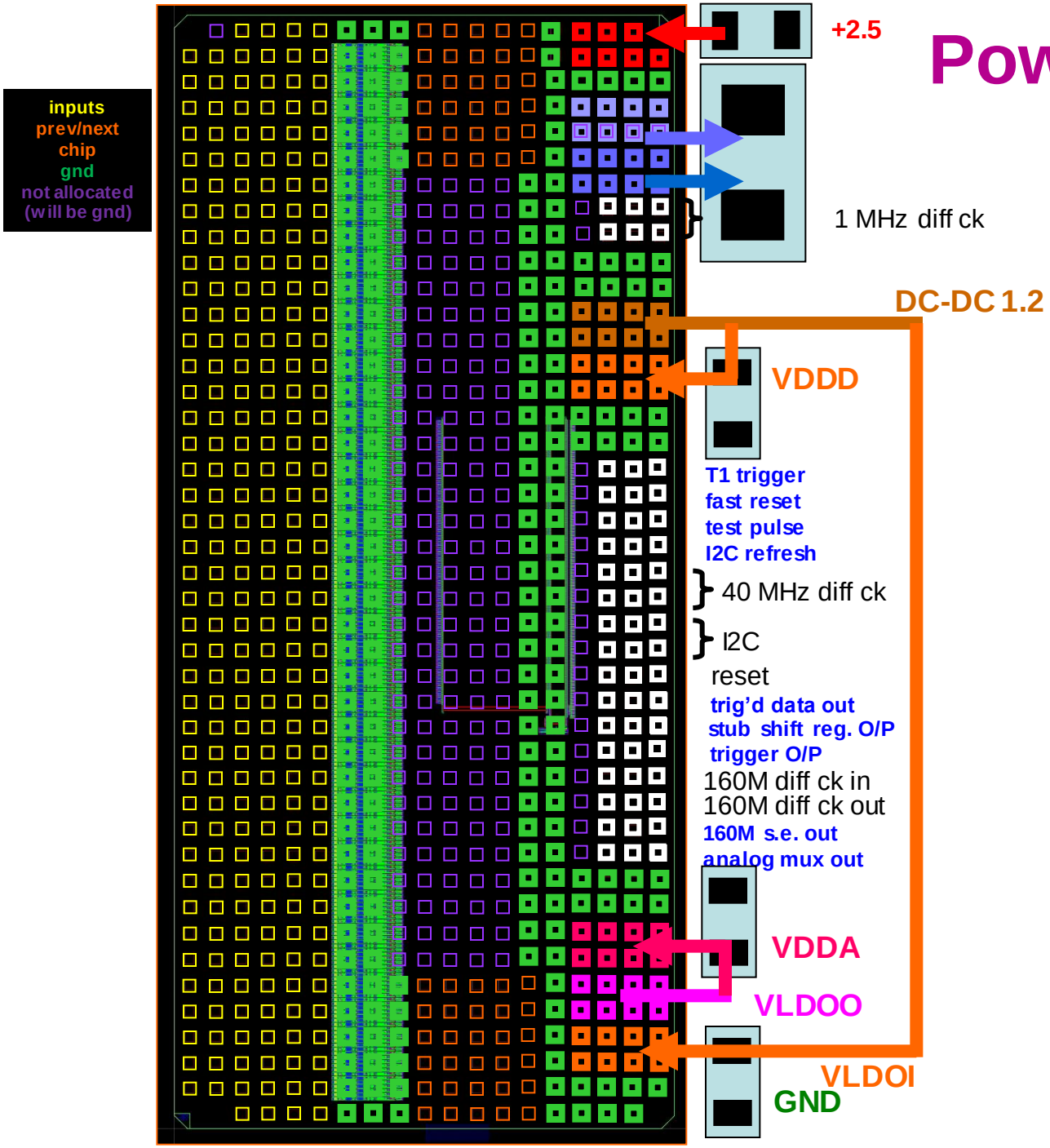
probe-able pads for wafer test

access to:
- power
- fast control
- I2C
- outputs

should be able to provide quite thorough test of chip functionality

NB: at least 2 columns of gnd pads must separate input pads and pads for digital inter-chip signals (orange)

Power distribution



NB: the last column of PADs to the right are wire-bondable, they will not be routed on hybrid (->possible to reach the 3 pads to their left)

All but 160MHz output pads have redundancy

lines and arrows
show direction of power flow
(GND not shown)

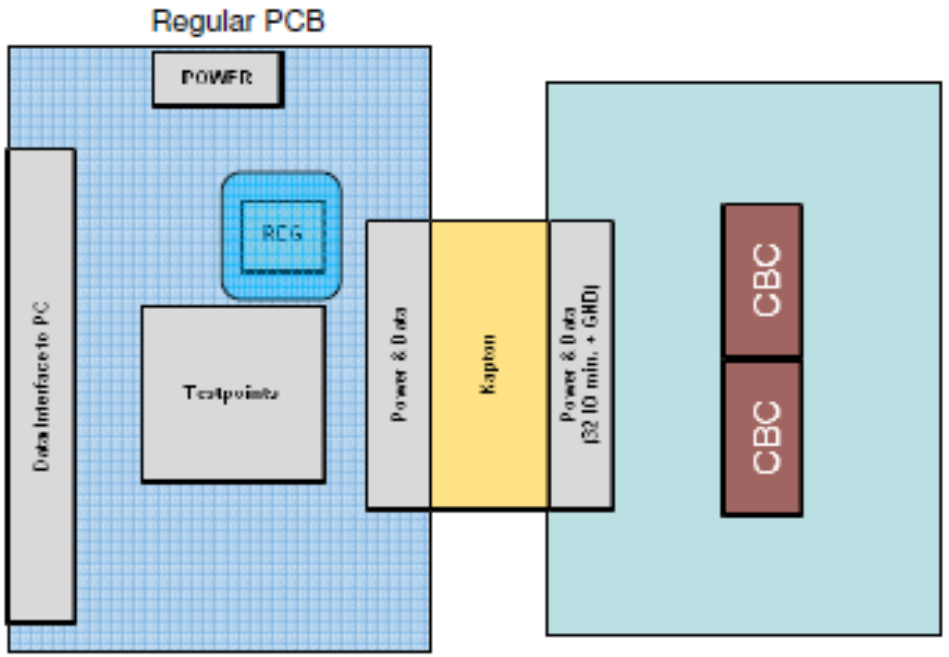
note:

DC-DC 1.2 not connected
to VDDD or VLDOI on-chip

LDO output also connected to VDDA off-chip

(the idea is to maximise possible effectiveness of off-chip filtering)

Future Work



1) Submission in June 2012

2) single ASIC functionality test (WB)

3) Dual chip test hybrid (BB): can investigate inter-chip connections and effects at chip boundaries (1 sensor connected at 2 chips)

3) 8chip substrate (BB)

4) once data readout clear we can start work on CBC3 with full stubs readout

Conclusions

- CBC2 builds on successful previous version for readout of silicon strips of CMS outer tracker (very low power)

- Introduces important new features such as BB connection to hybrid, 254 channels, a few fixes

- Incorporates stub finding logic (without significant additional power consumption)

- Allows us to make tangible progress with substrate development and test the performance/pitfalls of the stub finding concept in test beam