The CBC microstrip readout chip for LHC Phase II at CMS

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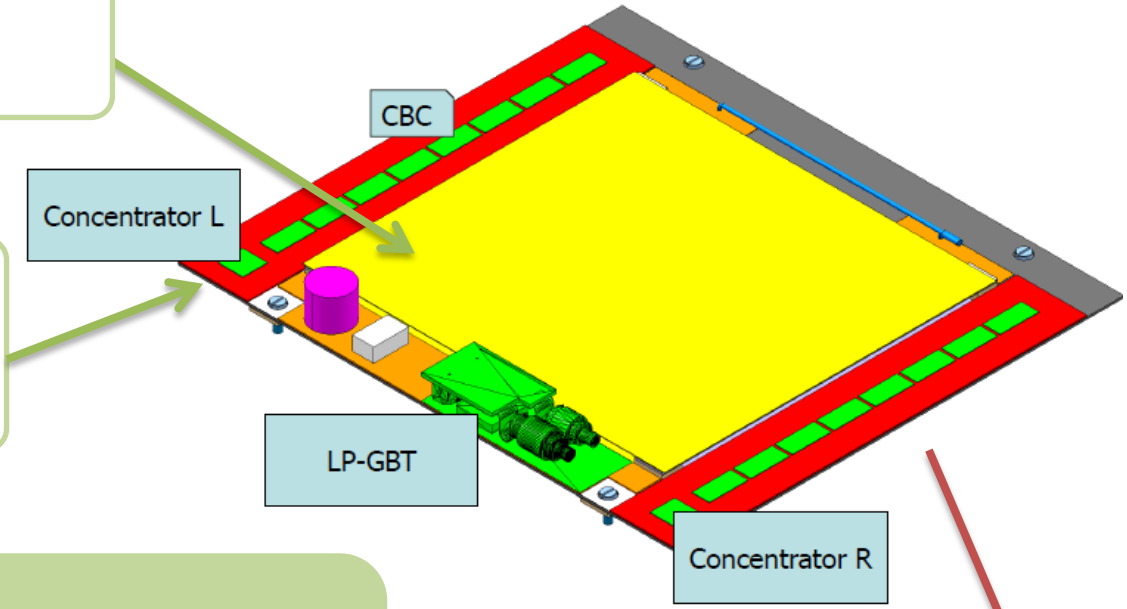
Imperial College, London, Rutherford Appleton Laboratory
CMS Collaboration

2nd Workshop on Intelligent Trackers
Pisa 3-5 May 2012

2S-PT outer tracker module

10cm x 10cm **stacked** strip sensors
strip length ~5cm
strip pitch 90um

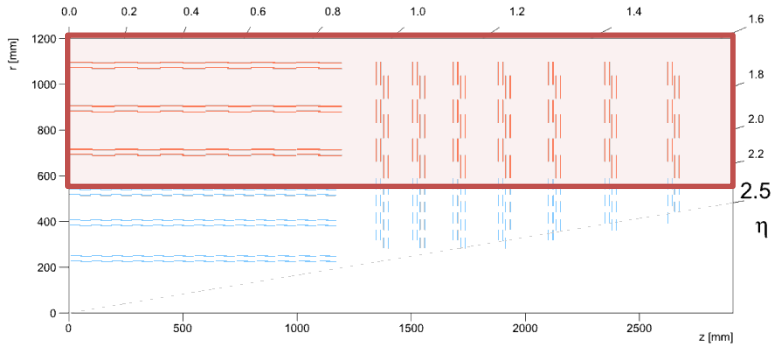
high density interconnect
pitch adaption
low mass



focus on 'simplest', lightweight design for provision of tracking-trigger information using stacked scheme

available/mature technologies – quick to prototype/test

inexpensive & power/mass/design efficient choices to instrument large area in outer tracker region



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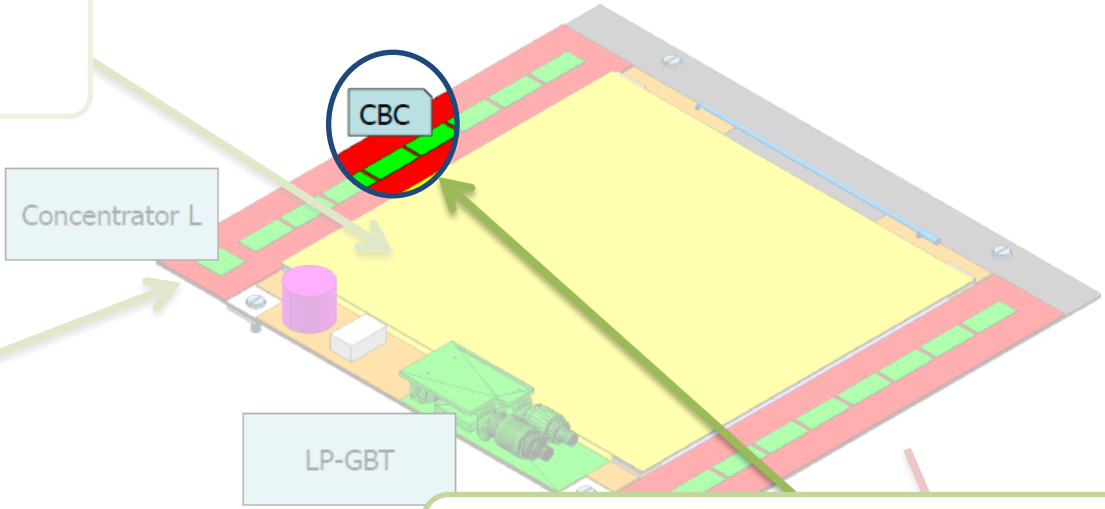

front end prototyping – CBC (CMS Binary Chip) for hit correlation and L1 readout

see also talk by D. Braga (afternoon) on next CBC iteration

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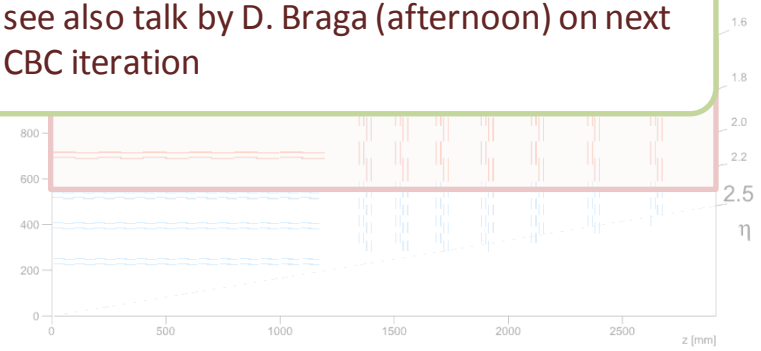
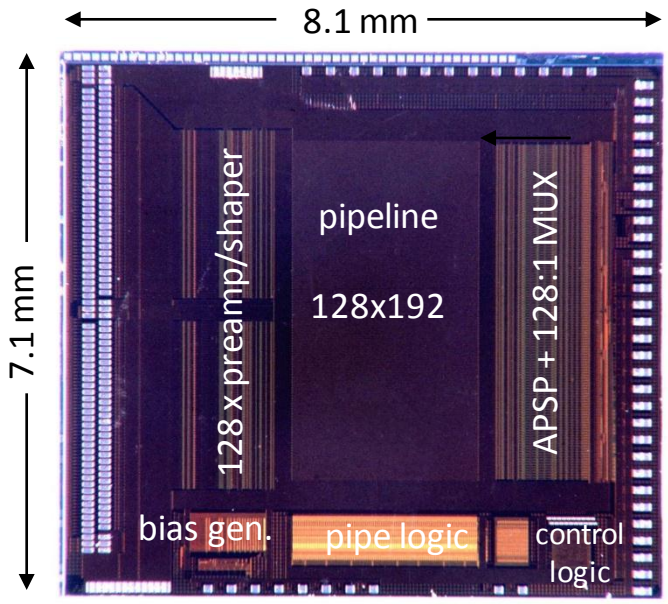


CMS tracker readout architecture

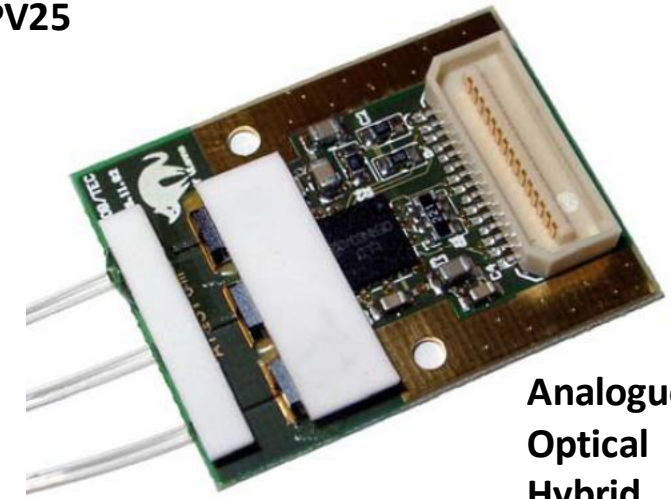
analogue pulse height, analogue unsparsified readout
- simple synchronous system, occupancy independent data volume
- useful for debugging (HIPs, SEUs, high rate noise, pipeline emulation etc) & commissioning

radiation hard 0.25µm CMOS chip (APV25)
- low power (~2.7mW/channel for 10-20cm strips)

analogue optical off-detector readout
- optical conversion on module
- transmission at 40 MS/s over 100m on 1310nm single-mode fibre
- approx 39k links



APV25



Analogue Optical Hybrid

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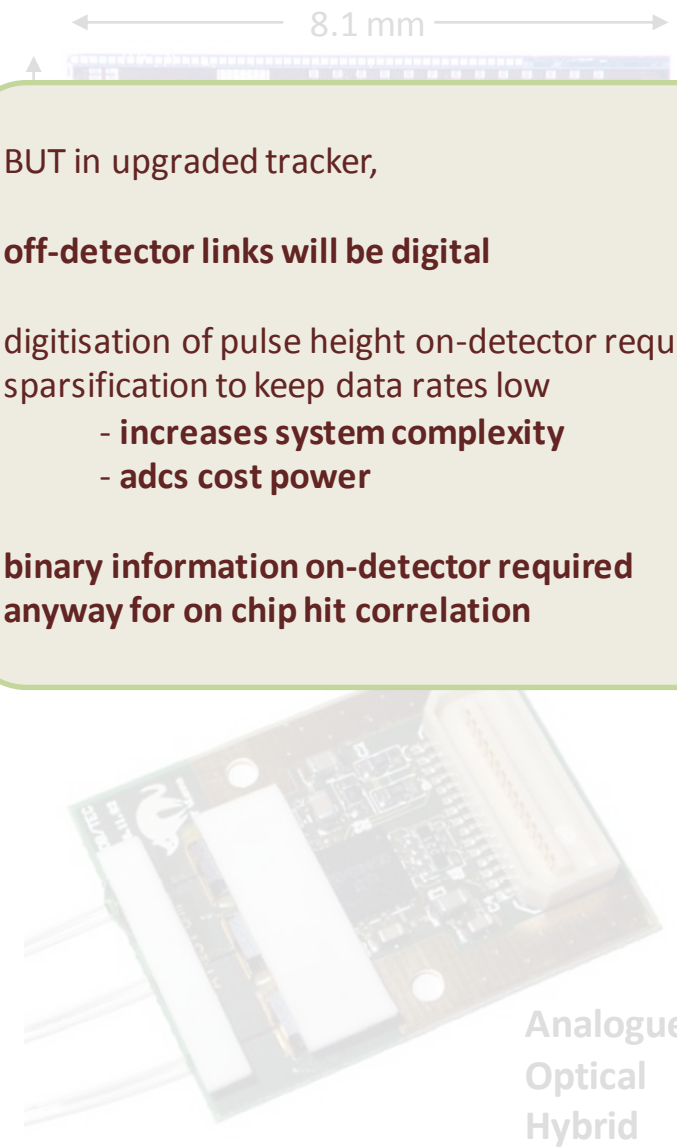
BUT in upgraded tracker,

off-detector links will be digital

digitisation of pulse height on-detector requires sparsification to keep data rates low
- **increases system complexity**
- **adcs cost power**

binary information on-detector required anyway for on chip hit correlation



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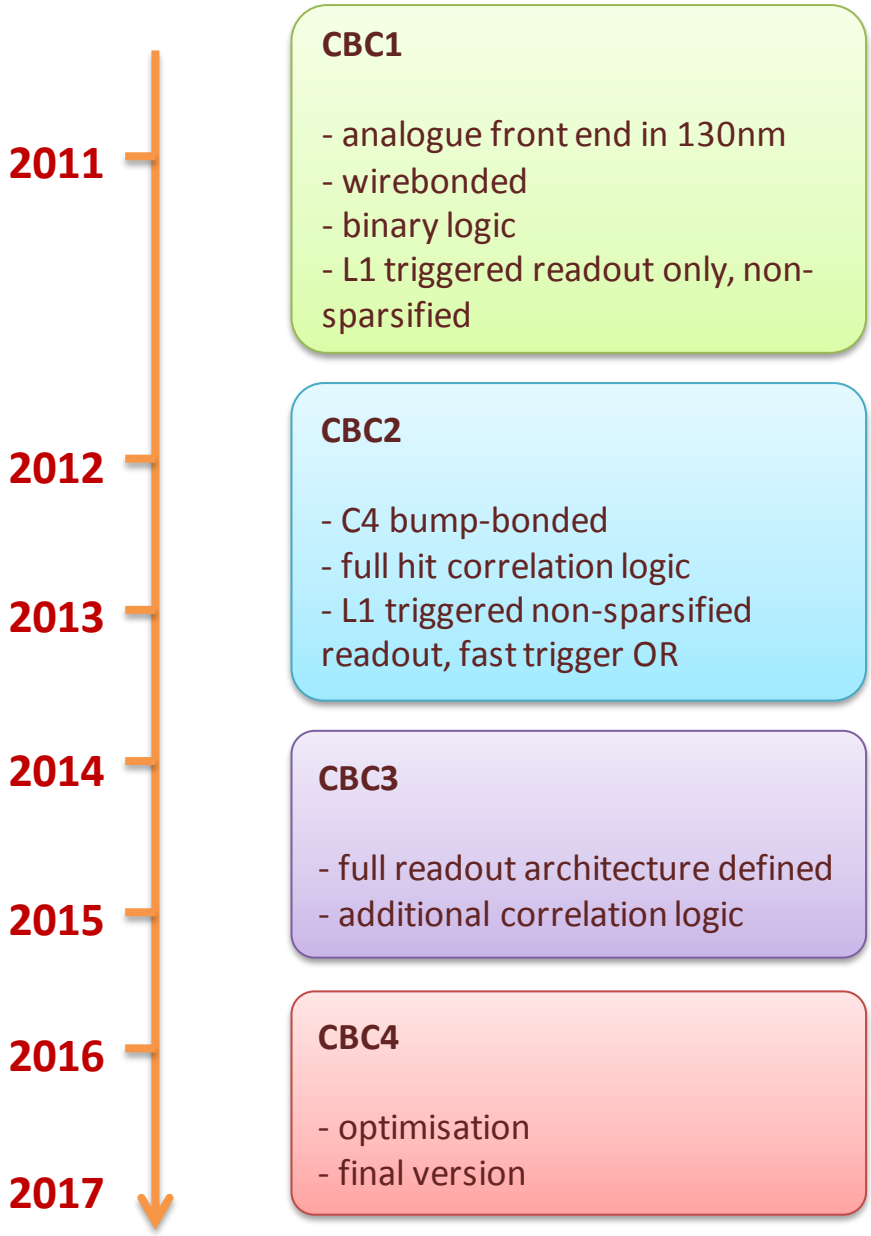
1. keep architecture as simple as possible

2. build/simplify on APV front end

3. reduce power as much as possible

4. iterative process

CBC 'rough' roadmap



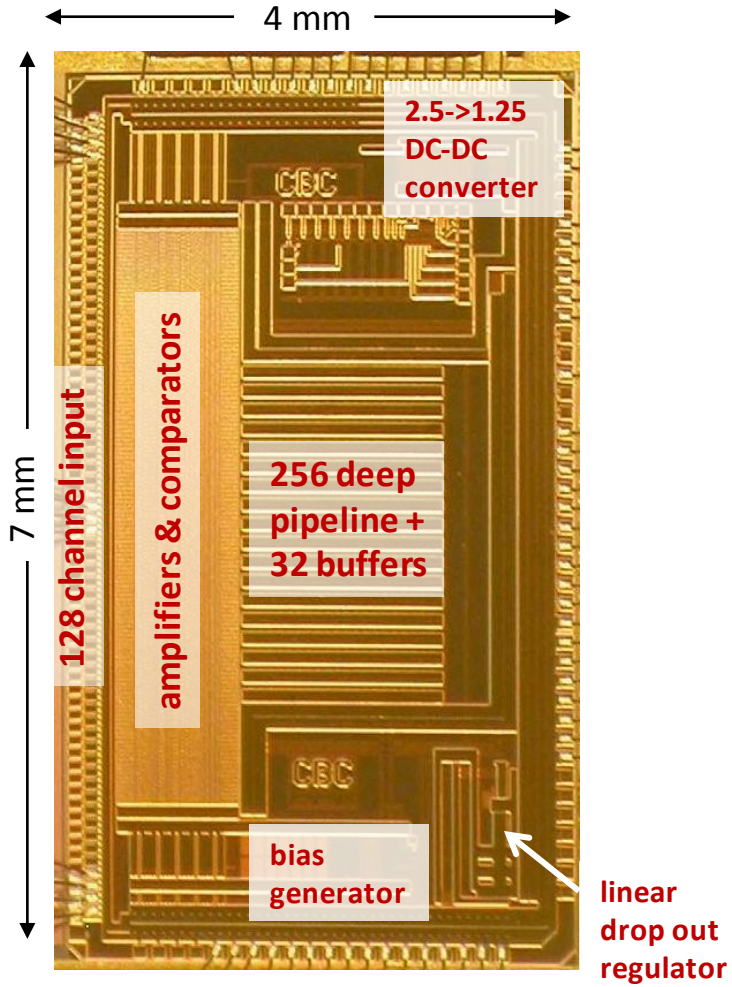
CMS Binary Chip (CBC)

CBC - 130nm prototype ASIC (Feb 2011)

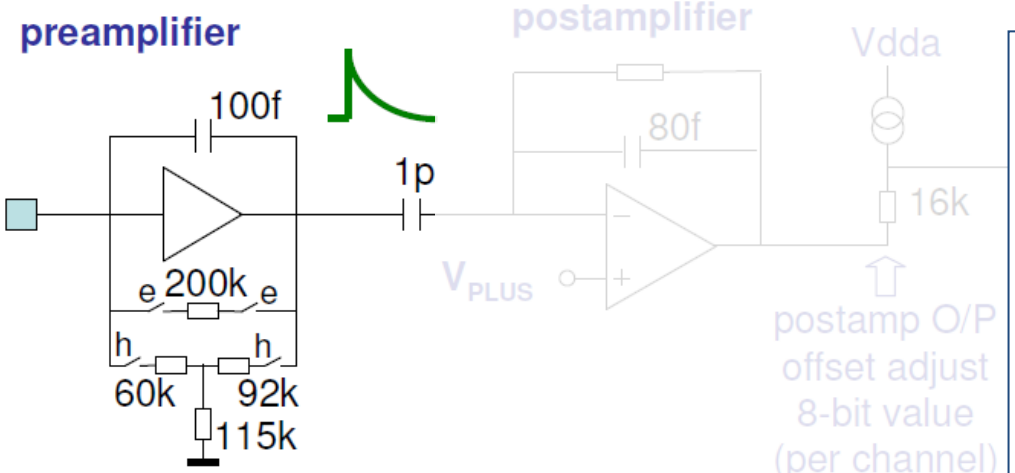
binary, unsparsified readout
- simple synchronous system ; fixed throughput

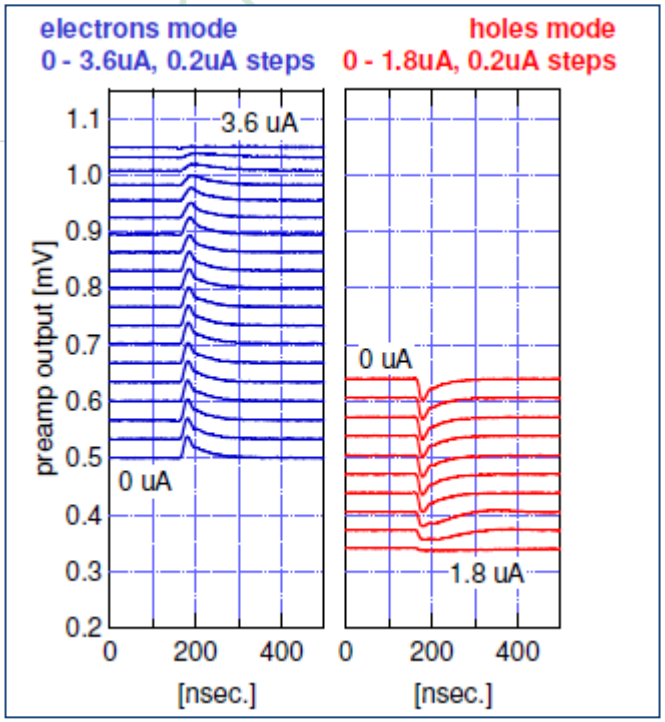
128 channel input, +/- polarity
50um input pitch
designed for short strips (2-5cm)
triggered serial data out (SLVS)
I2C programmable (bias, latency, thresholds etc)

powering options
- on chip DC-DC converter for 1.2V chip bias
- LDO for stable 1.1V analogue supply



front-end simplified schematic



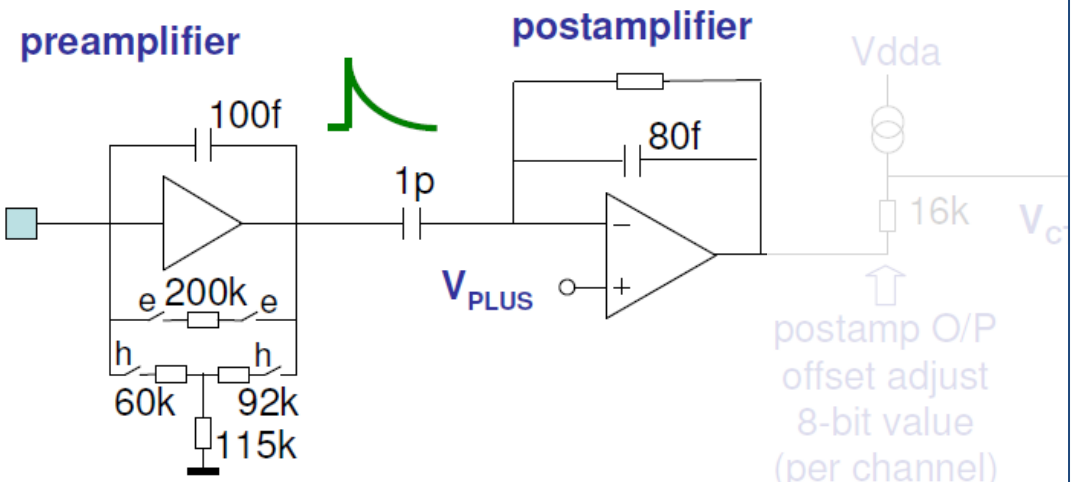


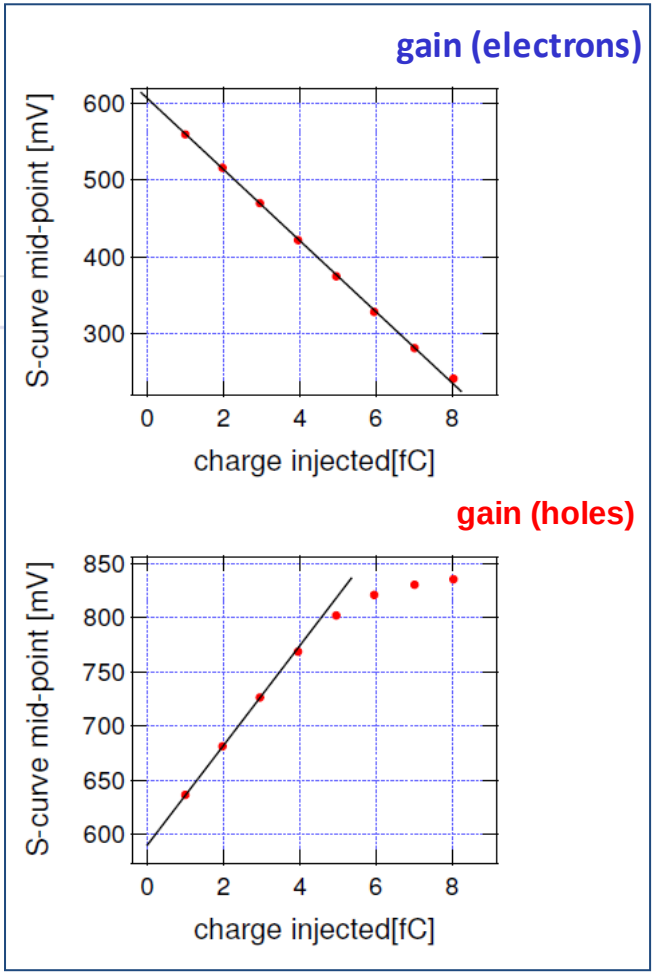
design allows AC or DC coupling

operates in electrons or holes mode
- adaptable to choice of sensor technology
- resistor network absorbs leakage current (more than 1uA headroom in holes mode)

20ns time constant
- shorter decay time, no deconvolution needed

front-end simplified schematic

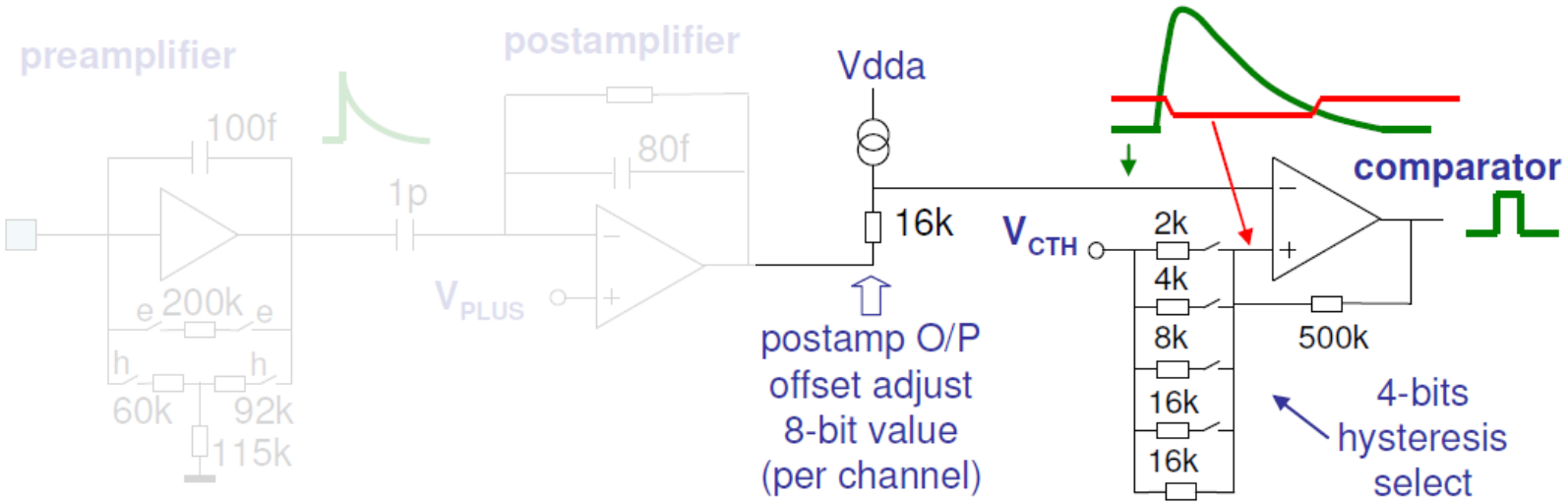




postamplifier stage is AC coupled to preamplifier output
- baseline postamp output voltage set by global V_{PLUS} bias
- overall 20ns peaking time
- 50mV/fC gain, good linearity at the threshold region

provides gain and high frequency noise filtering/shaping before comparator

front-end simplified schematic



comparator stage follows postamp via series resistor

each channel implements 8-bit I2C programmable current source to resistor to adjust DC level after postamp

- corrects for channel to channel variations for threshold uniformity

global comparator threshold via V_{CTH} and a 4-bit programmable resistive hysteresis network

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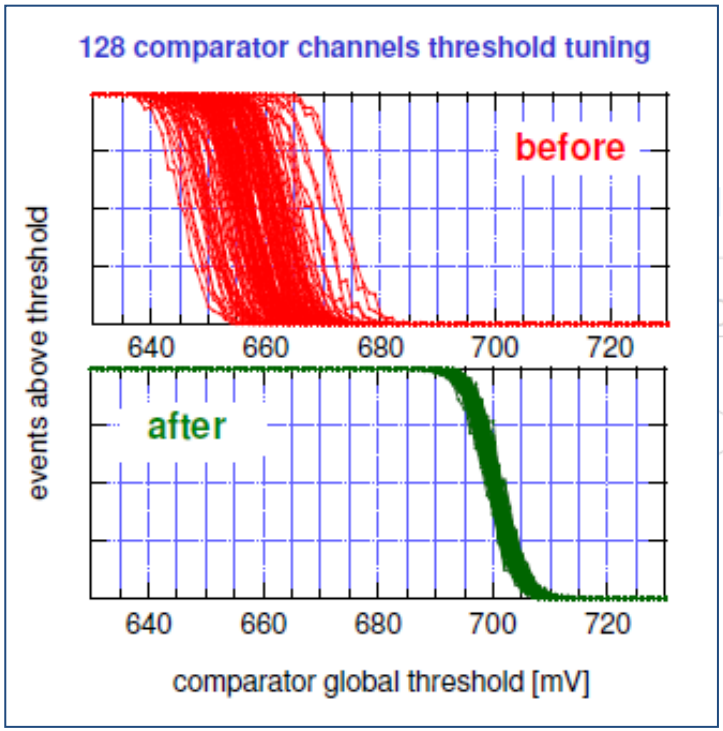

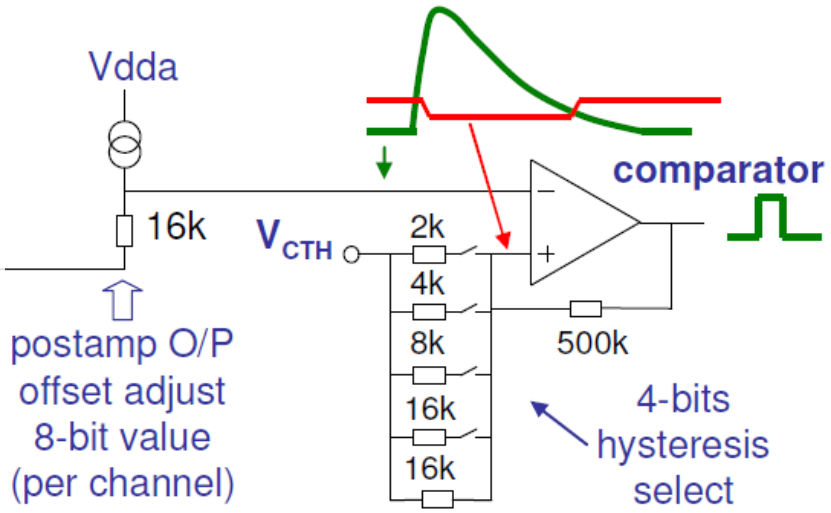

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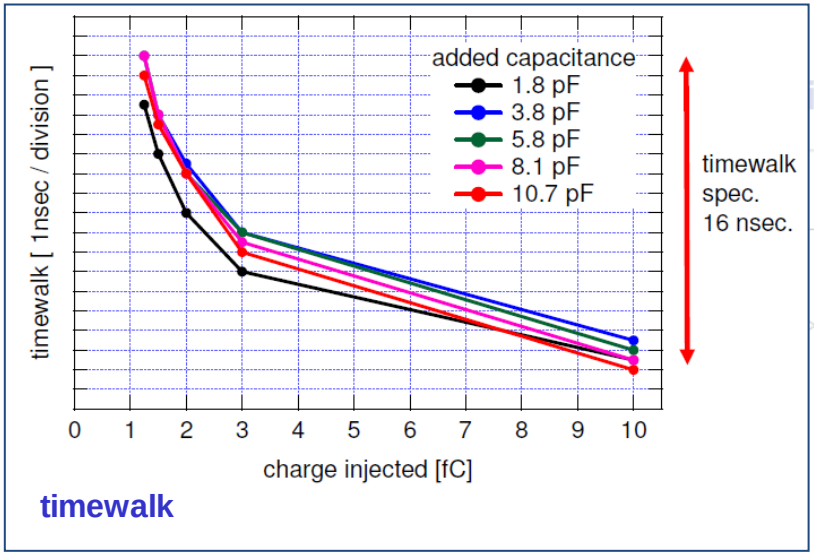

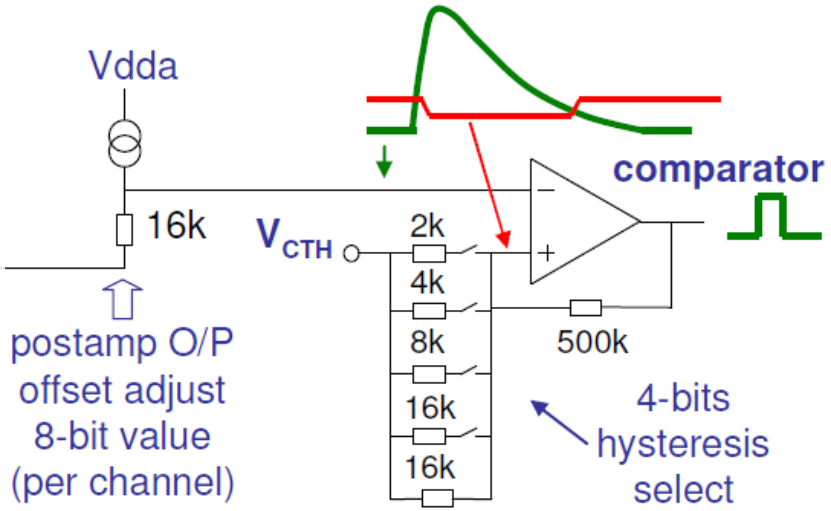

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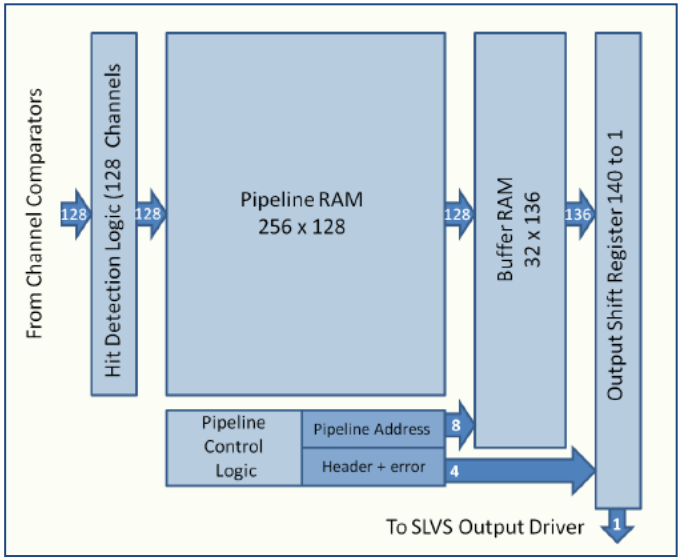
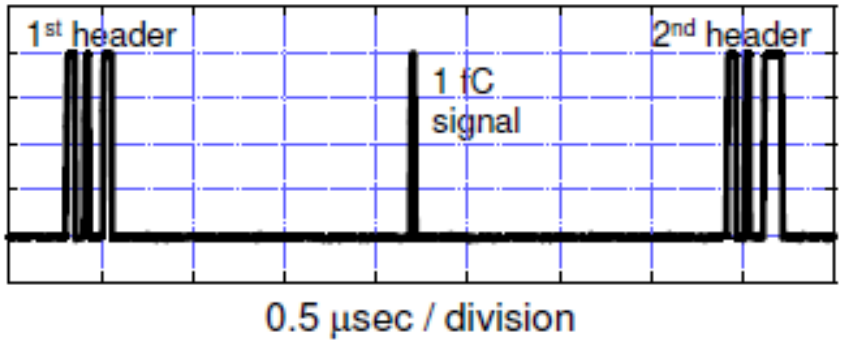
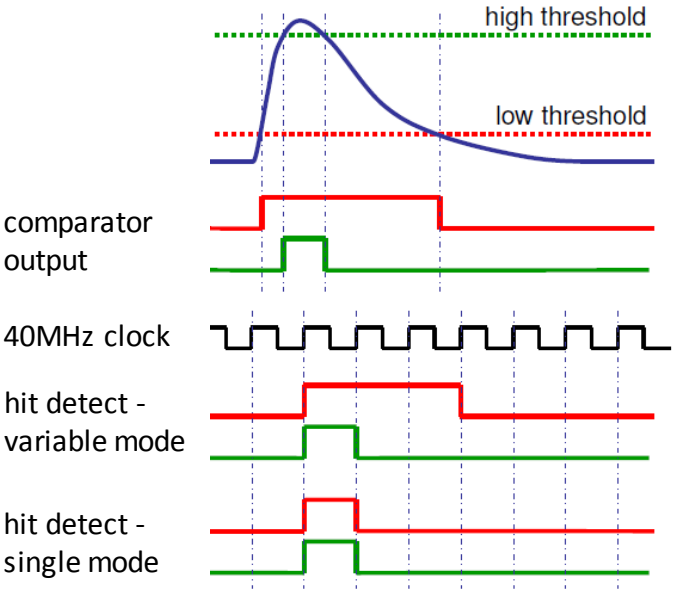
digital logic







no correlation/trigger logic in this iteration
- **triggered readout only** (~270kHz max sustained)

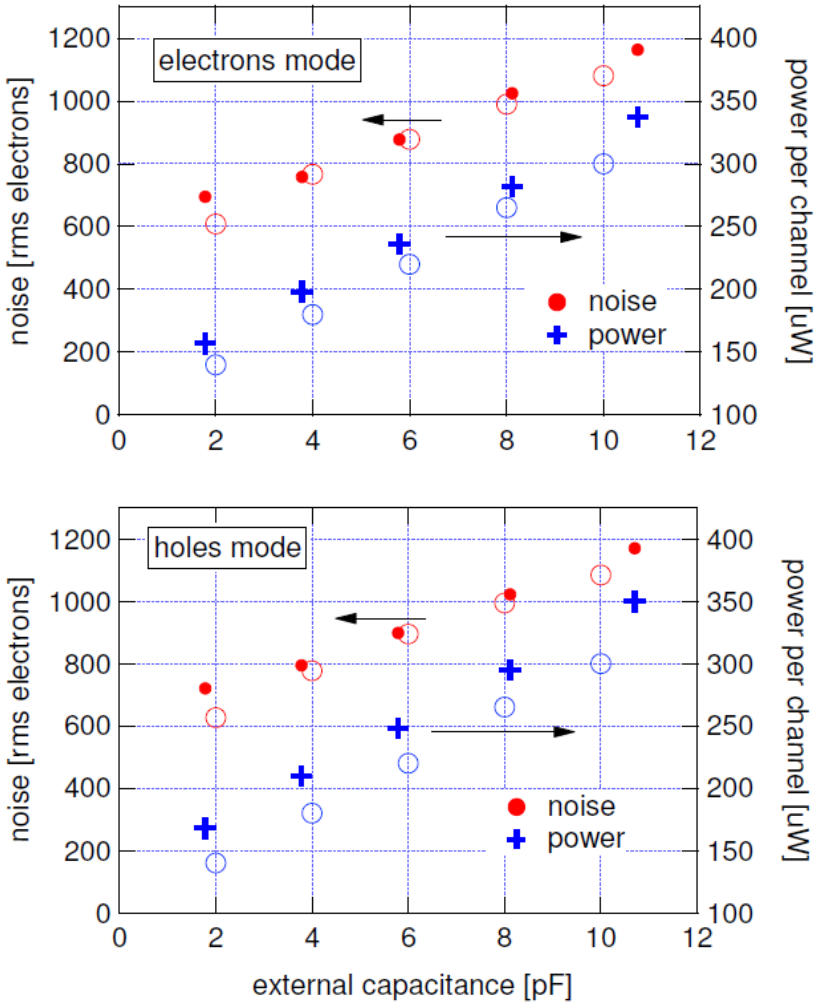
hit detect logic in two modes – single/variable

output from each channel stored in a 256 sample deep pipeline RAM (6.4us latency max)

32 trigger FIFO buffer

unsparsified readout (140-to-1 shift register)

power/noise



noise dependence on external capacitance
- performance for both polarities identical and matches simulation (open circles)

power dependence on external capacitance
- adjust preamp current to keep pulse shape
- performance for both polarities close to simulation (open circles)

analogue: 130 + (21 x C_{EXT}[pF]) uW/channel

digital: < 50 uW/channel

for 5pF sensor:

total power: <300uW/channel

noise [enc] : ~800 electrons

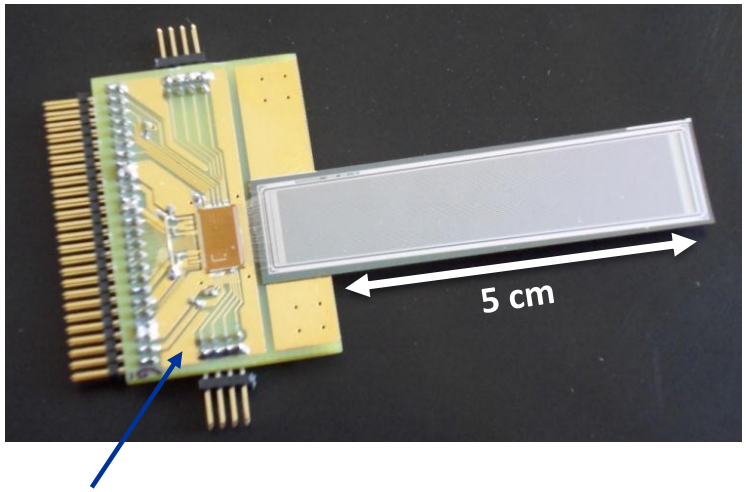
(target <1000 electrons, <500 uW/channel)

x9 reduction in power consumption wrt APV25

operation in beam tests

CBC under test in lab since February 2011

also tested at CERN H8 beam line with
- **400 GeV/c protons** (September)
- **up to 160 GeV/c/nucleon Pb(82+) ions** (November)



CBC sensor test board

CBC bonded to a short strip (5cm) p-on-n sensor for testing
- 120-150 um pitch (fan shaped)
- 320 um thick
- only 64 strips bonded to chip (no pitch adaptor)

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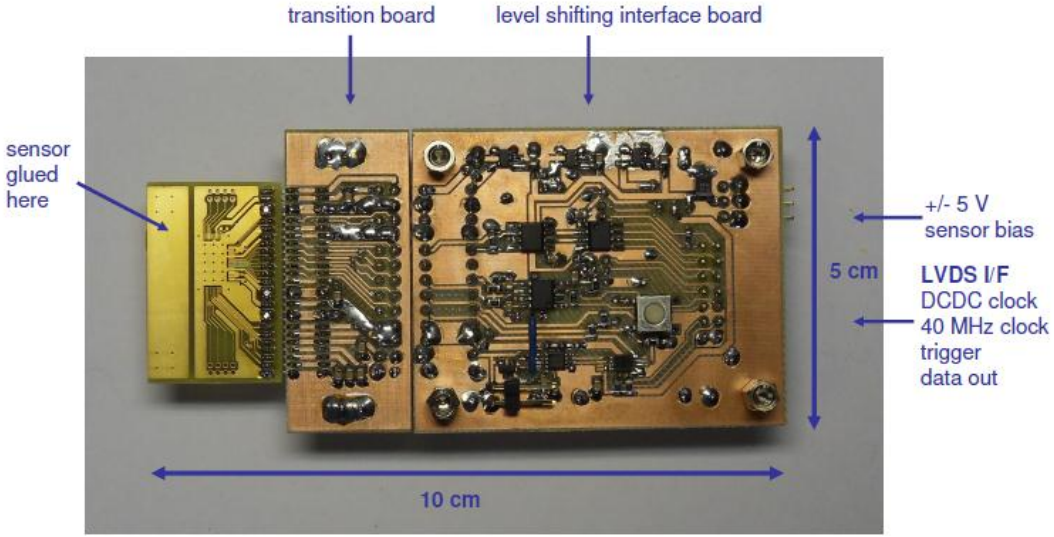

basic 'module' constructed

- level shifting board to perform external LVDS/internal SLVS conversion

- external interfaces board

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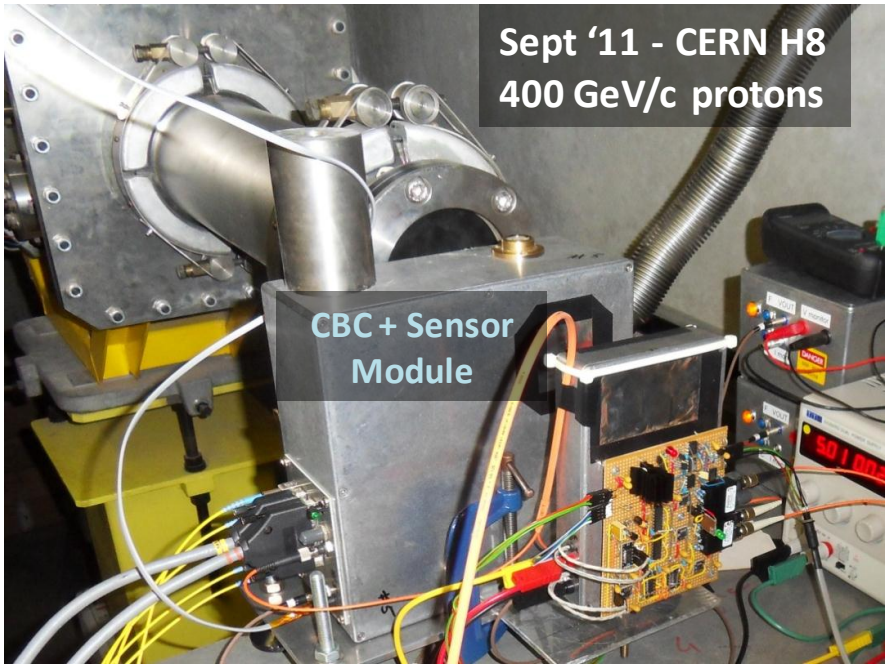


external interfaces board for

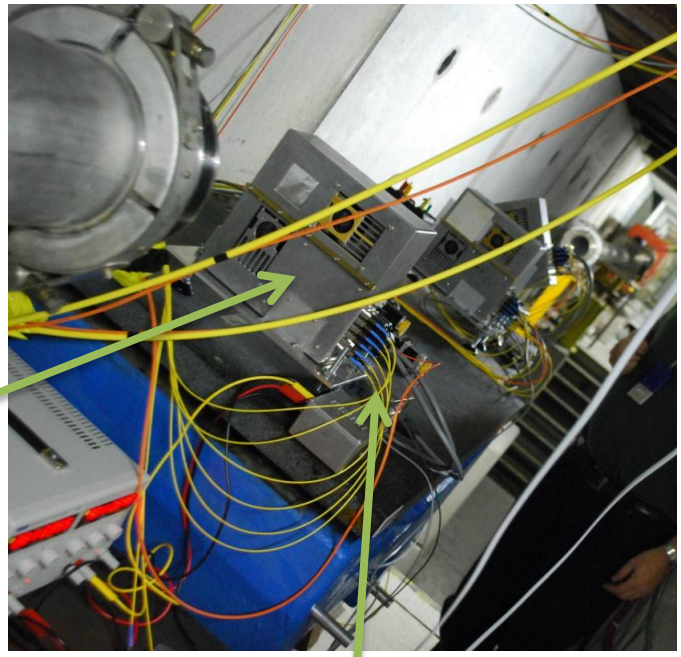
- optical 40MHz clock and trigger/reset recovery and conversion to LVDS

- biphase mark encoding of CBC data stream and LVDS-optical conversion

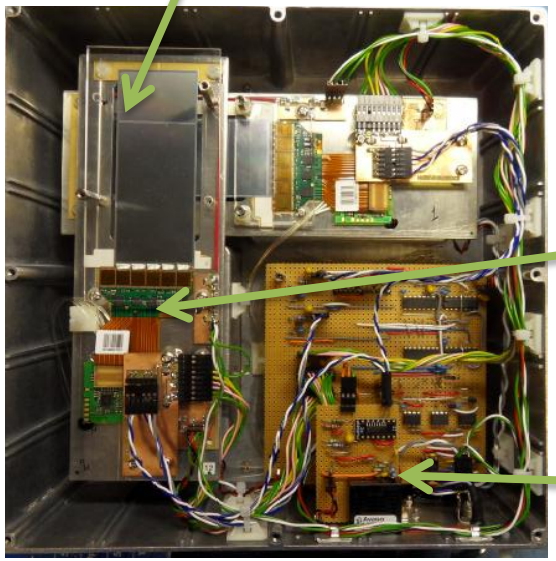
- 1.2V & sensor biasing, I2C

telescope for H8 beam line

CBC module operated in parallel with a silicon strip telescope used in H8, developed at IC
- actually running parasitically off UA9 test beam



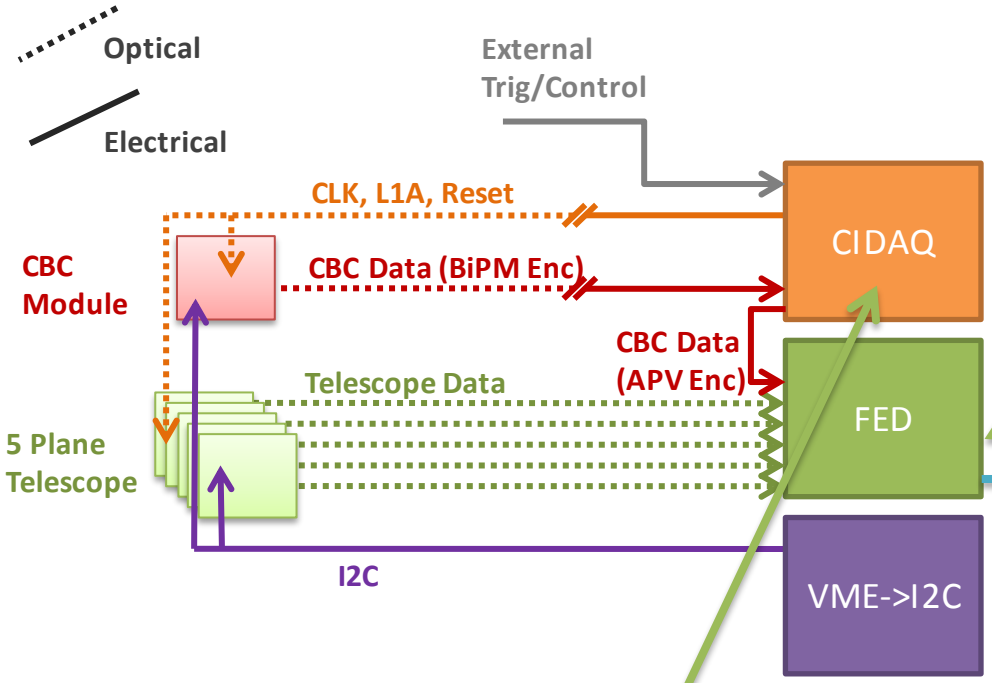
provides five 2D measurements (10 sensors)
- sensors with 60 um readout pitch
- plus intermediate floating strips



readout system based on CMS tracker
- APV25, PLL, AOH from tracker modules
- analogue optical data transmission

simple control via direct I2C

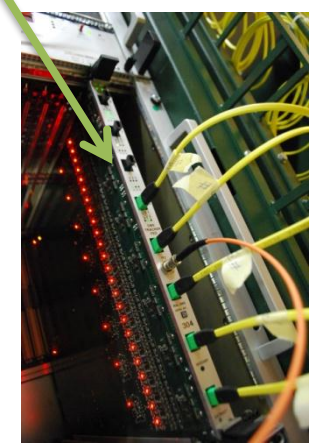
telescope and CBC DAQ



analogue optical data is digitised by FED
- pedestal/CM subtracted & sparsified
- transmitted to PC nodes via S-Link64 (400 MB/s)

FED Raw Data
(S-Link64)

PC Cluster

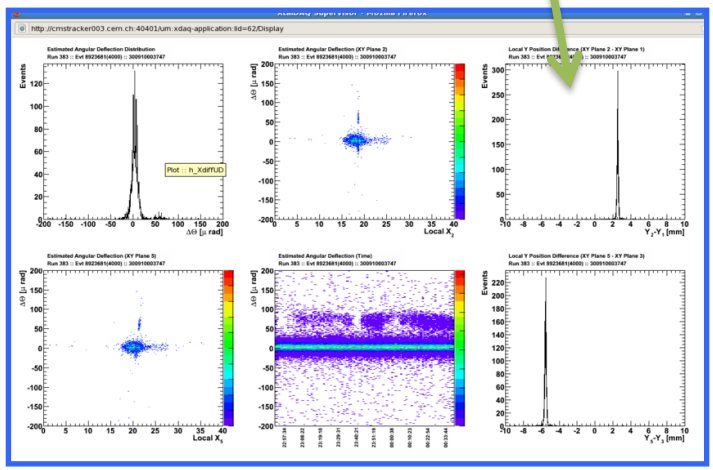


telescope & CBC module fast control via 6U VME DAQ card (iDAQ)
- trigger/reset control logic
- timestamp resolution <1ns
- CBC biphase data decoding & event buffering
- readout via VME or encoded as APV frame & sent synchronously to FED

PCs running full CMS DAQ framework
- fully compatible software
- implements HLT for reconstruction, event selection & online DQM

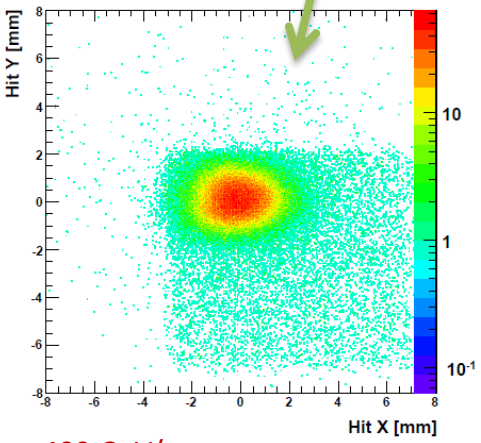
telescope performance

high rate flexible DAQ
- sustained rate 10kHz to disk
- 50kHz during spill (10s)
- online plots

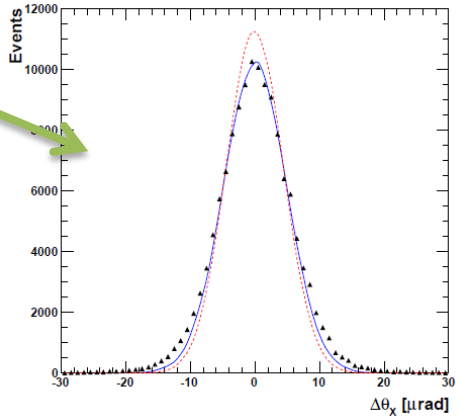


spatial resolution - 6.8-7.0um

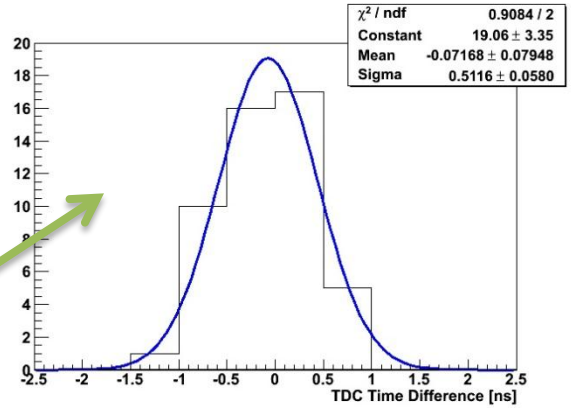
angular resolution - 5.2urad



400 GeV/c protons



0.51 ns trigger timestamp resolution in CiDAQ

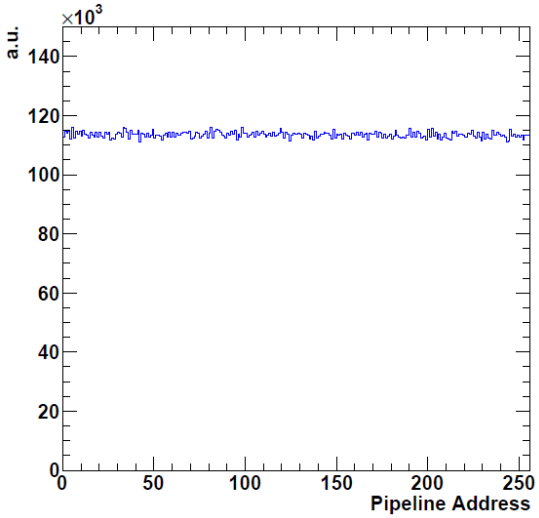


CBC performance in beam

operated successfully – no issues

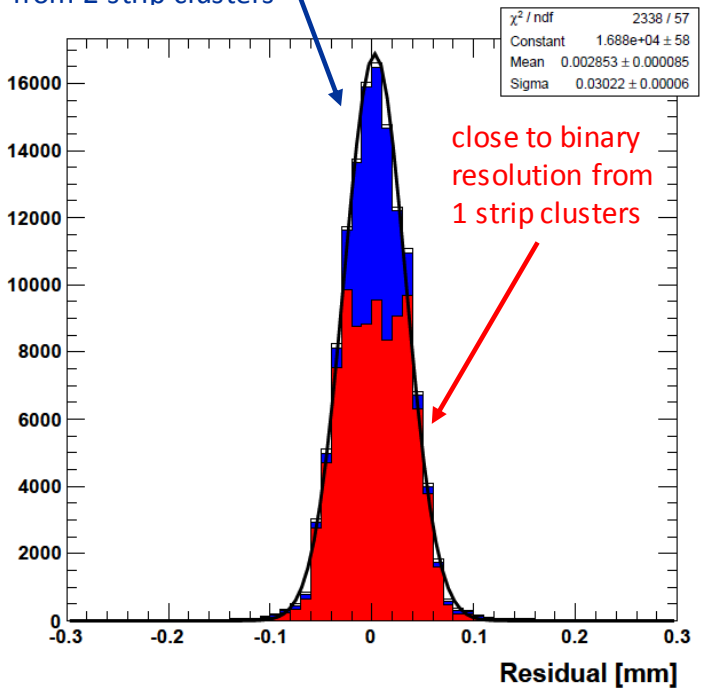
no pipeline errors

no CBC errors detected in > 30 M events



better than pitch/√12 due to contribution from 2 strip clusters

close to binary resolution from 1 strip clusters

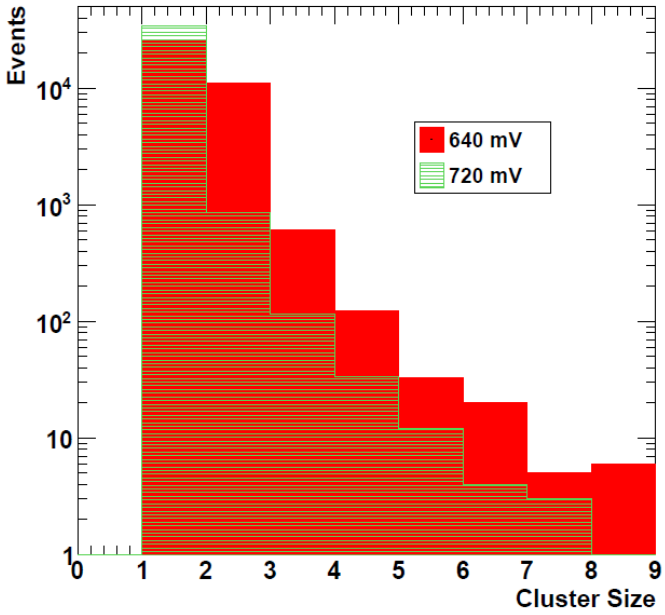


use telescope to select events at CBC module
- single track events only (pileup eliminated)
- incident on CBC sensor (transverse to strips)
- incident in 3mm along strips (const p=134um)
- events within 7ns of sampling clock

measure resolution of CBC module from residual
- using telescope for track extrapolation
- factoring out telescope spatial resolution

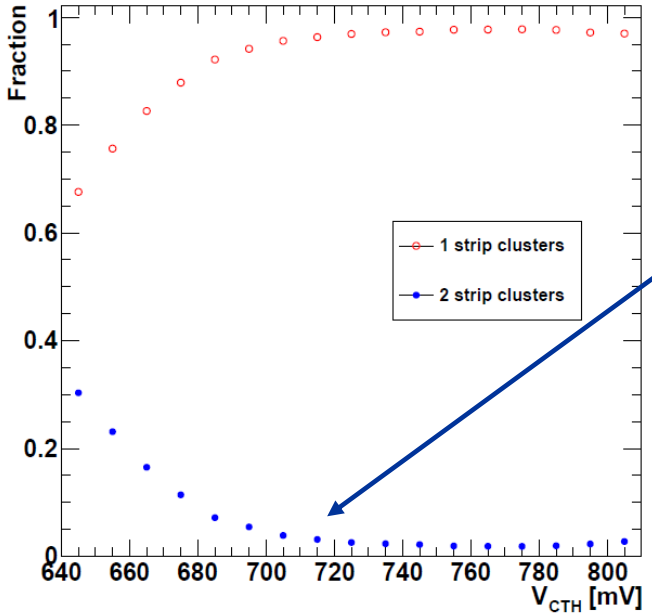
resolution: 29.4 um

CBC performance in beam



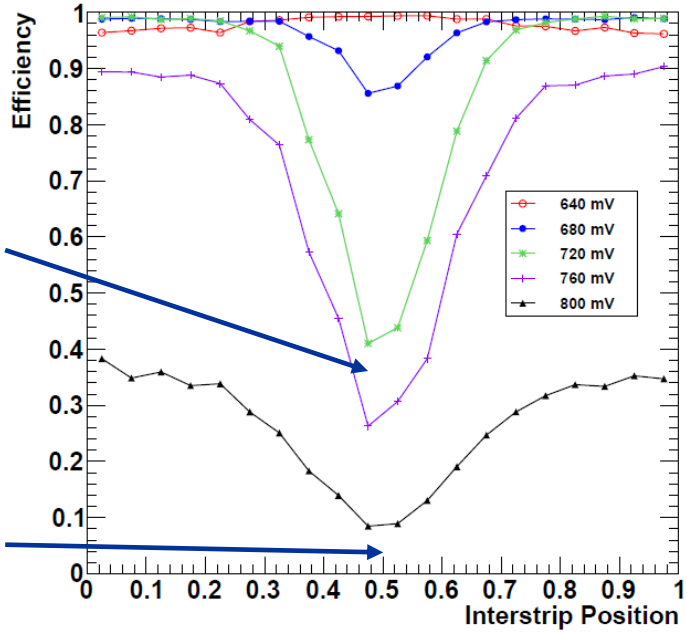
cluster width, resolution and efficiency will be affected by threshold setting

- expecting to operate at 1fC level (~640mV)
- important to get rough estimations for tuning stub/tracklet simulations
- study of noise occupancy with threshold required



2 strip clusters originate from interstrip region

efficiency drop due to charge sharing



CBC performance in beam

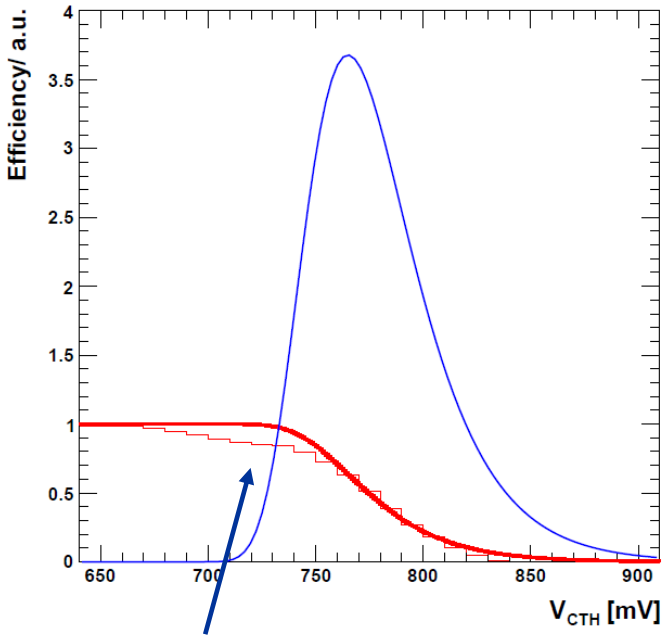
advanced measurements possible (in progress)
- reconstruction of the signal distribution in sensor
- reconstruction of the pulse shape

sweep threshold and measure CBC hit efficiency (after cuts)

assume landau-like signal -> fit reverse cumulative distribution to data

most probable signal: **3.5 fC (22,000 e)**

noise floor: **840 e**



not perfect - too coarse binning in time (events escape into next bx due to timewalk)

other tests remaining
- radiation: SEU, ionising effects
- cold temperature operation

concentrating on CBC2 design now

may wait to test on CBC2, more appropriate sensors, prototype module, etc

summary

focus on designing the first CMS binary front end chip in 130nm

prototype CBC – designed for readout of short strips, 128 channels, front end amplifier, comparator, pipeline, triggered binary unsparsified output

works with both sensor polarities, can be DC coupled

very low power (<300uW/channel at 5pF), low noise (800 electrons at 5pF)

measured similar performance in test beam, analysis ongoing

test system, beam telescope and DAQ ready for future tests

CBC2 design close to submission