WIT2012 Workshop on Intelligent Trackers

Report of Contributions

https://indico.cern.ch/e/154525

Contribution ID: **1** Type: **not specified**

A tracker for the novel mu3e experiment based on high voltage monolithic active pixel sensors

Thursday 3 May 2012 20:00 (1 hour)

The proposed mu3e experiment will study the lepton flavor violating decay mu->eee which is strongly (10^-50) suppressed in the standard model, but enhanced to observable levels in many models for new physics. In order to achieve the proposed branching ratio sensitivity of 10^-16 the detector has to have high rate capability and good background suppression, which in turn requires excellent momentum and vertex resolution.

The mu3e detector consists of two double layers of high voltage monolithic active pixel sensors (HV-MAPS) around a target double cone. To minimize multiple scattering of the low energetic decay electrons (<53 MeV), an ultralight layer design is proposed, with HV-MAPS thinned to 50 um. With on-sensor pre-amplification, discrimination and zero-suppression a separate read-out chip can be omitted, which further reduces the material budget. The detector design will be discussed and results from the characterization of the HV-MAPS prototype in 180 nm technology will be shown.

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Presenter: WIEDNER, Dirk (Ruprecht-Karls-Universitaet Heidelberg (DE))

Session Classification: Posters

Contribution ID: **4** Type: **not specified**

Nanosecond Timing Resolution with the APV25

Thursday 3 May 2012 20:00 (1 hour)

In an environment with high occupancy and continuous collisions, conventional readout of silicon strip detectors will lead to ambiguities in the time domain. This problem can in principle be minimized by reducing the shaping time, but that approach is limited by the noise penalty.

The APV25 chip, originally developed for the CMS experiment, includes an on-chip switched capacitor filter performing a "deconvolution" on three consecutive samples of the shaped signal in order to narrow down the signal to a single bunch crossing.
Unfortunately, this feature requires clock synchronous beam and thus cannot be used in case of quasi-continuous collisions which will occur in the future Belle II experiment at KEK (Japan). Nonetheless, multiple samples along the shaper output can be processed outside of the APV25 in order to determine both peak amplitude and timing of the sampled signal regardless of the asynchronous relation between particle and sampling, achieving a time resolution of a few nanoseconds. Moreover, the data processing can be performed in real-time using look-up tables in an FPGA. This allows comparing the timing of each hit to the trigger timing and discarding off-time background immediately, saving bandwidth, processing power and storage capacity in the subsequent DAQ.

Apart from the hit time finding, the future readout module for the Belle II Silicon Vertex Detector will also perform pedestal subtraction, common mode correction and zero suppression by FPGA firmware. In addition, the incoming analog data will be conditioned by a digital FIR filter. We will present the concept, existing prototypes, results from several beam tests on various (mostly double-sided) silicon strip detectors and what is under construction for the Belle II experiment.

Author: Dr FRIEDL, Markus (Austrian Academy of Sciences (AT))

Co-authors: Mr IRMLER, Christian (Austrian Academy of Sciences (AT)); STEININGER, Helmut (Austrian Academy of Sciences (AT))

Presenter: Dr FRIEDL, Markus (Austrian Academy of Sciences (AT))

Session Classification: Posters

Contribution ID: **6** Type: **not specified**

3D Vertical Integration Technology for Fast Pattern Recognition

Saturday 5 May 2012 11:00 (30 minutes)

Hardware-based pattern recognition for fast triggering on particle tracks has been successfully used in high-energy physics experiments for some time. The CDF Silicon Vertex Trigger (SVT) at the Fermilab Tevatron is an excellent example. The method used there, developed in the 1990's at Pisa, is based on algorithms that use a massively parallel associative memory architecture to identify patterns efficiently at high speed. However, due to much higher occupancy and event rates at the LHC, and the fact that the LHC detectors have a much larger number of channels in their tracking detectors, there is an enormous challenge in implementing fast pattern recognition for a track trigger, requiring about three orders of magnitude more associative memory patterns than what was implemented in the original CDF SVT. Scaling of current technologies is unlikely to satisfy the scientific needs of the future, and investments in transformational new technologies need to be made. As Moore's law is approaching severe limitations, it is expected that 3D Vertical Integration Technology will be the next scaling engine. More importantly, in certain cases, the 3D technology also provides novel design opportunities that are simply not possible in 2D and this is the case for fast pattern recognition, such as the associative memory approach. In this talk, we will present a new concept of using the emerging 3D vertical integration technology to significantly advance the state-of-the-art for fast pattern recognition within and outside HEP. A R&D collaboration based on this concept is being developed and the status of this R&D project as well as the future direction will be presented as well.

Authors: HOFF, Jim (Fermilab); LIU, Tiehui Ted (Fermilab)

Co-authors: DEPTUCH, Grzegorz (FERMILAB); Mr YAREMA, Ray (FNAL)

Presenter: LIU, Tiehui Ted (Fermilab)

Session Classification: Real time pattern-recognition and advanced algorithms

Track Classification: Real time pattern-recognition and advanced algorithms

Contribution ID: **7** Type: **not specified**

Instrumentation of a track trigger with double buffer front-end architecture

Thursday 3 May 2012 12:00 (30 minutes)

The planned high luminosity upgrade for the LHC (SLHC), will increase the collision rate in the ATLAS detector by approximately a factor 5 beyond the present LHC design goal, while also increasing the number of pile-up collisions in each event by a similar factor. This means that the level-1 trigger must achieve a higher rejection factor in a more difficult environment. We describe a possible design which splits the level-1 trigger into a two-level system, where the first level, using only calorimetry and muon chambers, defines regions of interest in the tracker from which to extract information for a second, refined trigger. The use of a two-buffer front-end architecture will allow a significantly longer decision time to move data off the detector keeping the data bandwidth and buffer sizes moderate. We will describe the implementation of the scheme in the ATLAS tracker front-end electronics and the simulated performance of the system. Results on thresholds, rejection, bandwidth and trigger latency will be shown and compared with the present requirements for SLHC upgrade in ATLAS.

Authors: KONSTANTINIDIS, Nikolaos (University College London (GB)); BRENNER, Richard (Uppsala University (SE))

Presenter: WARDROPE, David (University College London (UK))

Session Classification: Application of intelligent detectors / Coupled sensors and monolithic architectures

Track Classification: Applications of intelligent detectors

Contribution ID: **8** Type: **not specified**

A real-time clustering ASIC for the PXD in Belle II

Friday 4 May 2012 12:30 (30 minutes)

The grouping of data elements based on characteristic relations is known as clustering.
It can either be used for data compression in a DAQ chain, or even to calculate the characteristic trigger input values based on event data.
Driven by the requirements of the PXD detector in the Belle II experiment @KEK/Japan, a real-time clustering engine was developed.
This software-inspired hardware architecture is by a pipelined structure able to perform up to 50k times per second the full 2D clustering of the zero-suppressed data out of a detector array with 768x250 pixels with a up to 3% fill rate and only one frame latency.
Due to the scalable architecture of the clustering core, the engine can
be easily adapted to the specific needs of other target applications,
even to 3D or higher dimensional operation.
A first test chip in TSMC 65nm process technology is back from the production and goes now in initial tests.

Author: WASSATSCH, Andreas (MPI Physik / HLL)

Co-authors: MOSER, Hans-Guenther (MPI fuer Physik / HLL); RICHTER, Rainer (MPI Physik / HLL)

Presenter: WASSATSCH, Andreas (MPI Physik / HLL)

Session Classification: On-module electronic circuits (3D and conventional), intra-module and off-detector communication

Track Classification: Real time pattern-recognition and advanced algorithms

Contribution ID: **9** Type: **not specified**

A Fast Clustering Block for Silicon Strip Seeded Track Trigger

Friday 4 May 2012 15:00 (30 minutes)

A viable seeded track trigger for a high rate collider detector environment must have excellent angular precision, response times commensurate with beam crossing rate and low mass. We have designed a fast clustering block servicing 128 contiguous strips to be included in an LHC upgrade silicion strip readout ASIC with these objectives in mind. The block is based on the presence of an analog front end with binary (threshold determined) strip readout latched at each beam crossing. Combinatorial logic tests for the presence of one or two adjacent strips over threshold, a cluster, at each beam crossing and records the seven bit address of up to two clusters via a high speed LVDS output. A correlator chip receives this data and looks for coincident hits between silicon strip layers. Since the clustering output will report the presence of one or two hit strips, a half strip width (˜40um) resolution may be possible for each cluster. Our results show that the combinatorial clustering logic will settle within 6ns. Assuming a beam crossing rate of 40MHz, serialized data shifted out at 640MHz will meet the required beam synchronous update rate so that the correlator chip will receive cluster information delayed by a fixed offset of only two beam crossings. Present power estimates suggest that the fast cluster block with LVDS driver will consume less than 20mW.

Summary

See Attached

Author: Mr NEWCOMER, Mitch (University of Pennsylvania)

Co-authors: Mr AMOGH HALGERI, Amogh (University of Pennsylvania EE dept.); Dr GARCIA-SCIVERES, Maurice (Lawrence Berkeley Laboratory); Mr DRESSNANDT, Nandor (University of Pennsylvania)

Presenter: Mr NEWCOMER, Mitch (University of Pennsylvania)

Session Classification: On-module electronic circuits (3D and conventional), intra-module and off-detector communication

Track Classification: On-module electronic circuits (3D and conventional), intra-module and off-detector communication

Contribution ID: **10** Type: **not specified**

Application for front end intelligence in gaseous pixel detectors for triggering

Thursday 3 May 2012 11:30 (30 minutes)

The combination of gaseous detectors with pixel readout chips gives unprecedented hit resolution (improving from O(100 um) for wire chambers to 10 um), as well as high-rate capability, low radiation length and giving in addition angular information on the local track. These devices measure individually every electron liberated by the passage of a charged particle, leading to a large quantity of data to be read out. Typically an external trigger is used to start the read-out.

We are investigating the addition of local intelligence to the pixel read-out chip. A first level of processing detects the passage of a particle through the gas volume, and accurately determines the time of passage. A second level measures in an approximate but fast way the tilt-angle of the track. This can be used to trigger a third stage in which all hits associated to the track are processed locally to give a least-squares-fit to the track. The chip can then send out just the fitted track parameters instead of the individual electron coordinates.

This self-triggering capability could have a major application in the level-1 track trigger proposed for the ATLAS upgrade for the sLHC. I will briefly summarise the track trigger requirements for the ATLAS Upgrade and highlight the advantages of a gaseous detector for this application, followed by discussing one approach to the local intelligence needed to realise such a trigger.

Summary

This talk presents the possibilities of using local intelligence in a pixel readout chip coupled to a gaseous detector for trigger purposes. It could have applications in fast track triggers at the LHC detector upgrades.

Author: Dr HESSEY, Nigel (NIKHEF (NL))

Co-authors: VAN DER GRAAF, Harry (NIKHEF (NL)); VERMEULEN, Joseph (NIKHEF (NL))

Presenter: Dr HESSEY, Nigel (NIKHEF (NL))

Session Classification: Application of intelligent detectors / Coupled sensors and monolithic architectures

Track Classification: Applications of intelligent detectors

Contribution ID: **11** Type: **not specified**

Modulator Based High Bandwidth Optical Links for HEP Experiments

Thursday 3 May 2012 20:00 (1 hour)

Optical links will be an integral part of intelligent tracking systems at various scales from coupled sensors through intra-module and off detector communication. These links will be particularly useful if they utilize light modulators which are very small, low power , high bandwidth, and are very rad-hard.

Because of concern with the reliability, bandwidth, power, and mass of future optical links in LHC experiments, we are investigating the use of CW lasers external to the tracking, along with light modulators at the detector, as an alternative to VCSELs.

We have constructed a test system with 3 such links, each operating at 10 Gb/s. We present the quality of these links (jitter, rise and fall time) and eye mask margins (10GbE) for 3 different types of modulators:
LiNbO3-based, InP-based, and Si-based.

We present the results of radiation hardness measurements with up to ˜10ˆ12 protons/cmˆ2 and ˜65 krad total ionizing dose (TID), confirming no single event effects (SEE) at 10Gb/s with all 3 types of modulators.

In addition we present results on free space data links, utilizing
steering by MEMS mirrors and optical feedback paths for the control loop. Laser, modulator, and lens systems used are described, as well as two different electronic systems for a free space steering feedback loop. Results at 10 Gb/s are shown.

Some future developments of optical modulator-based high bandwidth
optical readout systems, and applications based on both fiber and
free space data links, such as local triggering and data readout
and trigger-clock distribution, are also discussed.

Summary

Optical links will be an integral part of intelligent tracking systems at various scales from coupled sensors through intra-module and off detector communication. These links will be particularly useful if they utilize light modulators which are very small, low power , high bandwidth, and are very rad-hard.

Because of concern with the reliability, bandwidth, power, and mass of future optical links in LHC experiments, we are investigating the use of CW lasers external to the tracking, along with light modulators at the detector, as an alternative to VCSELs.

We have constructed a test system with 3 such links, each operating at 10 Gb/s. We present the quality of these links (jitter, rise and fall time) and eye mask margins (10GbE) for 3 different types of modulators:
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Some future developments of optical modulator-based high bandwidth optical readout systems, and applications based on both fiber and free space data links, such as local triggering and data readout and trigger-clock distribution, are also discussed.

Author: UNDERWOOD, David (Argonne National Laboratory (US))

Co-authors: STANEK, Bob (Argonne National Laboratory (US)); Dr LOPEZ, Daniel (CNM, Argonne National Laboratory); Dr FERNANDO, Waruna (Argonne National Laboratory)

Presenters: STANEK, Bob (Argonne National Laboratory (US)); UNDERWOOD, David (Argonne National Laboratory (US)); Dr FERNANDO, Waruna (Argonne National Laboratory)

Session Classification: Posters

Contribution ID: **12** Type: **not specified**

The First Prototype for the FastTracker Processing Unit

Thursday 3 May 2012 20:00 (1 hour)

Modern experiments search for extremely rare processes hidden in much larger background levels. As the experiment complexity and the accelerator backgrounds and luminosity increase we need increasingly complex and exclusive selections. We present the first prototype of a new Processing Unit, the core of the FastTracker processor for Atlas, whose computing power is such that a couple of hundreds of them will be able to reconstruct all the tracks with transverse momentum above 1 GeV in the ATLAS events up to Phase II instantaneous luminosities (5×1034 cm-2 s-1) with an event input rate of 100 kHz and a latency below hundreds of microseconds. We plan extremely powerful, very compact and low consumption units for the far future, essential to increase efficiency and purity of the Level 2 selected samples through the intensive use of tracking.
This strategy requires massive computing power to minimize the online execution time of complex tracking algorithms. The time consuming pattern recognition problem, generally referred to as the "combinatorial challenge", is beat by the Associative Memory (AM) technology [2] exploiting parallelism to the maximum level: it compares the event to pre-calculated "expectations"or "patterns" (pattern matching) at once looking for candidate tracks called "roads". This approach reduces to linear the typical exponential complexity of the CPU based algorithms. The problem is solved by the time data are loaded into the AM devices.
We describe the board prototypes that face the very challenging aspects of the Processing Unit: a huge amount of detector clusters ("hits") must be distributed at high rate with very large fanout to all patterns (10 Millions of patterns will be located on 128 chips placed on a single board) and a huge amount of roads must be collected and sent back to the FTK post-pattern-recognition functions. The Processing Unit consists of a 9U VME board, the AMBoard, controlled by an AUX card on the back of the crate. The AMBoard has a modular structure consisting of 4 mezzanines, the Local Associative Memory Banks (LAMB). Each LAMB contains 32 Associative Memory (AM) chips, 16 per side. The proto - AUX card provides hits on 8 buses for a total of 12 Gbits/sec to the AMBoard through 12 high frequency serial links and will sink the found roads trough other 16 high frequency serial links (24 Gbits/sec). A special P3 connector allows the communication between the front and rear boards placed on the same VME slot. A custom board profile has been studied and simulated at the CAD to guarantee a perfect board-to-board closure of the P3 connector without a backplane support in that region. A network of high speed serial links characterize the bus distribution on the AMBoard. The hit buses are fed to the four LAMBs and distributed to the 32 AM chips on the LAMB, through fanout chips. The LAMB realization has represented a significant technological challenge, due to the high density of chips allocated on both sides, and to the use of advanced packages and high frequency serial links.

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BERTI, Fabrizio (INFN Sezione di Milano (INFN)); TANG, Fukun (University of Chicago (US)); TOMPKINS, Lauren Alexandra (Lawrence Berkeley National Lab. (LBNL)); BERETTA, Matteo Mario (Istituto Nazionale Fisica Nucleare (IT)); SHOCHET, Mel (University of Chicago (US)); BOGDAN, Mircea (The University of Chicago); GIANNETTI, Paola (Sezione di Pisa (IT))

Presenter: MAGALOTTI, Daniel (Universita e INFN (IT))

Session Classification: Posters

Contribution ID: **13** Type: **not specified**

A Low Mass On-chip Readout Scheme for Double-sided Silicon Strip Detectors

Thursday 3 May 2012 20:00 (1 hour)

B-factories like the KEK-B in Tsukuba, Japan, operate at relatively low energies and thus require detectors with very low material budget inside the sensitive volume in order to minimize multiple scattering. On the other hand, front-end chips with short shaping time like the APV25 have to be placed as close to the sensor strips as possible to avoid excessive noise, which is mainly caused by the capacitive load of the input amplifiers.
In order to achieve both - minimal material budget and low noise - we developed a readout scheme for double-sided silicon detectors, where the APV25 chips are placed on a single flexible circuit, which is glued onto the sensor. While the top-side strips are directly connected to the chips by wire-bonding and a small pitch adapter, those of the bottom-side are attached by two flexible circuits, which are bent around the edge of the sensor.
This so-called "Origami"design will be utilized to build the Silicon Vertex Detector of the future Belle II experiment, which will consist of 4 layers made from ladders with up to five double-sided silicon strip sensors in a row. Each ladder will be supported by two carbon fiber reinforced ribs, with a very light-weight Airex styrofoam core.
Placing the readout chip onto the sensor also requires sufficient cooling, which will be done by a highly efficient two-phase CO2 system. Thanks to the Origami concept, all APV chips inside the active Volume are aligned in a row and thus can be cooled by a single thin cooling pipe per ladder.
We will present the concept and the assembly procedure of the Origami chip-on-sensor modules, and show results of beam tests which were performed at CERN on prototype modules.

Author: Mr IRMLER, Christian (HEPHY Vienna)

Co-authors: Mrs FRANKENBERGER, Annekathrin (HEPHY Vienna); Mr GFALL, Immanuel (HEPHY Vienna); Dr FRIEDL, Markus (HEPHY Vienna); Mr SCHMID, Siegfried (HEPHY Vienna)

Presenter: Mr IRMLER, Christian (HEPHY Vienna)

Session Classification: Posters

Contribution ID: **14** Type: **not specified**

3D Monolithically Stacked CMOS Active Pixel Sensor Detectors for Particle Tracking Applications.

Thursday 3 May 2012 18:00 (30 minutes)

Typical tracking systems for particle trajectory reconstruction in High Energy Physics experiments are based on different separated sensing layers, featuring pixels and/or strips sensitive elements.

In this work we propose an innovative approach to particle tracking based on CMOS Active Pixel Sensors layers, monolithically integrated in a all-in-one chip featuring multiple, stacked, fully functional detector layers capable to provide momentum measurement (particle impact point and direction) within a single detector. This will results in a very low material detector, thus dramatically reducing multiple scattering issues.

To this purpose, we rely on the capabilities of the CMOS vertical scale integration (3D IC) technology. The chip prototype has been fabricated within a multi-project run using a 130nm CMOS Chartered/Tezzaron technology [1], featuring two layers bonded face-to-face (Fig. 1). Several test structures have been integrated, namely single pixels, as well as small matrices, e.g. featuring 5x5 and 16x16 pixels. Each pixel is 10x10 micrometers, with different sensitive element (photodiode) dimensions.

Tests have been carried out both on single sided (single tier) detectors (2D) and on full 3D structures, providing the functionalities of both tiers. To this purpose, laser scans have been carried out using highly focussed spot size (below two micrometers at 780nm and 531nm wavelengths), obtaining coincidence responses of the two layers (Fig. 2). Tests have been made as well with X-ray sources an on the electrons/positrons Beam Test Facilities at the INFN LNF Frascati (Rome), Italy.

[1] 3DIC Consortium http://3dic.fnal.gov/

Author: Dr PASSERI, Daniele (University of Perugia)

Co-authors: MARRAS, Alessandro (Deutsches Elektronen-Synchrotron); MAGALOTTI, Daniel (Universita e INFN (IT)); Dr SERVOLI, Leonello (Universita e INFN (IT)); PLACIDI, Pisana; Dr MEROLI, Stefano (I.N.F.N.)

Presenter: Dr PASSERI, Daniele (University of Perugia)

Session Classification: Application of intelligent detectors / Coupled sensors and monolithic architectures

Track Classification: Coupled sensors and monolithic architectures

Contribution ID: **15** Type: **not specified**

The Two 3Ds Combined: Tiles for Large Area Intelligent Arrays

Friday 4 May 2012 09:00 (30 minutes)

Future intelligent tracking systems are likely to require large area sensor modules with finely segmented, intelligent readout. However conventional module construction, with readout bonded at the periphery and significant sensor dead area, makes it difficult to build large area pixelated modules with good yield,low mass and small dead area. The combination of 3D active edge sensors and 3D (vertically integrated) electronics solves these problems by enabling the fabrication of readout chip/sensor tiles which can be butted on four sides and are readout through the top surface. We describe the concept for these "large area array" tiles and the design of active edge sensors and test modules currently being fabricated. We describe applications for the CMS Track Trigger as well as vertex detectors for future lepton colliders.

Author: Dr LIPTON, Ronald (Fermi National Accelerator Lab. (US))

Presenters: JOHNSON, Marvin (Fermi National Accelerator Lab.); Dr LIPTON, Ronald (Fermi National Accelerator Lab. (US))

Session Classification: Development of critical technologies and system integration

Track Classification: Development of critical technologies and system integration

Contribution ID: **16** Type: **not specified**

Active Pixel Sensors in high-voltage CMOS technologies for ATLAS

Thursday 3 May 2012 17:30 (30 minutes)

Active pixel sensors in high-voltage CMOS technologies combine the possibility to equip the sensor segments with complex electronics and a drift-based signal collection. High radiation tolerance has been demonstrated, which makes the technology interesting for LHC applications.
We have designed a small pixel sensor demonstrator that can be readout using existing pixel or strip-readout systems. In this way, we replace the presently used diode-based sensors with "intelligent" pixel sensors, which should improve the characteristics of the detector. Smaller pixel size, clustering, or simultaneous readout of two sensor layers, are theoretically possible.

Author: Dr PERIC, Ivan (Ruprecht-Karls-Universitaet Heidelberg (DE))

Presenter: Dr PERIC, Ivan (Ruprecht-Karls-Universitaet Heidelberg (DE))

Session Classification: Application of intelligent detectors / Coupled sensors and monolithic architectures

Track Classification: Coupled sensors and monolithic architectures

Contribution ID: **17** Type: **not specified**

Quadruple well CMOS MAPS for particle tracking with pixel-level analog processing, discrimination and time stamping

Thursday 3 May 2012 20:00 (1 hour)

In the last decade, the use of standard deep submicron CMOS technologies for the implementation of monolithic active pixel sensors for HEP experiments has been thoroughly investigated. One of the main issues with this approach is the fact that the charge collection efficiency may be negatively affected by the presence of competitive N-wells used to integrate PMOS transistors in the readout chain. These N-wells act as parasitics collecting electrodes subtracting part of the charge generated by a minimum ionizing particle (MIP) from the sensor. On the other hand, PMOS transistors are needed to design high performance, low power analog and digital blocks.
A novel approach for isolating the PMOS competitive N-wells is based on the use of a planar 180 nm CMOS process with quadruple well called INMAPS. By means of an additional processing step, an high energy deep P-well implant is deposited beneath the N-wells (except for the N-well diodes acting as collecting electrodes). This implant creates a barrier for the charge diffusing in the epitaxial layer, preventing it from being collected by the positively biased N-wells of the in-pixel circuits and allowing a theoretical charge collection efficiency of 100%. The NMOS transistors are designed in heavily doped P-wells located over a lightly P-doped epitaxial layer about 10 μm thick, which has been grown upon a relatively low resistivity substrate. The epitaxial layer, featuring a higher resistivity than both the deep P-well and the substrate, also plays an important role in the improvement of the charge collection properties: in fact, the presence of two small potential barriers (deep P-well/epitaxial layer or P-well/epitaxial layer and epitaxial layer/substrate) keeps the carriers within the epitaxial layer, preventing them from diffusing through the substrate. The foundry provides two different typologies of epitaxial layer: standard resistivity (about 50 Ω·cm) and high resistivity (1 kΩ·cm). Two lots of chips called Apsel4well differing for the resistivity of the epitaxial layer, have been fabricated (and delivered at the beginning of 2012). Comparing the charge collection efficiency of the two different approaches will be possible to further investigate the role played by the epitaxial layer resistivity on this performance.
The Apsel4well pixel features a 50 μm pitch, complying with the requirements of the SVT Layer0 of the SuperB experiment. The collecting electrode consists of 4 interconnected N-well square diodes each with a 1.5 μm side. The sensor is read out by a classical channel for capacitive detectors including a charge preamplifier, a shaper and a threshold discriminator, followed by the in-pixel readout logic. Other than analog smaller (3x3) pixel matrices and single channels, the Apsel4well chip also includes a 32x32 matrix which implements a sparsified readout architecture with time stamping in order to deal with the large amount of data expected in the experiments at the high luminosity colliders.

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Presenter: Dr ZUCCA, Stefano (University of Pavia and INFN)

Session Classification: Posters

Contribution ID: **18** Type: **not specified**

MCM-D Technology for Silicon Strip Frontend Hybrids

Friday 4 May 2012 09:30 (30 minutes)

Multi-chip Modules - Deposited (MCM-D) technology can be applied to silicon strip modules and promises advantages in terms of integration complexity and material budget. The principle is to deposit alternating dielectric and metal layers directly on the silicon sensor, building up a PCB like structure. With lithographic techniques traces and vias are etched with high resolution creating a circuit replacing the pitch adaptor, wire bonds and electronics hybrid.

This paper reports on a feasibility study performed in the context of the Atlas Upgrade. The technology was evaluated in two prototype processing runs. The first prototypes had a single dielectric and metal layer deposited on a silicon strip sensor, with the purpose of evaluating the change in performance due to the post-processing and the presence of a ground plane. Sensor parameters were measured before and after irradiation up to 10ˆ16 n_eq/cmˆ2 and charge collection efficiency was measured for several doses. A non-irradiated sensor was measured in a beam test yielding signal height and resolution for regions with and without ground plane. The second prototype was a fully functional 20-chip front-end hybrid with five metal layers build on a blank silicon sensor. The hybrid has the same performance as an identical circuit built in kapton technology.

Summary

The next generation silicon tracking detectors are tending to a higher density of read-out channels over a large area. Hence an increased level of integration of the detector modules is desirable. Multi-chip Modules - Deposited (MCM-D) technology applied to silicon strip modules and promises advantages in terms of integration complexity and material budget. The principle is to deposit alternating dielectric and metal layers directly on the silicon sensor, building up a PCB like structure. With lithographic techniques traces and vias are etched with high resolution creating a circuit replacing the pitch adaptor, wire bonds and electronics hybrid.

The features sizes possible are smaller compared to traditional PCB technologies. Minimum track width and spacing is in the order of 10-30 um and vias are in the order of 50 um. Layer thicknesses are typically 3-15 um for dielectric layers and 1-3 um for metal layers.

This paper reports on a feasibility study performed in the context of the Atlas Upgrade. The technology was evaluated in two prototype processing runs performed by a semi-industrial partner (Acreo, Norrkoping, Sweden). The first prototypes had a single dielectric and metal layer deposited on a silicon strip sensor, with the purpose of evaluating the change in performance due to the post-processing. The

design had via-connections to the strip pads and different types of ground planes covering the sensor area. This corresponds to the first layer of processing in a full design, hence giving the bulk of the change in performance of the sensor.

Sensor parameters such as I/V, C/V, C_is and R_is were measured for non-irradiated samples and for an array of doses up to 10ˆ16 n_eq/cmˆ2. Charge collection efficiency was also measured for the same doses. A non-irradiated sensor was measured in a beam test yielding signal height and resolution for regions with and without ground plane.

The second prototype was a fully functional 20-chip front-end hybrid with five metal layers build on a blank silicon sensor. The hybrid is digitally fully functional and shows the same analogue performance parameters (noise, gain, stability) as an identical circuit built in kapton technology.

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Session Classification: Development of critical technologies and system integration

Track Classification: Development of critical technologies and system integration

Contribution ID: **19** Type: **not specified**

A Fast Hardware Tracker for the ATLAS Trigger System

Thursday 3 May 2012 09:30 (30 minutes)

Selecting interesting events with triggering is very challenging at the LHC due to the busy hadronic environment. Starting in 2014 the LHC will run with an energy of 14TeV and instantaneous luminosities which could exceed 10ˆ34 interactions per cmˆ2 per second. The triggering in the ATLAS detector is realized using a three level trigger approach, in which the first level (L1) is hardware based and the second (L2) and third (EF) stage are realized using large computing farms.

It is a crucial and non-trivial task for triggering to maintain a high efficiency for events of interest while suppressing effectively the very high rates of inclusive QCD processes, which constitute mainly background. At the same time the trigger system has to be robust and provide sufficient operational margins to adapt to changes in the running environment. In the current design, track reconstruction can be performed only in limited regions of interest at L2 and the CPU requirements may limit this even further at the highest instantaneous luminosities.

Providing high quality track reconstruction over the entire detector volume for the L2 trigger decision would allow gains in efficiency and background rejection for triggers on tau leptons, b-hadrons and help reduce the luminosity dependence of isolation requirements for electrons and muons. The Fast Track Trigger (FTK) is an ongoing upgrade project aimed at providing track reconstruction over the |eta|<2.5 region using the silicon microstrip and pixel detectors. Pattern recognition and track fitting are executed in a hardware system utilizing massive parallel processing and achieve a tracking performance close to that of the global track reconstruction. The FTK system's design, based on a mixture of advanced technologies (FPGAs, ASICs, Associative Memories), and expected physics performance will be presented.

Summary

A track reconstruction system for the trigger of the ATLAS detector at the Large Hadron Collider is described. The Fast Tracker is a highly parallel hardware system designed to operate at the Level-1 trigger output rate. It will provide high-quality tracks reconstructed over the entire inner detector by the start of processing in the
Level-2 trigger. The system is based on associative memories for pattern recognition and fast FPGA' s for track reconstruction. Its design and expected performance under instantaneous luminosities up to 3x10ˆ34/cm2ˆ/s are discussed.

Author: Dr PENNING, Bjorn (University of Chicago (US))

Presenter: Dr PENNING, Bjorn (University of Chicago (US))

Session Classification: Application of intelligent detectors / Coupled sensors and monolithic architectures

Track Classification: Applications of intelligent detectors

Contribution ID: **20** Type: **not specified**

Multi_Gigabit wireless data transfer at 60 GHz

Friday 4 May 2012 16:30 (30 minutes)

The data transfer rate from highly granular tracking detectors are limited today by the available bandwidth in the readout links what prevents the detectors to be used for fast triggering.

MMwave technology is the next generation wireless technology that can provide multi-Gbps wireless connectivity for short distances between electronics [1]. Since the carrier frequency is higher (60 GHz), more data can be sent in a given period of time, by modulating the carriers amplitude, frequency or phase. The 60 GHz unlicensed frequency band is of particular interest for indoor point-to-point multi-gigabit due to its very low atmospheric attenuation and the large amount of spectral bandwidth (7-9 GHz). With such a bandwidth available and the optimum choice of modulation scheme, it would be possible to achieve a data rate in the 10's of Gbps, and could therefore be a suitable method to solve the data transfer rate problem. Furthermore, due to its small wave lengths at carrier frequency of 60 GHz (5mm), it becomes possible to integrate the antenna on-chip or in-package.
The narrow beams of millimeter wave also allow for deployment of multiple independent links in close proximity. That makes the wireless modules very suitable to pass data between tracking layers.
The high speed links are low mass, low power, more secure and does not interfere with other wireless technologies for short distance data transfer.

In this context a multi-Gigabit wireless readout chip operating in the 60 GHz region is currently under development at the University of Heidelberg. The design is based on the well known superheterodyne transceiver architecture with approximately 3Gb/s throughput, x mW transmit power, 5 dB receiver noise figure (NF) and high gain omni-directional antennas. With such specifications, the link budget calculation shows that a range of few meters is possible. The targeted data rate for our first prototype is 3Gbps.

In this talk the key building blocks necessary to realize this architecture will be described.
Silicon-Germanium (SiGe) Heterojunction Bipolar Transistors (HBTs) BiCMOS is chosen as the technology to demonstrate the concept. In addition, we will also report on the current status of the design and performance obtained in simulation of our Millimeter Wave Chip development for a possible upgrade of the ATLAS Fast Tracker, in terms of area, estimated power consumption, data rate, and the emerging 3-D technology implementation scenarios that is particularly beneficial for 3-D wireless chip development.

[1] R. Brenner. "Multigigabit wireless transfer of trigger data through millimetre wave technology"
.
2010 JINST 5 c07002

Author: Mr SOLTVEIT, Hans Kristian (Ruprecht-Karls-Universitaet Heidelberg (DE))

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Session Classification: On-module electronic circuits (3D and conventional), intra-module and off-detector communication

Track Classification: On-module electronic circuits (3D and conventional), intra-module and off-detector communication

Contribution ID: **22** Type: **not specified**

A Dedicated Electronics-Based Pixel Tracking System for CMS for HL-LHC Luminosities

Thursday 3 May 2012 20:00 (1 hour)

Addressing challenges of triggering in the High Luminosity LHC environment require development of fast and efficient track-based triggering methods. We consider a dedicated electronics-based system, which could be used as a co-processor performing fast tracking using data from the pixel detector for events passing the CMS Level-1 trigger. In this scenario, a list of tracks above a certain threshold will be made available for use at the very early stages of the software-based CMS High Level trigger allowing fast and efficient reduction in the rate of events necessary to allow performing more complex and time-consuming reconstruction methods on surviving events. While primarily targeted for later stages of "Phase I"upgrades, the same system can be utilized in the Phase II luminosity regime as part of the Level-1 trigger logic. In this case, the system will take advantage of the increased Level-1 trigger latency to perform tracking in regions of interest identified by the Level-1 calorimeter or muon triggers. In this scenario, the system will either confirm or deny presence of an energetic track and relay that information back to the Level-1 trigger decision logic before the final Level-1 decision to accept or reject an event is made.

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Presenter: GILMORE, Jason (Texas A & M University (US))

Session Classification: Posters

Contribution ID: **23** Type: **not specified**

The ultra low mass cooling system of the Belle II DEPFET detector

Thursday 3 May 2012 20:00 (1 hour)

The new e^+e^- colliders impose unprecedented demands to the performance of the vertex detectors. To achieve the required resolution in the vertex reconstruction, besides highly segmented pixel detectors, the material budget has to be kept at very low levels to reduce the multiple Coulomb scattering. These requirements are even more challenging in the case of the new Japanese Super Flavour Factory (SuperKEKB) where the very low momentum of the particles in the final state requires a vertex detector with less than 0.2%~X_0 per layer, together with 50x50~μm^2 pixels, to achieve the aimed resolution of 8.5~μm.

As a consequence, there is an obvious impact on the cooling system, that has to be carefully designed, not allowing active cooling pipes inside the acceptance region. Due to the low power dissipation of the DEPFET sensor and the special geometry of the detectors (with the front end electronics placed at both ends of the ladder), the system can be chilled using 2-phase CO_2 cooling through the massive support structures outside of the acceptance, while the sensitive area relies on forced convection with cold dry air.

In the talk not only full thermal simulations will be presented but also measurements done with a real mock up, showing that a proper cooling of the vertex detector can be made using this approach.

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Presenter: Dr MARINAS PARDO, Carlos (Bonn University)

Session Classification: Posters

Contribution ID: **24** Type: **not specified**

Interconnect issues for the CMS 3-D track trigger

Thursday 3 May 2012 20:00 (1 hour)

The 3-D track trigger concept being developed for the CMS upgrade involves interconnections for signals to be transmitted between various layers of sensors and readout electronics. In this design, the two sensitive layers are separated by an interposer, which provides the lever arm for measuring transverse momenta. Such an assembly would require new challenges for bump-bonding of large arrays. Progress in various techniques being investigated for this purpose will be presented. Sequential bump-bonding steps using solders with different melting points will be described. Plans for achieving high yields in assembly will be discussed.

Author: Prof. TRIPATHI, Mani (UC Davis)

Presenter: Prof. TRIPATHI, Mani (UC Davis)

Session Classification: Posters

Contribution ID: **25** Type: **not specified**

A fast digital readout architecture for vertically integrated pixel sensors

Thursday 3 May 2012 20:00 (1 hour)

A digital architecture for fast sparsified readout has been developed for the implementation of wide 3D pixel sensors. The Italian VIPIX collaboration is realizing two prototypes exploiting the Tezzaron-Chartered vertical integration process in order to build a 12k-pixel 3D deep n-well MAPS sensor, and a 3D 4k-pixel front-end chip, with 50 um pitch, for a fully depleted silicon sensor. In both cases the digital and analog circuits are implemented on dedicated tiers in order to reduce the digital noise induction and enhance the digital logic at pixel level. The dense in-pixel logic allows for innovative sparsified hit extraction techniques, in order to reduce the pixel occupancy. The readout logic we propose can face an input hit rate of the order of 100MHz/cm2 and allows a time resolution of 100 ns, in addition it can be configured to work in data-driven or triggered mode.
The technology process is a Chartered CMOS 130 nm, this feature size presents an intrinsic radiation tolerance and allow the use of foundry's standard cells. The architecture has been deeply investigated in terms of efficiency on a wide span of input parameters (hit rate, time resolution, trigger latency etc.) thanks to a parameterized VHDL synthesizable model, that has been designed to match even larger matrices of pixels. The model was stimulated within a complex test bench environment that included a Monte Carlo generator for the hit extraction, a simulation monitor and a C++ framework for the efficiency analysis and error detection. The flexibility of the code allow to easily tailor the architecture and of the test bench on different matrix dimensions: we observed this scalable architecture working properly even with bigger matrices, of the order of 50k pixels.
The paper presents the readout efficiency versus a variety of parameters as the clock rate, the pixel hit-rate and
the time-stamp resolution. The overall project leads to design a high-density thin vertex detector with an on-chip
sparsified digital readout system, for particle tracking, aimed at matching the requirements of future high-energy physics
experiments like SuperB.

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Presenter: Dr GIORGI, Filippo Maria (Universita e INFN (IT))

Session Classification: Posters

Contribution ID: **26** Type: **not specified**

Front end intelligence for triggering and local track measurement in gaseous pixel detectors

Friday 4 May 2012 15:30 (30 minutes)

The TimePix3 chip, currently being designed, is a pixel read-out chip with precision tdc (< 2 ns) recording hit arrival times and time-over-threshold. The read-out architecture [1] allows for continuous and trigger-free readout of sparsely distributed data with the rate up to 20 Mhits cmˆ-2 sˆ-1. It is designed for both solid-state pixel sensors and gaseous detectors. When used with gaseous detectors 3D tracking on one chip becomes possible. We are investigating the addition of fast pattern recognition of tracks in gaseous detectors in a successor chip to TimePix3. This includes recognition, without external trigger, of the passage of a particle, filtering of tracks to select only those with the desired angles, and fast measurement of the track. For example, tracks with small tilt angle correspond to high momentum tracks in solenoid-field inner trackers. Being able to select these fast and without external input could have applications at the future upgrades of the LHC detectors.

I will discuss the initial results in terms of which algorithms look most promising, with estimates of requirements for the extra electronics in terms of power, data rates, latency, and chip area.

[1] V. Gromov et al, “Development and Applications of the Timepix3 Readout Chip”, Proceedings of Science (PoS) of the 20th Anniversary International Workshop on Vertex Detectors (19-24 June 2011, Rust, Austria)
http://pos.sissa.it/archive/conferences/137/046Vertex%202011_046.pdf

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Session Classification: On-module electronic circuits (3D and conventional), intra-module and off-detector communication

Track Classification: Real time pattern-recognition and advanced algorithms

Contribution ID: **27** Type: **not specified**

A clusterization algorithm for ATLAS pixel upgrade.

Saturday 5 May 2012 08:30 (30 minutes)

The increase in the LHC luminosity and the reduction of the pixel size foreseen for the ATLAS pixel upgrade leads to an increased amount of data generated by the pixel detector at each beam crossing.
The bandwidth of the readout should be upgraded to deal with this increase of data, to keep a good detector efficiency.
Another approach, studied at LAPP, consists in decreasing the amount of data, by grouping adjacent pixels, thus forming clusters on the read-out chip. The analog center of gravity of the cluster can be determined directly inside the readout ASIC, and cluster can be classified at an early stage as "high Pt MIP-compatible" or not. Only the first category contains precise position information of interest to the tracking, and requires digitizing the barycenter position. The clusters in the second category contain only topological information and do not require digitization.
In addition to the data reduction, the early availability of cluster positions of high Pt tracks can speed up trigger algorithms,
The implementation of the local clustering algorithm takes advantage of TEZZARON 130nm 3D electronics, with analog readout of pixel, but it can also be applied to deep submicron 2D technology such 65 nm.
The architecture will be detailed and the bandwidth will be compared to the one of more classical approach readout electronics.

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Session Classification: Real time pattern-recognition and advanced algorithms

Track Classification: On-module electronic circuits (3D and conventional), intra-module and off-detector communication

Contribution ID: **29** Type: **not specified**

Monolithic Active Pixel Matrix with Binary Counters (MAMBO) ASIC, using a nested well structure to decouple the detector from the electronics

Thursday 3 May 2012 20:00 (1 hour)

Monolithic Active Matrix with Binary Counters (MAMBO) IV ASIC has been designed for detecting and measuring low energy X-rays from 6-12keV. A nested well structure with a buried n-well (BNW) and a deeper buried p-well (BPW) is used to electrically isolate the detector from the electronics. BNW acts as an AC ground to electrical signals and behaves as a shield. BPW creates a homogenous electric field in the entire detector volume. The ASIC consists of a matrix of 41×42 pixels, each of 105x105μm2. Each pixel contains analogue functionality accomplished by a charge preamplifier, CR-RC2 Shaper and a baseline restorer. It also contains a window comparator with Upper and Lower thresholds which can be individually trimmed by 4 bit DACs to remove systematic offsets. The hits are registered by a 12 bit counter which is reconfigured as a shift register to serially output the data from the entire ASIC.

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Presenter: KHALID, Farah (F)

Session Classification: Posters

Contribution ID: **30** Type: **not specified**

CBC2: a microstrip readout ASIC with coincidence logic for trigger primitives at HL-LHC

Friday 4 May 2012 14:30 (30 minutes)

We present the design of a new version of the CBC (CMS Binary Chip) ASIC for the readout of CMS Tracker Phase-two upgrade. CBC2, designed in 130nm CMOS, doubles the input channels to 254 and will be bump-bonded to the substrate. The ASIC is designed to instrument double layer modules in the outer tracker, consisting of two overlaid silicon sensors with aligned microstrips, and incorporates the logic to identify L1 trigger primitives in the form of "stubs": high transverse-momentum candidates which are isolated from the low momentum background by selecting correlated hits between two closely separated microstrip sensors. The functionality of the coincidence logic, which includes rejection of wide clusters and offset correction to account for the position of the module in the R-Φ plane, is described in detail.

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Presenter: BRAGA, Davide (STFC - Science & Technology Facilities Council (GB))

Session Classification: On-module electronic circuits (3D and conventional), intra-module and off-detector communication

Track Classification: On-module electronic circuits (3D and conventional), intra-module and off-detector communication

Contribution ID: **31** Type: **not specified**

The new variable resolution Associative Memory for Fast Track finding

Saturday 5 May 2012 10:00 (30 minutes)

We describe a VLSI processor for pattern recognition based on Content Addressable Memory (CAM) architecture,
optimized for on-line track finding in high-energy physics experiments.
We have developed this device using 65 nm technology combining a full custom CAM cell with standard-cell control logic.
The customized design maximizes the pattern density, minimizes the power consumption and implements the
functionalities needed for the planned Fast Tracker, an ATLAS trigger upgrade project at LHC.
We introduce a new variable resolution pattern matching technique using "don't care"bits to set the pattern-matching
window for each pattern and each layer can be independently.

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Session Classification: Real time pattern-recognition and advanced algorithms

Track Classification: Real time pattern-recognition and advanced algorithms

Contribution ID: **32** Type: **not specified**

Online tracking applications of the general purpose EDRO Board

Thursday 3 May 2012 20:00 (1 hour)

The capability to perform extremely fast track reconstruction online is becoming more and more important for the LHC upgrade as well as the next generation of HEP experiments, where the expected instantaneous luminosities (in excess of 10ˆ34 /cmˆ2/s) and the very low signal/background ratio ask for fast and clean identification of the main characteristics of interesting events.
The Slim5 R&D project studied different aspects of fast and high-precision tracking in dedicated hardware: data-push silicon sensors, high bandwidth DAQ systems and Associative Memories (AM) for fast track identification. The central element of the development system is a high traffic board, called EDRO, capable of collecting and processing digital data with an input rate of 16 Gbps. The input hits, suitably formatted or clusterized, are sent to an AM board sending back candidate tracks, which are identified at a rate of 40 MHz. The EDRO board is then able to deliver triggers and formatted events for further processing. The EDRO-AM system was first exploited on beam tests where it was able to process events at a maximum rate of 2.5 MHz, trigger events with identified tracks (maximum latency 1 us) and provide a clean sample of events with well reconstructed tracks.
The flexibility of the EDRO-board design allows it to be coupled with completely different hit sources. In the ATLAS project called "FTK Vertical Slice" the EDRO board receives level 1 triggered data from a part of the inner detector and, together with an AM board, identifies tracks for a possible use by the second level trigger processors.
Design criteria of the EDRO board as well as the systems in which it has been or will be used are described together with the performance measured both in lab and real experiments with beam.

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Presenter: Prof. VILLA, Mauro (Universita di Bologna e INFN (IT))

Session Classification: Posters

Contribution ID: **34** Type: **not specified**

A Fast General-Purpose Clustering Algorithm Based on FPGAs for High-Throughput Data Processing

Thursday 3 May 2012 20:00 (1 hour)

We present a fast general-purpose algorithm for high-throughput clustering of data "with a two dimensional organization". The
algorithm is designed to be implemented with FPGAs or custom electronics. The key feature is a processing time that scales
linearly with the amount of data to be processed. This means that clustering can be performed in pipeline with the readout, without
suffering from combinatorial delays due to looping multiple times through all the data. This feature makes this algorithm especially
well suited for problems where the data has high density, e.g. in the case of tracking devices working under high-luminosity
condition such as those of LHC or Super-LHC.
The algorithm is organized in two steps: the first step (core) clusters the data; the second step analyzes each cluster of data to
extract the desired information. The current algorithm is developed as a clustering device for modern high-energy physics pixel
detectors. However, the algorithm has much broader field of applications. In fact, its core does not specifically rely on the kind of
data or detector it is working for, while the second step can and should be tailored for a given application. For example, in case of
spatial measurement with silicon pixel detectors, the second step performs center of charge calculation. Applications can thus be
foreseen to other detectors and other scientific fields ranging from HEP calorimeters to medical imaging.
An additional advantage of this two steps approach is that the typical clustering related calculations (second step) are separated
from the combinatorial complications of clustering. This separation simplifies the design of the second step and it enables it to
perform sophisticated calculations achieving offline-quality in online applications. The algorithm is general purpose in the sense
that only minimal assumptions on the kind of clustering to be performed are made.

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Session Classification: Posters

Contribution ID: **35** Type: **not specified**

Study of system integration for the pixel detector of the PANDA experiment

Thursday 3 May 2012 20:00 (1 hour)

The PANDA experiment will make use of antiproton cooled beams of unprecedented quality, that will become available at the Facility for Antiproton and Ion Research (FAIR) in Darmstadt, featuring up to 2•10ˆ11 antiprotons and momentum between 1.5 –15 GeV/c.
To handle forward particle distribution due to the Lorentz boost, the apparatus is arranged in an asymmetric layout around the interaction point between antiprotons and pellet or gas jet target.
This peculiarity requires a tracking detector with a forward design and in particular an innermost Micro Vertex Detector (MVD) based on silicon devices with an innovative design in an unusual geometry. The material budget of this silicon tracker has to be minimized in view of particle momenta ranging from few hundreds of MeV/c up to several GeV/c. Besides high interaction rate asks for fast data readout being PANDA without low-level trigger selection and particle identification is planned over the full range of energies.
To cope with these requirements MVD includes innermost layers made of thinned epitaxial silicon hybrid pixel detectors and outermost composed of double side silicon micro strips.
In particular the mechanics integration of the pixel detector is a challenge due to the compact volume of the MVD asking for specific solutions as carbon foam both to increase the heat dissipation towards the cooling pipes and acting as mechanics supports.
To cope with high data rate new non-triggered readout chips developed in 130 nm CMOS technology feature high speed readout and charge measurement with Time over Threshold, and to deal with the limited material budget request new aluminium strips are developed for data transmission and specific busses design are under study.
Results concerning the developments of prototypes to solve critical items will be presented.

Summary

The PANDA experiment will make use of antiproton cooled beams of unprecedented quality, that will become available at the Facility for Antiproton and Ion Research (FAIR) in Darmstadt, featuring up to 2•10ˆ11 antiprotons and momentum between 1.5 –15 GeV/c.
To handle forward particle distribution due to the Lorentz boost, the apparatus is arranged in an asymmetric layout around the interaction point between antiprotons and pellet or gas jet target.
This peculiarity requires a tracking detector with a forward design and in particular an innermost Micro Vertex Detector (MVD) based on silicon devices with an innovative design in an unusual geometry. The material budget of this silicon tracker has to be minimized in view of particle momenta ranging from few hundreds of MeV/c up to several GeV/c. Besides high interaction rate asks for fast data readout being PANDA without low-level trigger selection and particle identification is planned over the full range of energies.
To cope with these requirements MVD includes four cylindrical layers in the region around the interaction point, the barrels, and six planar layers in the forward region, the disks, equipped with silicon detectors: hybrid pixel detectors in the innermost layers and double sided micro strip in the outermost layers.
In particular the mechanics integration is a challenge due to the compact volume of the MVD.
First hybrid pixel prototypes based on thinned epitaxial silicon sensors have been developed as a detector technology capable to sustain the expected radiation levels at room temperature.
Besides the handling of high data rate in a triggerless mode suggested a new non-triggered readout ASIC, for the hybrid pixel detector, that has been developed in 130 nm CMOS technology. This one

provides time information via a time stamp synchronous with the 155.5 MHz global clock signal and energy information via the Time over Threshold technique. High speed serial links and early electrical to optical conversion are adopted to reduce the amount of cables and material.
Besides to cope with the limited material budget request new aluminium strips are developed for data transmission and specific busses design are under study.
Thermal power produced by the dedicated electronics, evaluated as
˜ 1 W/cmˆ2 is removed by a water cooling system operating below atmospheric pressure mode.
For the cooling system design a material with low density, high thermal conductivity, low thermal expansion coefficient, easily machined, feasible to glue, stable at different temperatures and radiation resistant has been searched. The material which answer to all these requirements is the carbon foam: his open pore structure graphite combined with a dense graphite matrix produces a material with high thermal properties and low density. The material properties, mechanical and thermal, were studied for radiation hardness.
Besides, this material acts as mechanics support too for the pixel disks.

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Presenter: CALVO, Daniela (INFN-Torino (IT))

Session Classification: Posters

Contribution ID: **36** Type: **not specified**

A 0.18 µm CMOS Low-Power Radiation Sensor for Asynchronous Event-Driven UWB Wireless Transmission

Thursday 3 May 2012 20:00 (1 hour)

We describe the design of a floating gate-based MOS sensor embedded in a read-out CMOS sensing element used as a radiation sensor. The read-out cell asynchronously triggers an all-digital Ultra-Wide Band (UWB) transmitter operating in a 0-5GHz band, with a repetition frequency, which dynamically depends on the radiation level. The trigger signal ranges 20 to 30MHz, with a designed sensor input range, between 0 and 2V.
The floating gate MOS sensor has been recently characterized and here emulated with a commercial radiation-sensitive FETs based on a metal-oxide-silicon p-channel structure, for a 2V variation given an equivalent absorbed dose of 100rad within 1 and 100krad. A maximum sensitivity of 1mV/rad is estimated up to 10krad. The paper shows the design of a preliminary microelectronic circuit that includes a sensor, an oscillator and modulator, which is now under submission. The prototype will be interfaced to an external power supply and to an antenna for pulse transmission, to provide a preliminary proof-of-concept validation before a complete integration. Given the small estimated area of the complete chip prototype, comprising the antenna, i.e. less than 1mm2, the IC can enable a large variety of applications for spot radiation monitoring systems (High-Energy Physics experiments might benefit of this concept). The paper shows measurements on a mini test-board equipped with the full-custom components comprising an external transmitter IC that will be integrated in the ASIC prototype (TowerJazz). First measurements, obtained at the "Istituto Italiano di Tecnologia", Center for Space Human Robotics, demonstrate the feasibility of the proposed event-driven asynchronous Ultra-Low Power (ULP) UWB transmission. The Science and Technology Facility Council of the Rutherford Appleton Laboratory (RAL), UK, supports the entire research.

Authors: Dr GABRIELLI, Alessandro (Universita e INFN (IT)); Dr DEMARCHI, Danilo (IIT, Istituto Italiano di Tecnologia, MiNES Lab, Dept. of Electronics and Telecommunications, Politecnico di Torino, Italy); Dr VILLANI, Enrico Giulio (STFC - Science & Technology Facilities Council (GB)); Dr CREPALDI, Marco (IIT, Istituto Italiano di Tecnologia, Politecnico di Torino, Italy)

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Presenter: Dr GABRIELLI, Alessandro (Universita e INFN (IT))

Session Classification: Posters

Contribution ID: **37** Type: **not specified**

The CBC microstrip readout chip for LHC phase II

Friday 4 May 2012 11:30 (30 minutes)

The CBC is a 130 nm CMOS chip designed for the readout of short silicon microstrips for the CMS Phase II tracker upgrade. It is a 128 channel wire-bonded chip which can be DC coupled to sensors of either polarity. The replacement tracker is also expected to provide limited tracking information to the Level 1 hardware trigger. With a binary front end the chip is well suited to adapting for use in stacked strip sensor modules in order to promptly identify high transverse momentum candidates. In this version, binary data are retained in a 256 deep pipeline and transmitted in an unsparsified format in response to an incoming trigger. The CBC performance has been evaluated in the laboratory and in a test beam. Details of the design and latest results of the measured performance will be presented.

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Presenter: PESARESI, Mark (Imperial College Sci., Tech. & Med. (GB))

Session Classification: On-module electronic circuits (3D and conventional), intra-module and off-detector communication

Contribution ID: **38** Type: **not specified**

TBC: Dynamic Cluster Formation in Pixilated Detectors

Given charge spread in particle detection and charge sharing between multiple detecting elements, clusters of hit pixels are inevitable in pixilated detectors, and the problem is, of course, worse for smaller pixel sizes. At the same time, in order to optimize the detective quantum efficiency (DQE) and the throughput, it is important to produce one and only one "winning"pixel address per hit and to
produce this winner in the front-end circuitry rather than downstream in the data acquisition firmware. Therefore, the problems of cluster finding and resolution in front-end electronics are becoming more
and more important.
In some cases, clusters are hard-wired as arrays of detector elements. If a particle deposits its charge entirely within a particular array of detector elements, then its location will be properly determined, but if the charge is distributed between two or more hard-wired arrays, then more than
one hit location will be registered and the data acquisition system will be forced to resolve the problem
in firmware or software. In other cases, the cluster finding algorithms assume a fixed size and shape,
but they are not hard-wired to a particular location. Each pixel can view itself as being at the center of
its own array. Again, if charge spread or particle angle or energy pushes the charge cloud beyond the
assumed array borders, then the hit location cannot be properly resolved within the front-end chip itself. Dynamic cluster formation is a means by which any cluster, regardless of size or shape, can be
formed. This will allow the constituents of the dynamic cluster to arbitrate with one another to determine which pixel or pixels are the centers of the particle hit or hits. The challenge is to perform
dynamic cluster formation with a minimum of circuit complexity so that it can be employed in smaller
pixel sizes.
Complicating the problem of dynamic cluster formation is the problem of time walk. Charge distribution from particle detection is not uniform among the pixels. Therefore, the propagation delay
through the different front ends affected by the passage of a particle will not be uniform. The timeover-
threshold will not be uniform either. Therefore, some method is necessary not only to determine which detector elements are members of a dynamic cluster, but also when the arbitration among them
has concluded.
A novel method of dynamic cluster formation is proposed. It is a two step process. The first step is to form the cluster on the fly by determining its edges with a self-triggered process. On the inside of a cluster, charge deposition has exceeded a user-defined threshold; on the outside of the cluster this has not happened. Linkage is accomplished by tying the members of the cluster to a

common timing signal that maintains arbitration until all cluster members agree that arbitration is over.
The second step is the arbitration itself and, theoretically speaking, any arbitration method implementable in silicon is usable.
The prototype arbitration algorithm is called C8 or "Compare 8"and it has been implemented in a readout chip for x-rays. The actual method used to convert the C8 algorithm into a Dynamic Cluster C8
algorithm is presented here. The explanation will be general, but the emphasis will be on its implementation targeting 3D chip integration technology.

Authors: DEPTUCH, Grzegorz (FERMILAB); HOFF, Jim (Fermilab)

Presenter: HOFF, Jim (Fermilab)

Track Classification: On-module electronic circuits (3D and conventional), intra-module and off-detector communication

Contribution ID: **39** Type: **not specified**

Development of high performance tracking layers as a sandwich of optimised CMOS pixel sensors

Thursday 3 May 2012 20:00 (1 hour)

We propose to enhance the performances of tracking layers by building a sandwich of low power time-integrating CMOS pixel sensors. Sensors equipping one side of the layer offer a high spatial resolution (few μm), while the sensors on the other side focus on the time resolution (few μs). The whole device targets a material budget lower than 0.5 % of X0.
We will present the in-beam test results of a double-sided ladder featuring 8 millions of pixels (18.4 × 18.4 μm2) read-out in 110 μs and an equivalent thickness of 0.6 % of X0, build by the PLUME collaboration. Plans to reach 0.3 % of X0 will also be discussed.
We will then review the development of CMOS pixel sensors with various optimisations with respect to the spatial or time resolution. Especially the road to reach a few microseconds read-out time, while maintaining the power budget at the few μW per pixel level will be described.
The conclusion will show possible implementation of these double-sided tracking layers.

Summary

See attached file.

Author: BAUDOT, Jerome (Institut Pluridisciplinaire Hubert Curien (FR))

Co-authors: Dr NOMEROTSKI, Andrey (University of Oxford (GB)); BESSON, Auguste Guillaume (Institut Pluridisciplinaire Hubert Curien (FR)); Dr GREGOR, Ingrid (Deutsches Elektronen-Synchrotron (DE)); Dr GOLDSTEIN, Joel (University of Bristol (GB)); WINTER, Marc (Institut Pluridisciplinaire Hubert Curien (FR)); GAULD, Rhorry (University of Oxford); Dr SENYUKOV, Serhiy (Institut Pluridisciplinaire Hubert Curien (FR))

Presenter: BAUDOT, Jerome (Institut Pluridisciplinaire Hubert Curien (FR))

Session Classification: Posters

Contribution ID: **40** Type: **not specified**

From hybrids pixels to smart vertex detectors using 3D technologies

Friday 4 May 2012 08:30 (30 minutes)

Even if 3D electronics suffers difficult beginnings, industrial trends are now strongly pushing that way to a production phase. Keeping in mind the usual arguments of power consumption, speed, technology mixing, new and less expected possibilities are now appearing.
In trackers world, few attempts have been made to introduce 3D not only as an alternative to shrinking technologies but also as a source of new possibilities.
Post-processed TSV have yet proven to be feasible in HEP circuits allowing for new routing schemes of circuits IO without modifying the original process. On the other hand, 3D structures as part as the chip process offers more possibilities but the price to pay is the poor commercial offers.
With new ideas for building depleted sensors with standard MOS process, 3D tech could allow a fully integrated fabrication of future vertex chips (sensor + read-out) in the same production chain.
This talk will try to give an idea of the efforts made and of the results obtained using these 3D techniques in the scope of HL LHC R&D programs (ATLAS)

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Presenter: CLEMENS, JCC (Universite d'Aix - Marseille II (FR))

Session Classification: Development of critical technologies and system integration

Contribution ID: **41** Type: **not specified**

A hybrid module architecture for a prompt momentum discriminating tracker at HL-LHC

Thursday 3 May 2012 15:00 (30 minutes)

The capability of performing quick recognition of particles with high transverse momentum (more than a few GeV/c) in the inner tracker is deemed essential to keep the CMS trigger rate at an acceptable level at a higher luminosity LHC (L > 10ˆ34 cm-2 s-1). We present an architecture for a novel tracking module based on a combination of a pixelated sensor with a short strip sensor that would offer such capability. The critical aspects of the design such as the projected power consumption, the resulting material budget, and the data flow model are discussed and estimates are given. It is also shown that a manufacturable module of this type is well within the capabilities of currently available microelectronic and packaging-assembly technologies.

Author: MARCHIORO, Alessandro (CERN)

Co-author: ABBANEO, Duccio (CERN)

Presenter: ABBANEO, Duccio (CERN)

Session Classification: Application of intelligent detectors / Coupled sensors and monolithic architectures

Track Classification: Coupled sensors and monolithic architectures

Contribution ID: **42** Type: **not specified**

Use of Associative Memories for L1 triggering in LHC environment.

Saturday 5 May 2012 09:30 (30 minutes)

Modern high energy physics experiments search for extremely rare processes hidden in much larger background levels. As the experiment complexity, the accelerator backgrounds and luminosity increase we need increasingly exclusive selections to efficiently select the rare events inside the huge background.
In the framework of the CMS experiment at LHC one of the identified challenges for future upgrade is the capability of using the tracker information to trigger events already at L1 (now they are used at L2).
This strategy requires massive computing power to minimize the online execution time of complex tracking algorithms and the "combinatorial challenge".
Associative Memories (AM) have been already used in other experiments (CDF) as a way to compare the tracker informations of each event to pre-calculated "expectations"(pattern matching) in a very short time and contribute to the trigger decision. To use the AM approach for the CMS tracker one of the main challenges is to make available the tracker data to the AM processor in a very short time (6 ⊠s is the L1 latency for CMS).

We describe a possible application of AM in the CMS environment using the existing hardware developed for other experiments, the AMBslim mother board consisting of 4 smaller boards, the Local Associative Memory Banks (LAMB), each hosting 32 AM chips to contain the stored patterns with the readout logic. The ability of a single AMBSlim to process a single event is much less than the amount of input data foreseen for the CMS case, and the latency strongly depends on the time necessary to load the data in the AM system and to process a single event.
One possible solution is to parallelize the event processing inside the AMBslim board assigning each event to one LAMB. We describe the firmware implementation of this concept in the current hardware and the results obtained.

Finally we discuss a possible modification of the LAMB hardware in order to obtain the minimum delay time for processing events.

Authors: MAGALOTTI, Daniel (INFN Sezione Perugia (IT)); SERVOLI, Leonello (INFN Sezione Perugia (IT)); BIASINI, Maurizio (Universita degli Studi Peugia e INFN Sezione Perugia(IT)); NAPPI, Nello (Universita degli Studi di Perugia); GUNNELLINI, Paolo (Universita degli Studi Perugia(IT)); TARONI, Silvia (Universita degli Studi Perugia e INFN Sezione Perugia(IT))

Presenter: MAGALOTTI, Daniel (INFN Sezione Perugia (IT))

Session Classification: Real time pattern-recognition and advanced algorithms

Track Classification: Real time pattern-recognition and advanced algorithms

Contribution ID: **43** Type: **not specified**

Hybrid circuits and substrate technologies for the CMS Tracker upgrade

Friday 4 May 2012 10:00 (30 minutes)

The upgrade of the CMS tracker at the HL-LHC will require the design of new front-end modules. These tracker modules will embed new front-end flip-chip ASICs that will be bump bonded to high density substrates, and those will be directly wire bonded to the tracker sensors. The resulting hybrid circuits will concentrate the module data flow and feed an optical transmitter module (GBT) that will be located on an adjacent service board. To achieve this degree of integration, the hybrid circuits have to be designed in large formats using high density substrate technologies that are commonly used for integrated circuits packaging. The different technologies that have been identified will be presented with their respective merits and constraints. Different circuits arrangements will be proposed for the assembly of the module electronics, aiming for a cost effective and reliable manufacturability of the CMS tracker modules.

Author: BLANCHOT, Georges (CERN)

Co-authors: MARCHIORO, Alessandro (CERN); ABBANEO, Duccio (CERN); VASEY, Francois (CERN)

Presenter: BLANCHOT, Georges (CERN)

Session Classification: Development of critical technologies and system integration

Track Classification: Development of critical technologies and system integration

Contribution ID: **45** Type: **not specified**

Radiation tolerant IP-cores for the control and readout of Front-End electronics in future Silicon detectors

Thursday 3 May 2012 20:00 (1 hour)

The FF-LYNX protocol represents an innovative and flexible solution for the distribution of Timing, Trigger and Control (TTC) signals and the data readout in future detectors for the High Energy Physics. Transmitter (TX) and Receiver (RX) interfaces to serial electrical links implementing the FF-LYNX protocol with different speed options (160Mbps, 320Mbps, 640Mbps) have been developed. They are available as VHDL cores for integration in commercial FPGA devices and as Standard-Cell based cores, designed and developed in the IBM CMOS 130nm technology. Architecture and behavior of the interfaces and results of test and characterization of the prototypes embedded in the test ASICs fabricated in 2011 will be presented.

Radiation tolerant FIFOs have been developed as input and output buffers in TX and RX interfaces. They are available as stand-alone IP-cores and can be used in Front-End ASICs or other circuits where radiation tolerant data buffers are required. Architecture and behavior of these FIFO blocks will be described as well as results of irradiation tests performed on the their prototypes.

Results of tests performed with FF-LYNX Encoder and Decoder directly coupled with the GBT Transmitter and Receiver in an FPGA proof-of-concept demonstrator of optical links handled by GBT transceivers and running data encoded with the FF-LYNX protocol will be presented as well as the architecture and the behavior of the Data Concentrator Module, a VHDL core that merges input data transmitted from multiple sources through “low-speed”serial links into one (or more) “high-speed”output serial links.

Finally future plans, mainly focused on the development of interfaces with improved speed and power performances and including custom Serializer and Deserializer modules will be presented.

Summary

The FF-LYNX protocol developed by INFN-Pisa, University of Pisa, Department of Information Technology, and UCSB, Physics Department, represents an innovative and flexible solution for the distribution of Timing, Trigger and Control (TTC) signals and the data readout in future detectors for the High Energy Physics. It provides different speed options (“4x”, “8x”, “16x”) and robustness of critical information (triggers, frame headers and frame descriptors) against errors due to noise and radiation, It allows to share the same physical channel between time critical and fixed latency information, as triggers or “trigger’data, and information with lower priority and unbounded latency, as “raw”data or “slow”controls.

The protocol has been extensively validated through functional simulations and tests in FPGA based emulators. Transmitter (TX) and Receiver (RX) interfaces to “double-wire”(clock and data on separate lines) serial electrical links have been developed in the three speed options as VHDL cores, available for integration in commercial FPGA devices, and as Standard-Cell based cores, designed in the IBM CMOS 130nm technology. A test circuit with prototypes of the interfaces has been fabricated in 2011.

A full set of TX and RX interfaces implementing a new version of the FF-LYNX protocol with a DC-balanced “8b/10b like”channel encoding that provides compatibility with optical links and standard Clock Recovery Devices (CRD) and, therefore, with “single-wire”links (clock and data

encoded onto one line) has been also developed. Prototypes of the interfaces in the "8x"speed option have been designed as Standard-Cell based cores and integrated in a second test circuit.

The behavior and the performance of the TX and RX interfaces in both versions will be shortly described and the results of the test and the characterization (also under irradiation) of their prototypes embedded in the test ASICs will be presented.

FIFOs implementing error detection and correction and scrubbing have been developed as input and output buffers in TX and RX interfaces. These modules can be used as stand-alone IP-cores in Front-End ASICs or other circuits where radiation tolerant data buffers are required. The architecture and the behavior of these FIFO blocks will be shortly described as well as results of irradiation tests performed on the FIFO prototypes.

FF-LYNX Encoder and Decoder have been directly coupled with the GBT Transmitter and Receiver in an FPGA (Xilinx Virtex 6) and a proof-of-concept demonstrator of optical links handled by GBT transceivers and running data encoded with the FF-LYNX protocol has been developed and validated. Results of the tests performed in the demonstrator will be presented.

We have also very recently developed and validated the Data Concentrator Module (DCM), a digital module that merges input data transmitted from multiple sources through "low-speed"serial links into one (or more) "high-speed"output serial links. This IP-core could play a key role in concentrating and buffering data from different Front-End ASIC in future detector modules before transmission to optical transceivers. Both DCM architecture and behavior will be described.

Future plans will be finally shortly described. They mainly foresee the development as IP-cores of TX and RX interfaces compatible with "single-wire"serial links with improved speed (up to 800 Mbps) and power performance and tolerance to Single Event Transient effects. This will require the development of custom Serializer and Deserializer devices and of a radiation tolerant CRD. The submission of a test circuit including prototypes of these devices is foreseen before the end of 2012.

Author: MAGAZZU, Guido (Univ. of California Santa Barbara (US))

Presenter: MAGAZZU, Guido (Univ. of California Santa Barbara (US))

Session Classification: Posters

Contribution ID: **46** Type: **not specified**

A Self Seeded First Level Track Trigger for ATLAS

Saturday 5 May 2012 09:00 (30 minutes)

For the planned high luminosity upgrade of the Large Hadron Collider, aiming to increase the instantaneous luminosity to 5-7 x 10ˆ34/cmˆ2/s, the implementation of a first level track trigger has been proposed, which could be installed in the year 2020/21 along with the complete renewal of the ATLAS Inner Detector.
The fast readout of the hit information from the Inner Detector is considered as main challenge of such a track trigger. Different concepts for the implementation of a first level trigger are currently studied within the ATLAS collaboration.
The so called “Self Seeded” track trigger concept exploits fast front-end filtering algorithms based on cluster size reconstruction and fast vector tracking to select hits associated to high momentum tracks. Simulation studies have been performed and results on efficiencies and expected bandwidth reductions are presented for different layouts.

Possible hardware implementations of the first level track processor able to reconstruct all high momentum tracks in every collision within a latency of 1 mus will be discussed.

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Co-authors: JOHN, Arno (Ruprecht-Karls-Universitaet Heidelberg (DE)); SCHMITT, Sebastian (Ruprecht-Karls-Universitaet Heidelberg (DE))

Presenters: SCHOENING, Andre (Ruprecht-Karls-Universitaet Heidelberg (DE)); SCHMITT, Sebastian (Ruprecht-Karls-Universitaet Heidelberg (DE))

Session Classification: Real time pattern-recognition and advanced algorithms

Track Classification: Real time pattern-recognition and advanced algorithms

Contribution ID: **47** Type: **not specified**

Status of Work on Vertically Integrated Circuits

Thursday 3 May 2012 20:00 (1 hour)

Commencing work on the 3D-integrated circuits in the High Energy Physics (HEP) community, which coincided with the appearance at the same time of first commercial 3D-IC design kits, whetted the appetite of the community and raised confidence in the rapid rollout of 3D-IC technology, which undoubtedly introduces a new quality to integrated readout system for the detectors. The Fermilab team was in this group of a few, who spearheaded the development of 3D integrated circuits for detector's readout. At the first place a proprietary fully-depleted CMOS SOI process by MIT-LL and the via-last based wafer bonding technology was used. Commercial bulk CMOS wafers with front-end-of-line integrated micrometers-size through silicon vias (TSVs) and the Tezzaron wafer bonding technology was used at the later time. The early Fermilab work led to the formation of an international consortium, grouping major research centers, for the development of vertically integrated circuits. The consortium submitted the first multi project wafer (MPW) run to Tezzaron with over 25 different designs in 2009. The run unfortunately has been suffering from multiple problems causing an overall delay to such an extent that no diced 3D parts could be delivered to the participants until the drafting of this abstract. Despite of this downbeat of the apparent picture of the state of the first HEP MPW run, it is received as the source of learning experiences, about 3D-IC processing technology and its crucial ingredients, like requirements for the surface flatness and surface treatment, alignment, gas atmosphere, etc. Due to the use up of initial stocks of wafers for failed attempts of bonding, it was necessary to start an additional lot of wafers at the foundry. By having the conditions of the bonding process fine-tuned, it is expected that the wafers will eventually be bonded successfully, resulting in distribution of chips for testing. The review of consecutive steps undertaken with Tezzaron, illustrated by their results, will be provided at the presentation. In the autumn of last year, a group of professional brokers (MOSIS/CMP/CMC) decided to open an access to the Tezzaron/GlobalFoundries 3D-IC process through the MOSIS MPW scheme. The decision drew deeply from the knowledge acquired in the completion of the 3D-IC MPW run by Fermilab and nonetheless existing positive experience of full processing of another MPW run (parallel to the HEP one) by Tezzaron. New high density circuit bonding techniques, wafer thinning, and submicrometer size TSVs allowing connection to top and bottom sides of an IC provide new opportunities for the detector designer. These opportunities will be presented by looking at various 3D designs that have been completed for the MPW run or are being planned for exploration.

Author: DEPTUCH, Grzegorz (FERMILAB)

Co-authors: Mrs SHENAI, Alpana (Fermilab); KHALID, Farah (F); HOFF, Jim (Fermilab); TRIMPL, Marcel (Fermilab); Mr YAREMA, Ray (FNAL); Dr LIPTON, Ronald (Fermi National Accelerator Lab. (US)); Mr ZIMMERMAN, Tom (Fermilab)

Presenter: DEPTUCH, Grzegorz (FERMILAB)

Session Classification: Posters

Contribution ID: **48** Type: **not specified**

Asynchronous readout architectures for Tracker Front-End ASICs

Friday 4 May 2012 12:00 (30 minutes)

We preset a design of a front end ASIC that combines a level 1 trigger and normal event readout. It uses asynchronous logic through out the design to reduce both power consumption and noise sensitivity. The only clock used is the 40 MHz LHC clock. A test chip based on this design is planned to be submitted in July of this year.

Summary

The use of architectures based on asynchronous logic represents an innovative approach in the readout of Front-End circuits for Silicon Trackers. These architectures have several key advantages with respect to traditional synchronous architectures. First, when there is no data most of the circuitry remains inactive with a significant saving in power. Second, there is no need for a high frequency clock which reduces potential noise sources. Finally, the digital circuits operate over a much wider frequency range than clocked ones and therefore the power spectrum will not be concentrated in a restricted set of frequency values. This will reduce noise and make shielding easier.

An architecture based on asynchronous "mousetrap"pipelines has been developed for a possible upgrade of the CMS Silicon Tracker. This design supports a level 1 trigger as well as conventional silicon readout. We describe in detail the behavior and the timing performance of this readout architecture as well as the methods used to minimize the effect of noise and single event upsets

This architecture has been mapped into a Standard Cell library for the IBM CMOS 130nm technology. A custom approach in the placement and routing of the Standard Cells has been chosen in order to optimize and equalize delays along the asynchronous pipelines. A test ASIC is currently under development and it will be submitted for fabrication this summer. The only clock on-chip is the 40 MHz clock used to synchronize data acquisition with the LHC bunch crossings rate. All data transmission within and between ASICs is via asynchronous logic. Data is converted to synchronous logic at the connection to the optical transceivers (GBT). The test ASIC and a possible module architecture based on it will be described in detail.

Author: Dr JOHNSON, Marvin (Fermilab)

Co-author: Mr MAGAZZU, Guido (UCSB)

Presenters: Dr JOHNSON, Marvin (Fermilab); JOHNSON, Marvin (Fermi National Accelerator Lab. (US))

Session Classification: On-module electronic circuits (3D and conventional), intra-module and off-detector communication

Track Classification: On-module electronic circuits (3D and conventional), intra-module and off-detector communication

Contribution ID: **49** Type: **not specified**

A Level-1 Tracking Trigger for the CMS Upgrade using stacked silicon strip detectors and advanced pattern recognition technologies

Thursday 3 May 2012 10:00 (30 minutes)

Experience at high luminosity hadrons collider experiments shows that tracking information enhances the trigger rejection capabilities while retaining high efficiency for interesting physics events. The design of a tracking based trigger for the High Luminosity LHC (HL-LHC) is an extremely challenging task, and requires the identification of high-momentum particle tracks as a part of the Level 1 Trigger. Simulation studies show that this can be achieved by correlating hits on two closely spaced silicon strip sensors, and reconstructing tracks at L1 by employing an Associative Memory approach. The progresses on the design and development of this micro-strip stacked prototype modules and the performance of few prototype detectors will be presented. Preliminary results of a simulated tracker layout equipped with stacked modules are discussed in terms of pT resolution and triggering capabilities. Finally, a discussion on the L1 architecture will be given.

Author: BOUDOUL, Gaelle (Universite Claude Bernard-Lyon I (FR))

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Presenter: BOUDOUL, Gaelle (Universite Claude Bernard-Lyon I (FR))

Session Classification: Application of intelligent detectors / Coupled sensors and monolithic architectures

Track Classification: Applications of intelligent detectors

Contribution ID: **50** Type: **not specified**

Progress on silicon and carbon foam composite wafers for interposer or hybrid use

Thursday 3 May 2012 20:00 (1 hour)

We present updated results of prototyping silicon and carbon foam composite wafers for use as either low mass interposers or active hybrids. Composite 4 inch wafers have been prototyped with approximately 4 mm thickness and average density 20% that of silicon. A composite wafer consists of top and bottom silicon face-plates on a carbon foam core, assembled with adhesive that can withstand 300 C process temperature. Embedded in the foam core are vertical silicon "fins"that can have passive vertical metal traces for interposer applications or active IC's for hybrid applications. Metal contacts on the vertical fins are exposed by grinding the face-plates. Lithographic processing of the composite wafer can then be applied to interconnect the exposed contacts. This final step has not yet been prototyped.

Summary

this is follow-on work to concepts and initial prototypes shown at WIT2010. IF there will be a poster session this could be a poster rather than an oral presentation.

Author: GARCIA-SCIVERES, Mauricio (Lawrence Berkeley National Lab. (US))

Presenter: GARCIA-SCIVERES, Mauricio (Lawrence Berkeley National Lab. (US))

Session Classification: Posters

Contribution ID: **51** Type: **not specified**

A Level-1 Tracking Trigger for the CMS Upgrade using stacked silicon strip detectors and advanced pattern recognition technologies

Experience at high luminosity hadrons collider experiments shows that tracking information enhances the trigger rejection capabilities while retaining high efficiency for interesting physics events. The design of a tracking based trigger for the High Luminosity LHC (HL-LHC) is an extremely challenging task, and requires the identification of high-momentum particle tracks as a part of the Level 1 Trigger. Simulation studies show that this can be achieved by correlating hits on two closely spaced silicon strip sensors, and reconstructing tracks at L1 by employing an Associative Memory approach. The progresses on the design and development of this micro-strip stacked prototype modules and the performance of few prototype detectors will be presented. Preliminary results of a simulated tracker layout equipped with stacked modules are discussed in terms of pT resolution and triggering capabilities. Finally, a discussion on the L1 architecture will be given.

Author: BOUDOUL, Gaelle (Universite Claude Bernard-Lyon I (FR))

Presenter: BOUDOUL, Gaelle (Universite Claude Bernard-Lyon I (FR))

Contribution ID: **54** Type: **not specified**

Trigger and Data Acquisition Strategy for the LHCb Upgrade

Thursday 3 May 2012 10:30 (30 minutes)

The LHCb experiment is making strong strides towards the exploitation of physics opportunities that may lead to the discovery and elucidation of physics beyond the Standard Model. While LHCb will be able to measure many interesting channels in the upcoming few years, an upgrade aimed at increasing its sensitivity by about a factor of 10 will broaden the discovery potential of the experiment. Two key elements of the upgrade are the ability of reading out the detector at 40 MHz and a flexible and efficient software trigger, that exploits the unique features of the signal events sought. The key elements of the data acquisition and trigger strategies will be discussed, with particular emphasis on how the tracking information is incorporated to provide an effective selection of interesting beauty and charm events.

Summary

Trigger and Data acquisition strategy for the LHCb Upgrade, with particular emphasis on how the strategy ensures fast tracking to be incorporated in a very fast and efficient software trigger.

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Session Classification: Application of intelligent detectors / Coupled sensors and monolithic architectures

Track Classification: Applications of intelligent detectors

Contribution ID: **56** Type: **not specified**

FPGA and ASIC based algorithms for the present and upgraded LHCb silicon vertex detector

Thursday 3 May 2012 12:30 (30 minutes)

The LHCb experiment is dedicated to the search for new physics signatures in beauty and charm decays. The selection of interesting signal events requires accurate measurements of decay lifetimes and reconstruction of complex vertex topologies. The VErtex LOcator (VELO) has been designed to fulfill these functions, by providing tracking information close to the proton-proton collision region.

At present analogue information from its readout electronic is digitized, corrected for various sources of coherent noise, and further processed through a series of algorithms implemented on FPGAs residing on the ìoff detectorî readout boards. The tuning of the parameters of these algorithms is performed using a bit-perfect emulation of these algorithms integrated in to the full off-line software of the experiment. These algorithms are described, and their performance and tuning in the course of the 2011 data taking cycle are summarized.

For the LHCb upgrade in addition to the evolution to the present strip design a pixel option is also being developed. In both cases the zero-suppression functionality will be preformed by the read out front-end chip. For this a new ASIC is being designed - the chip will be a derivative of the TimePix/MediPix family. The chip will incorporate a local intelligence in the pixel for time over threshold measurement, time stamping and spare read out. In order to cope with the data rates and use the pixel area most effectively an on-chip data compression scheme will be implemented. This contribution will give an overview of the chip digital architecture, and describe the off-detector signal processing, including the time ordering and clustering.

Summary

Signal processing for the LHCb VELO detector and LHCb upgrade

Authors: ARTUSO, Marina (Syracuse University (US)); Dr SZUMLAK, Tomasz (Glasgow University)

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Session Classification: Application of intelligent detectors / Coupled sensors and monolithic architectures

Track Classification: Applications of intelligent detectors

Contribution ID: **57** Type: **not specified**

Pattern recognition with vector-type detector hits

Saturday 5 May 2012 11:30 (30 minutes)

Novel types of "intelligent" trackers provide hits consisting of position-cum-direction rather than position alone.
We study several types of track finding algorithms in this context, for example the Hough transform, neural networks, a cellular automaton, track following, and the combinatorial Kalman filter. The performance of the algorithms is compared on simulated data in a simplified detector model, for various assumptions about the occupancy. We also voice some conjectures on which algorithms might be promising candidates for online deployment.

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Presenter: Dr FRÜHWIRTH, Rudolf (ÖAW, HEPHY Vienna)

Session Classification: Real time pattern-recognition and advanced algorithms

Contribution ID: **58** Type: **not specified**

Micro-channel cooling for pixel detectors

Thursday 3 May 2012 20:00 (1 hour)

In HEP experiments the use of pixel detectors requires that high power density in the sensitive area (up to 2 W/cm2) should be carried away by efficient thermal systems, eventually integrated in the light mechanical support structures.
The micro-channel cooling technology is featured by a highly efficient thermal exchange and it can profit by the miniaturization technique applied on composite materials. Thus a viable solution based on microchannel can be provide both for the thermal and mechanical structure of a silicon module.
We present the latest progress on the development of mechanical supports with microchannel cooling for pixel detector systems, designed in particular to match the specifications of the most internal layer of the Silicon Vertex Tracker of the Super-B experiment.
The low-material budget prototypes have thickness of 0.11 % X0 and the results of the characterization tests performed at the thermal-fluid-dynamic facility of the INFN Pisa are reported.

Author: BOSI, Filippo (INFN Pisa)

Presenter: BOSI, Filippo (INFN Pisa)

Session Classification: Posters

Contribution ID: **59** Type: **not specified**

Radiation-Hard and High-Speed Parallel Optical Engine

Friday 4 May 2012 17:00 (30 minutes)

Parallel optical engine allows a compact design for high-speed data transmission. The design is enabled by the readily available high-speed VCSEL arrays. With the use of a 12-channel array operating at 10 Gb/s per channel, a parallel optical engine can deliver an aggregated bandwidth of 120 Gb/s. With the spacing of 250 mm between two VCSELs, the width of a VCSEL array is only 3 mm. This allows the fabrication of rather compact parallel optical engine for installation at a location where space is at a premium. We have designed an ASIC for use in a parallel optical engine for a new layer of the ATLAS pixel detector for the initial phase of the LHC luminosity upgrade. The ASIC is a 12-channel driver of a VCSEL array for operation up to 5 Gb/s. The ASIC is designed using a 130 nm CMOS process to enhance the radiation-hardness. A redundancy scheme has also been implemented to allow the bypass of a broken VCSEL. We have received the ASIC and the performance up to 5 Gb/s is satisfactory. We are able to program the ASIC to bypass a broken VCSEL. The power-on reset circuit is also successfully implemented which sets the ASIC to a default configuration with no signal steering. In addition, we are able to set the drive current in individual channels. We plan to port the design to the 130 nm SiGe BiCMOS process in order to operate at 10 Gb/s for an aggregated bandwidth of 120 Gb/s and some preliminary results of the design will be presented.

Author: Prof. GAN, KK (Ohio State University)

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Session Classification: On-module electronic circuits (3D and conventional), intra-module and off-detector communication

Track Classification: On-module electronic circuits (3D and conventional), intra-module and off-detector communication

Contribution ID: **60** Type: **not specified**

An innovative detection module concept for PET

Thursday 3 May 2012 15:30 (30 minutes)

The design of a positron emission tomography (PET)detection module capable of working inside a magnetic resonant imaging (MRI) system is the main objective of the INFN 4D-MPET project. Simultaneous PET/MRI technology offers better soft tissue contrast and lower radiation doses by providing both functional and morphological information at the same time. The detector will be based on Silicon Photomultipliers (SiPM), which are magnetic field compatible, coupled to a single LYSO scintillator crystal in order to determine the x and y coordinates on the detector with high precision. An improved performance will be accomplished by measuring the Depth of Interaction (DOI) and evaluating the Time of Flight (TOF): the former information is used for decreasing the uncertainty of the z coordinate while the latter reduces the image background noise.
The SiPM detectors will be laid out on both the top and bottom large scintillator faces with respect to the incoming radiation. The two faces will feature identical and independent readout electronics for time and energy measurement. Each readout system will include four identical front-end (FE) mixed-mode ASIC's connected to the SiPM matrices, a cluster processor (CP) ASIC for data reduction and a laser driver/photodiode receiver/clock reconstruction (LD) ASIC for communication with the external data acquisition system through fibre-optics. All ASIC's will be mounted and wire-bonded without package and communicate each other through low voltage differential signalling (LVDS) pads for MRI interference reduction.
The front-end ASIC's will have multiple-channels each of them reading one SiPM output. Every channel will be made up of a preamplifier, a shaper, two discriminators for self-triggering and a time to digital converter (TDC) with a time over threshold (TOT) feature for energy evaluation. The first discriminator will have a fast response so as to trigger efficiently on single photo-electrons; it will provide the starting time information to the TDC/TOT block so as to measure a time which is very close to the interaction time in the scintillator. The second discriminator will provide event validation and TOT start/stop signals with a threshold which must be programmable between 3 and 10 photo-electrons. Such a double threshold technique is necessary to get a high resolution (σLSB =100ps) if the SiPM intrinsic background rate of around 2MHz/mm2 is considered. If the event is valid then the conversion can be completed and the event is transmitted to the cluster processor. If, on the other hand, the high threshold is not reached within a given time window then the TDC must reset itself and wait for the next low threshold event. Moreover, simulations have shown that a better time resolution can be accomplished if the timing information from both crystal faces is used. Shaping is necessary to avoid challenging constraints on the stability and uniformity of the signal shape which must be used for the TOT measurement. Moreover, the tail-linearising filter implies a lower precision requirement on the trailing edge thus reducing the readout complexity.
The cluster processor task will consist in reducing the amount of data to be sent to the external acquisition system based on a clustering technique. Three different clustering levels with increasing complexity are under investigation: the first is the time-stamp clustering, where the cluster comprises all the channels with the same time-stamp. If the cluster energy is higher than a given threshold, all its data is transmitted. The second clustering level is based on both time-stamp and spatial distribution: in this case only one time value per cluster is transmitted; time-stamp and spatial clustering with centroid is the third clustering option where the data transmission is reduced to the cluster position coordinates (x, y, time and amplitude). Moreover, clustering will be used in the evaluation of the DOI by considering the asymmetry in the cluster size on the two crystal

faces.
Finally, the LD ASIC will be used in order to minimize the number of communication devices to one optical input plus one optical output.
An active temperature control is required for the system so as to reduce the SiPM dark count and keep its heat dissipation as low as possible in order to avoid degradations in the electronics performance.
Furthermore, two modes of operation will be implemented both for pre-clinical and clinical applications.

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Presenters: MARINO, Nahema; MARINO, Nahema; Dr MARINO, nahema (university and INFN pisa)

Session Classification: Application of intelligent detectors / Coupled sensors and monolithic architectures

Contribution ID: **61** Type: **not specified**

Introduction and logistic

Thursday 3 May 2012 09:00 (30 minutes)

Presenter: PALLA, Fabrizio (Sezione di Pisa (IT))

Contribution ID: **62** Type: **not specified**

Discussion

Friday 4 May 2012 10:30 (30 minutes)

Session Classification: Development of critical technologies and system integration

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Contribution ID: **63** Type: **not specified**

Discussion

Friday 4 May 2012 17:30 (1 hour)

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Discussion

Saturday 5 May 2012 12:00 (1 hour)

Session Classification: Real time pattern-recognition and advanced algorithms

Contribution ID: **65** Type: **not specified**

Discussion

Thursday 3 May 2012 16:30 (1 hour)

Session Classification: Application of intelligent detectors / Coupled sensors and monolithic architectures

Contribution ID: **66** Type: **not specified**

A Level-1 Track Trigger for CMS with double stack detectors and long barrel approach

Thursday 3 May 2012 14:30 (30 minutes)

The upgrade of the LHC machine is planned to deliver luminosities 5 to 10 times larger than the design one of 1e34 cm-2s-1. A novel tracking system for the CMS experiment must be designed and built. One main aspect of the current activities consists in understanding the capabilities that different designs such a tracker would have to provide for the Level 1 hardware trigger to complement the muon and calorimeter information. Data rate reduction at hardware level consists in both reducing multiple hits from a single track and rejection of low Pt tracks. Pattern-based hit correlation of properly built clusters of hits would provide quality Level 1 primitives to the hardware trigger. These can be combined together in a projective geometry to perform a rough tracking to be implemented online, returning rough Pt, direction and vertex information for a candidate track. The benchmark results from simulations within the official CMS framework are presented for one particular layout based on barrel trigger layers, emphasizing the flexibility of this tool for the design and test of different tracking strategies at level 1 to be compared with the developments in trigger architectures implementation.

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Session Classification: Application of intelligent detectors / Coupled sensors and monolithic architectures