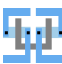
Active Pixel Sensors in high-voltage CMOS technologies for ATLAS

Ivan Perić
University of Heidelberg, Germany

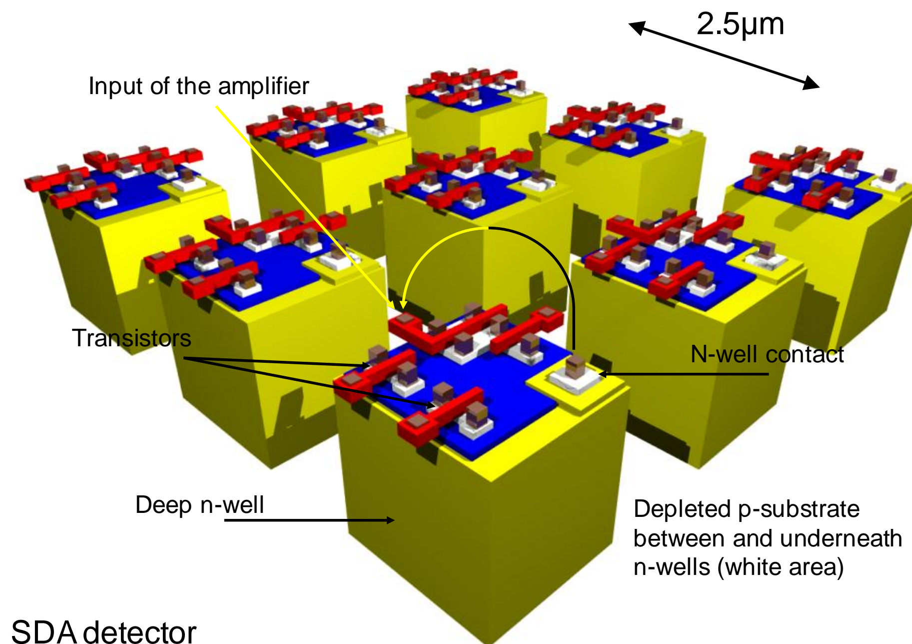
Introduction:
High-Voltage CMOS Pixel Detectors

HV CMOS detectors



- High-voltage particle detectors in standard CMOS technologies (or "smart diode arrays" - SDAs) are a new detector family that allows implementation of low-cost radiation-tolerant detectors with good time resolution.
- The deep n-well in a p-substrate is used as the charge-collecting electrode
- The entire CMOS pixel electronics are placed inside the deep n-well. PMOS transistors are placed directly inside the deep n-well, NMOS transistors are situated in their p-wells that are embedded in the deep n-well as well.
- A typical reverse bias voltage is 60 V and the depleted region depth ~15 µm. Signal charge collection occurs mainly by drift.

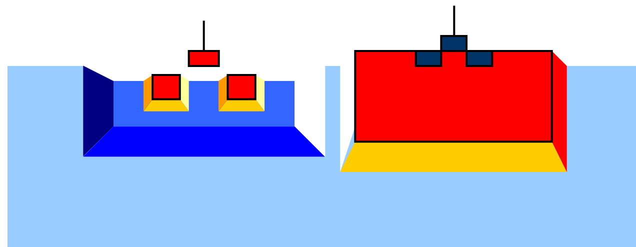
The use of a high voltage technology is not mandatory for the concept .
A SDA structure has been also implemented in a low-voltage 65 nm technology
Pixel size is 2.5µm!



SDA detector

Nine pixels of the SDA-based pixel detector implemented in 65nm CMOS technology.
3D presentation of the real layout.

HV CMOS detectors



Pixel

"Smart" Diode

n-Well

Drift

Potential energy (e-)

~15µm

Depletion zone

P-Substrate

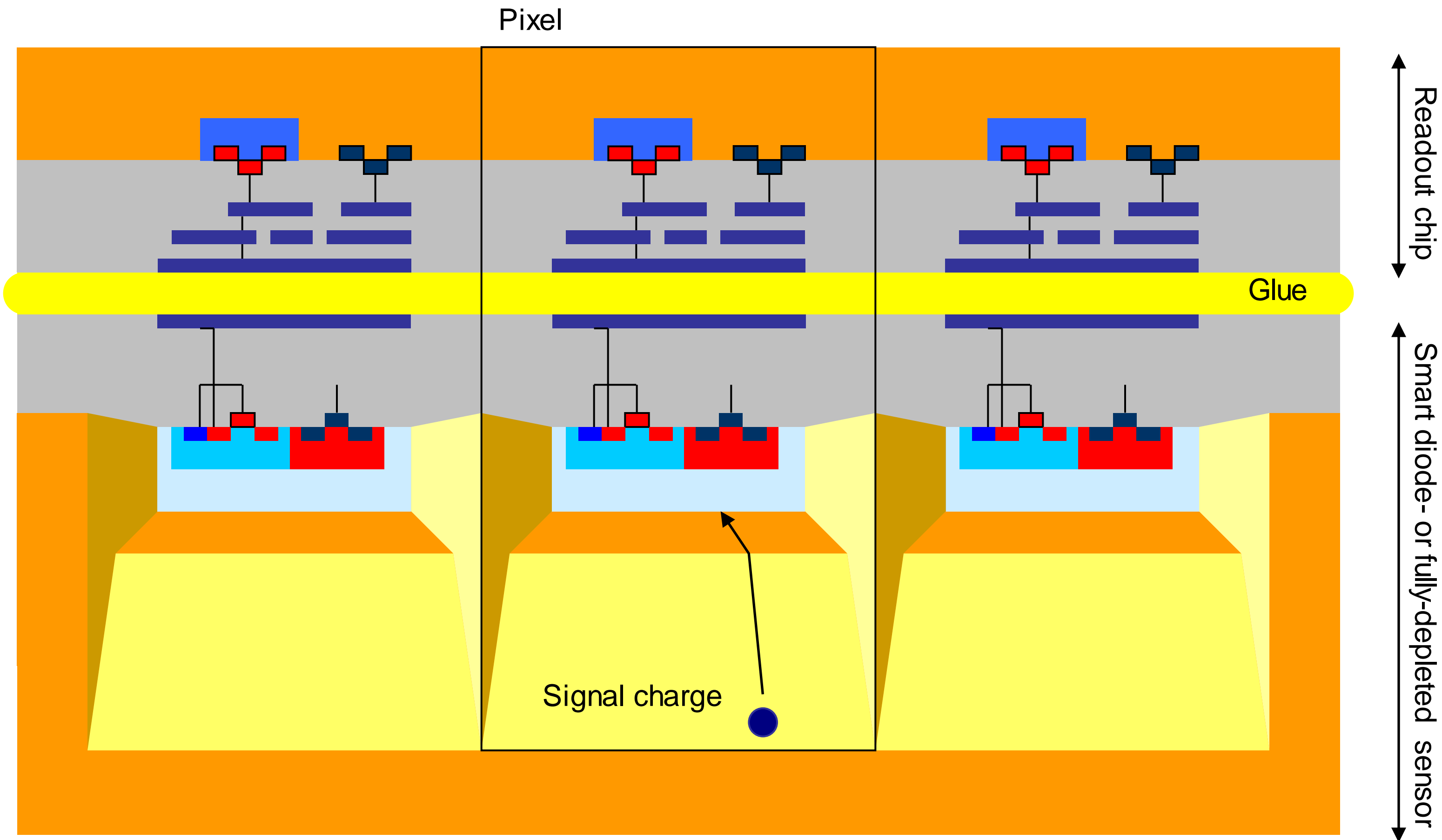
"Smart diode" array

The third dimension illustrates electron potential energy.

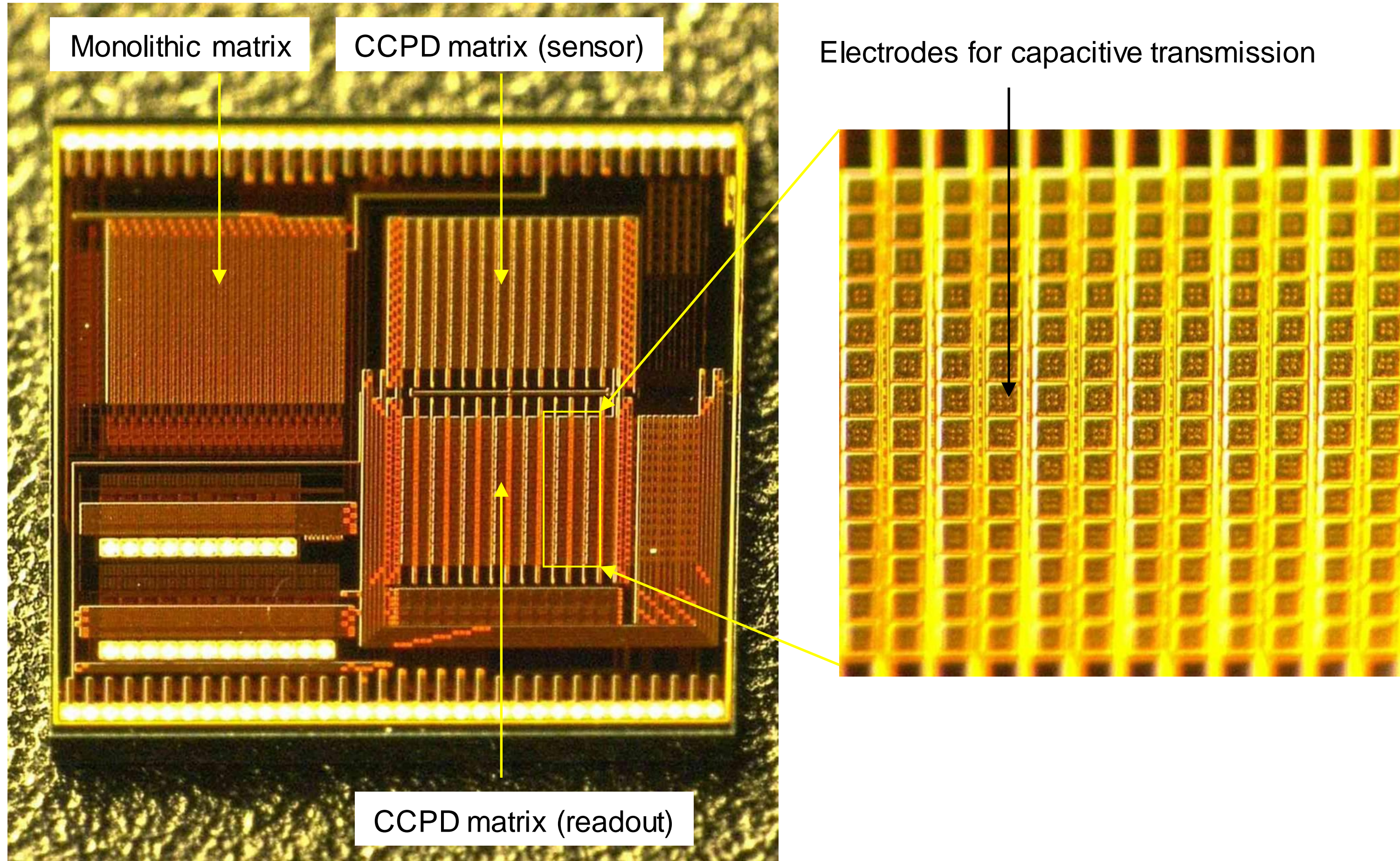
Strong points

- 1) Active sensor
- 2) CMOS in-pixel electronics – “intelligent “detectors.
- 3) Fast signal collection
  - ~15μm drift path, 50V
- 4) Thinning possible
  - Since the charge collection is limited to the chip surface, the sensors can be thinned.
- 5) Price and technology availability
  - Standard (HV) technology without any adjustment is used
  - Many industry relevant applications of HV CMOS technologies assure their long tern availability.
  - 180nm technology: 160k€ and 1.5k€/8 inch wafer (1 wafer ~ 200 cm^2)
  - The structure can be also implemented in many low voltage technologies.
- 6) High tolerance to non-ionizing radiation damage
  - High drift speed
  - Short drift path
- 7) High tolerance to ionizing radiation
  - Deep submicron technology
  - Radiation tolerant design can be used.
  - PMOS transistors, that are more tolerant to radiation, can be used as well in contrast to standard MAPS.

Capacitive Coupled Pixel Detectors
- CCPDs

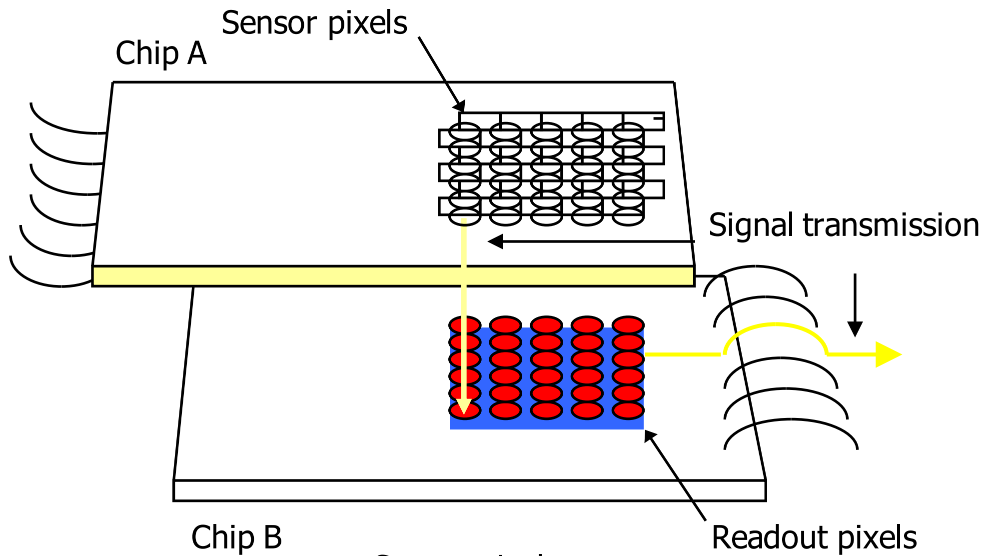


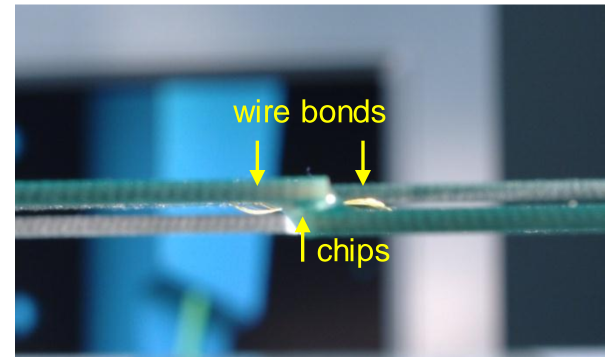
The signal from sensor chip is transmitted capacitively to the readout chip.
The sensor and readout chips are flipped and glued .

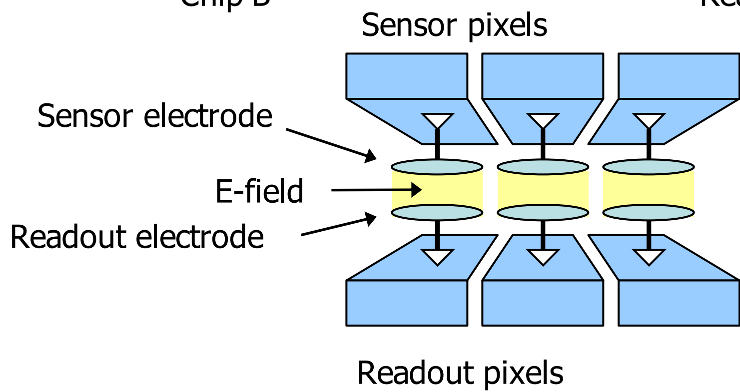


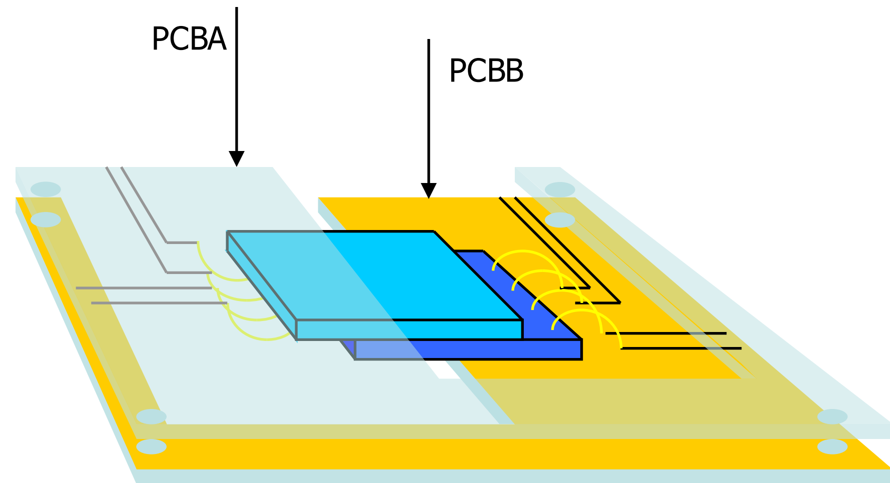
Sensor and readout matrix implemented as same design (to save costs)

CCPD - test system





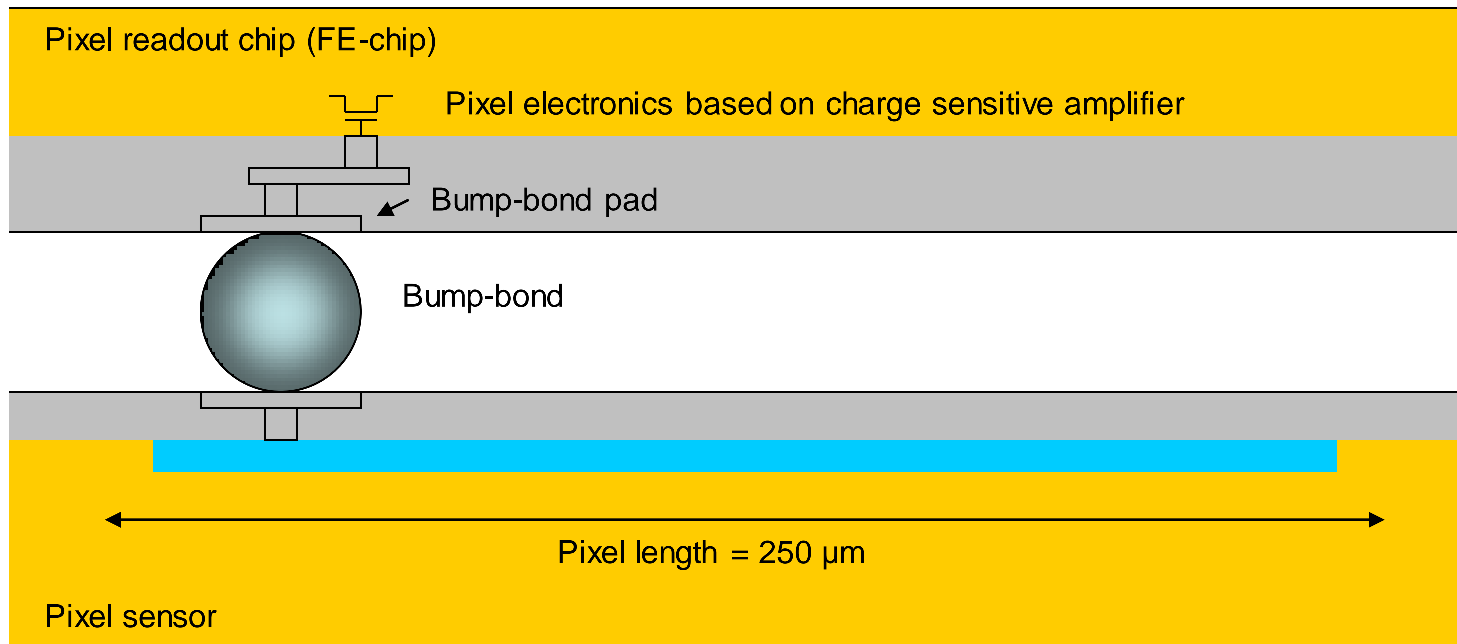




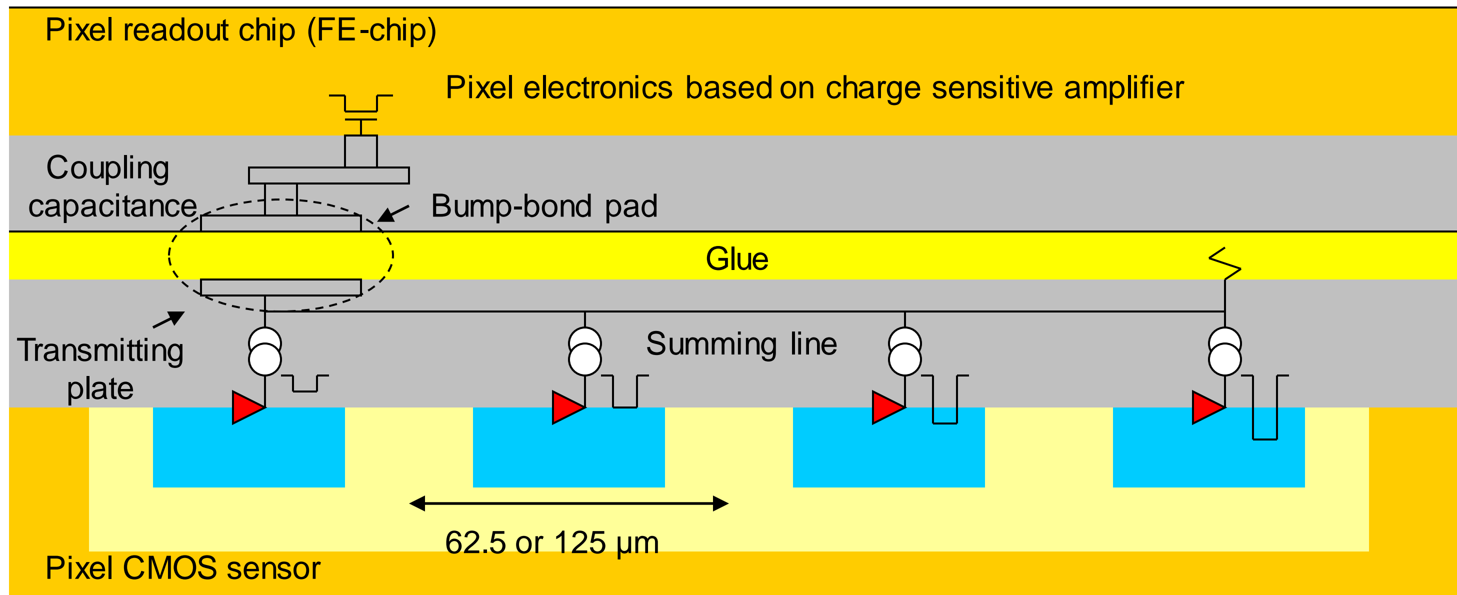
High-Voltage CMOS Detectors for ATLAS

CCPD Concept

- Replacing the passive diode-based pixel sensor with an “intelligent” pixel sensor implemented in HV CMOS technology.
- Intelligence: the pixels are able to distinguish a signal from the background and to respond to a particle hit by generating an address information.

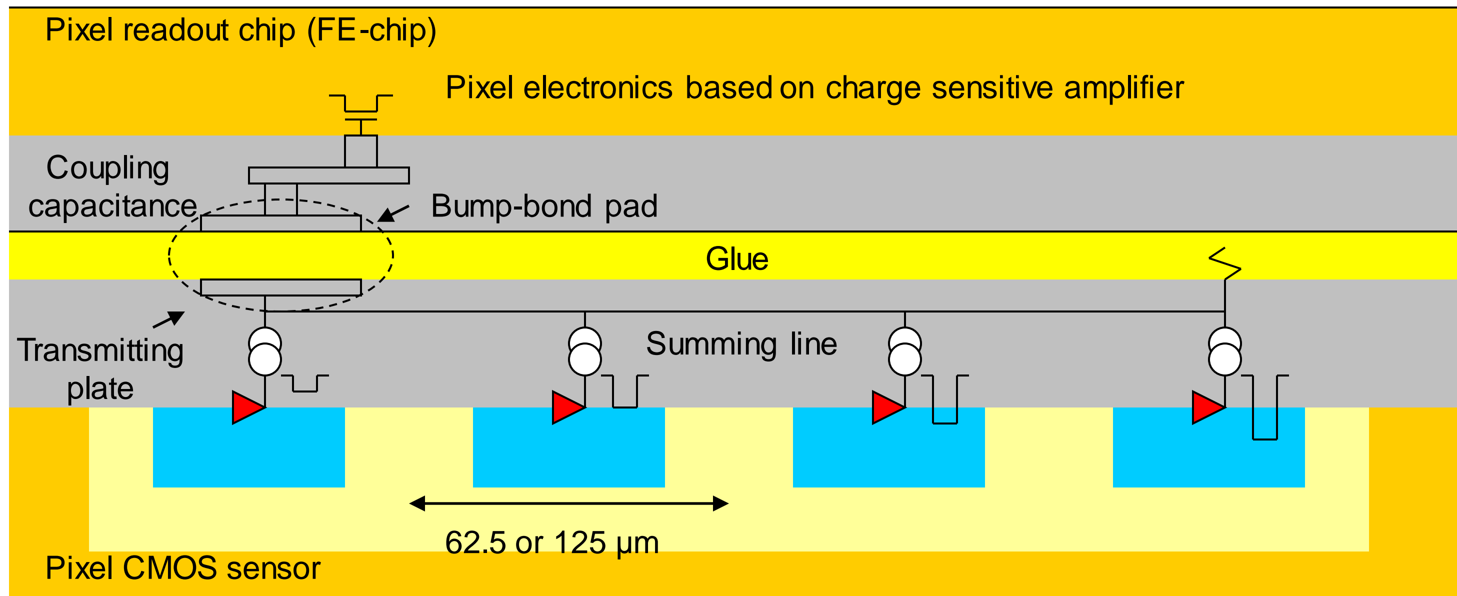


- The HVCMOS sensor pixels are smaller than the standard ATLAS pixels, for instance 25µm x 125µm - so that several such pixels cover the area of the original pixel.
- The HV pixels contain low-power (~5 µW) CMOS electronics based on a charge sensitive amplifier and a comparator.



CCPD for ATLAS pixel detector

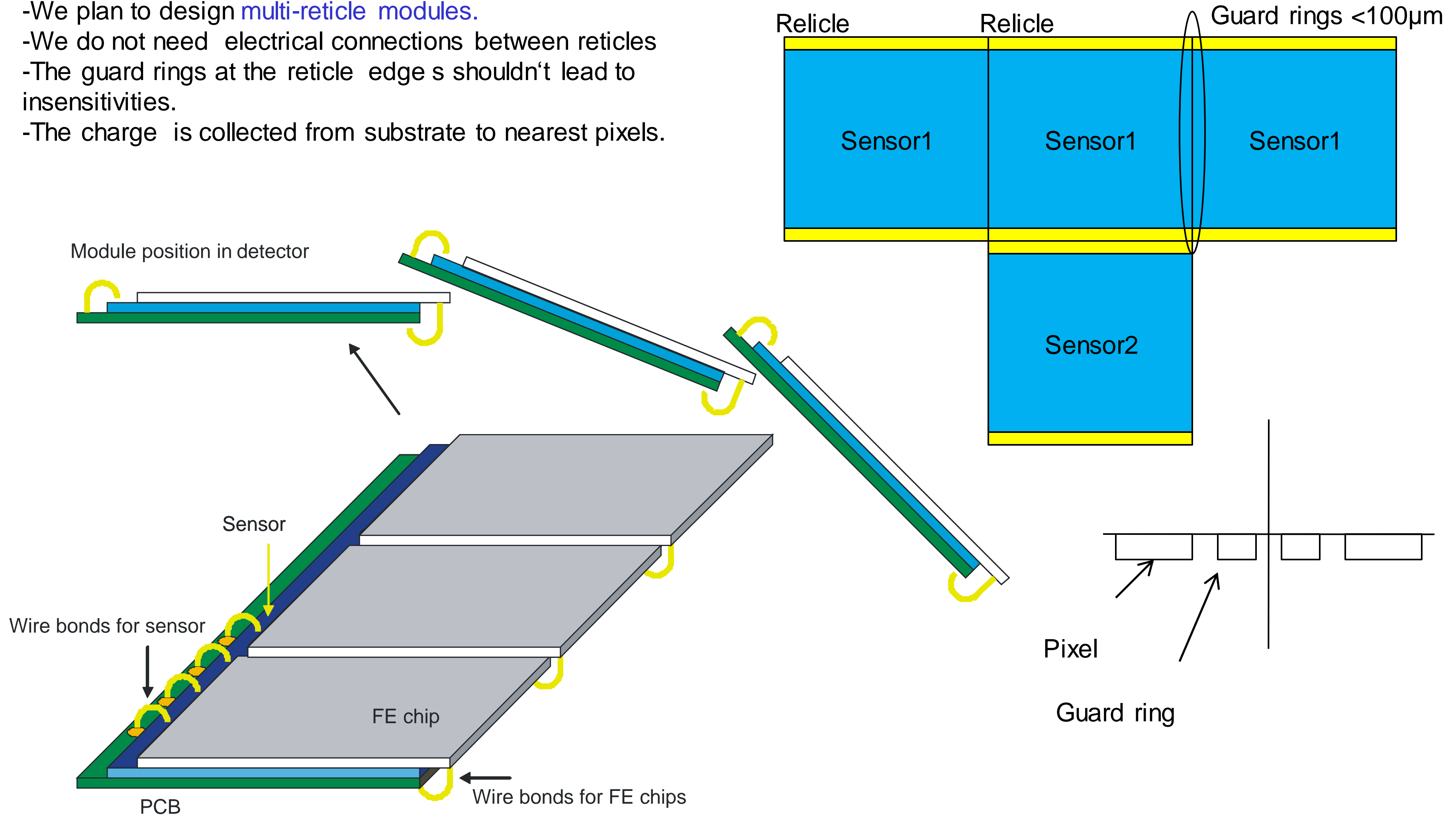
- The electronics responds to a particle hit by generating a pulse.
- The signals of a few pixels are summed, converted to voltage and transmitted to the charge sensitive amplifier in the corresponding channel of the FE chip using AC coupling.
- For comparison and testing purposes, the signal transmission can – in addition to capacitive coupling – also be established by classical bump-bonding.



- Each of the pixels that couple to one FE receiver can have its unique signal amplitude, so that the pixel can be identified by examining the amplitude information generated in FE chip.
- In this way, spatial resolution in φ- and z-direction can be improved.

Module concept

-We plan to design multi-reticle modules.
-We do not need electrical connections between reticles
-The guard rings at the reticle edge s shouldn‘t lead to insensitivities.
-The charge is collected from substrate to nearest pixels.

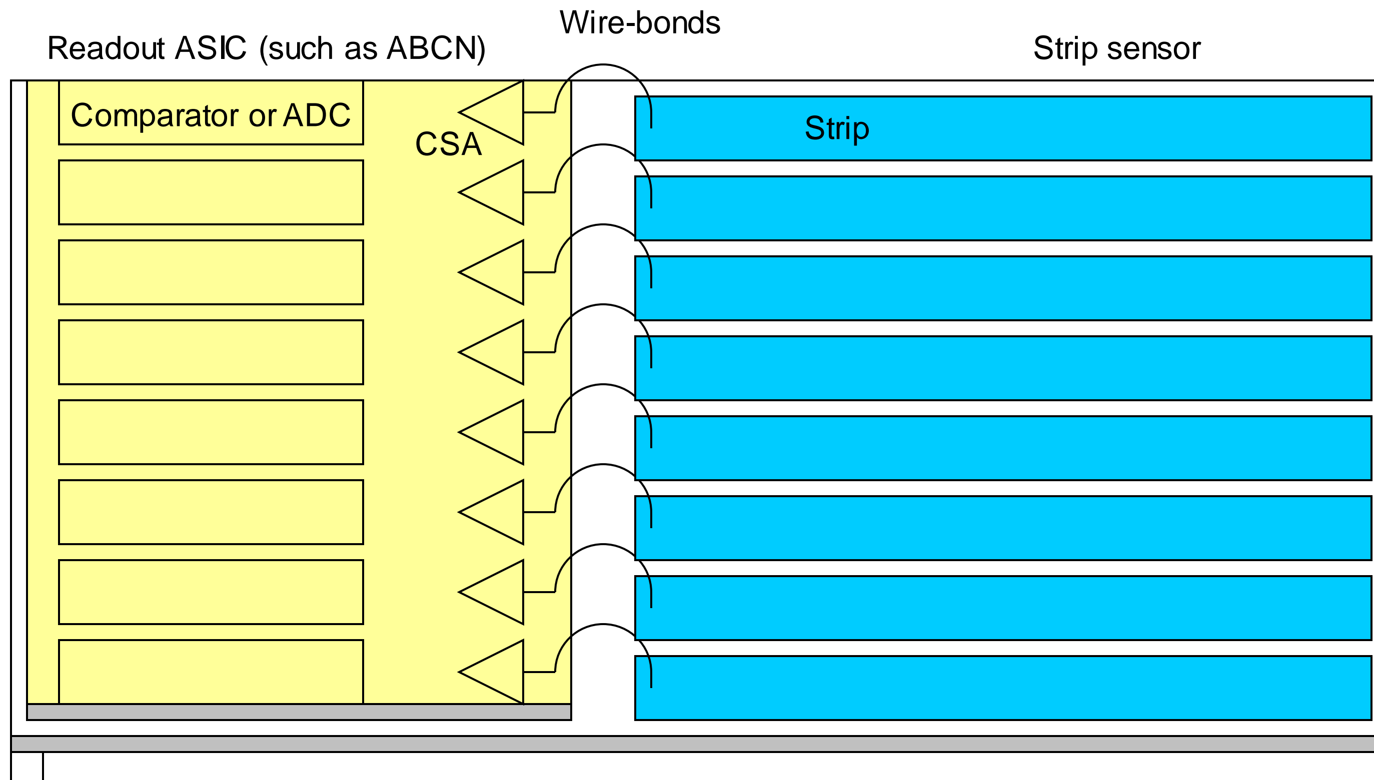


Advantages compared to existing detectors

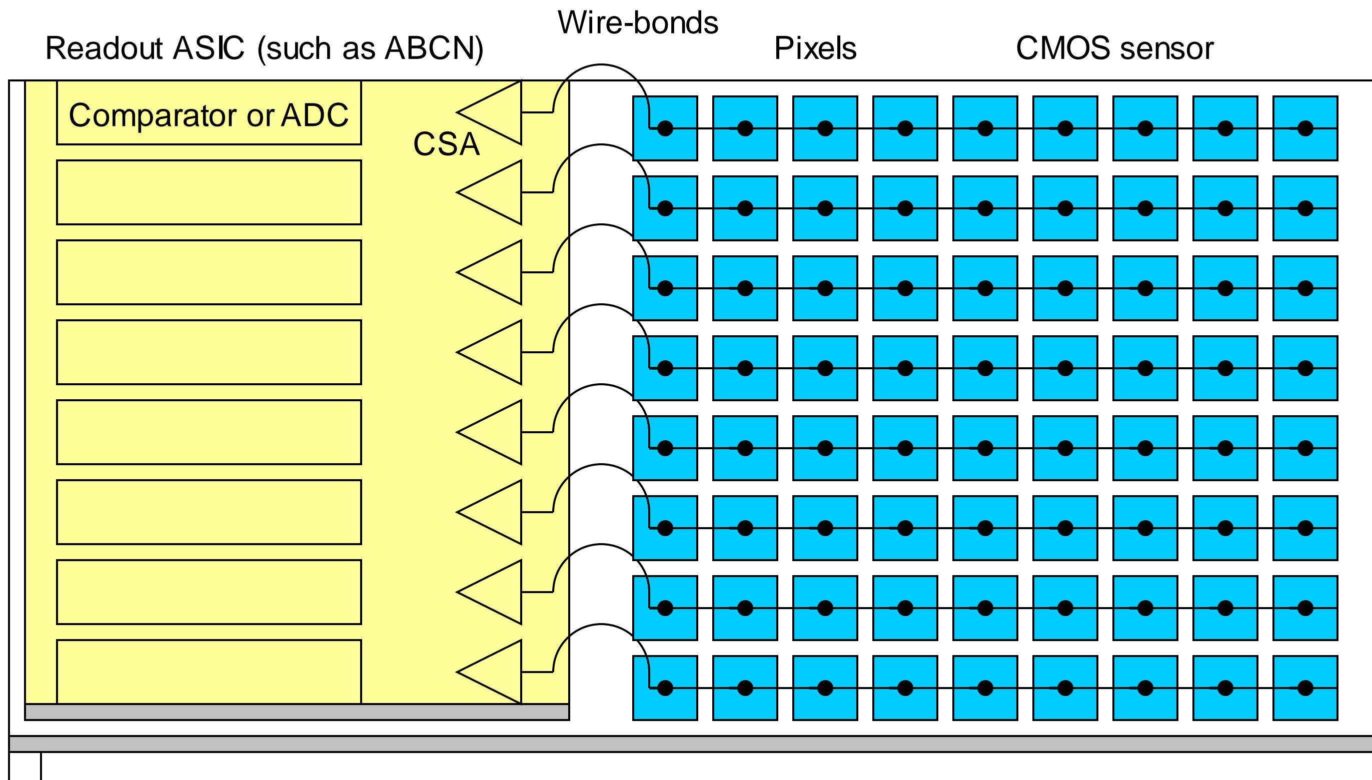
- No need for bump-bond connection between the sensor and readout chip – lower price, better mechanical stability, less material
- Commercial sensor technology – lower price
- No need for bias voltages higher than 60V
- Operation at temperatures above 0C is according to tests possible (irradiations to $10^{15}\ n_{eq}/cm^2$)
- Increased spatial resolution (e.g. 25μm x 125μm binary resolution) with the existing FE chip
- Smaller clusters at high incidence angles
- Possibility of sensor-thinning without signal loss. Since we do not use bumps and FE chips can be thinned as well, the amount of material would be very low.
- Interesting choice for other experiments where low-mass detectors are needed such as CLIC, ILC, CBM, etc...

Strip-like Concept

- Present LHC strip detectors consist of large-area strip sensors that are connected by wire bonds to multi-channel ASICs.

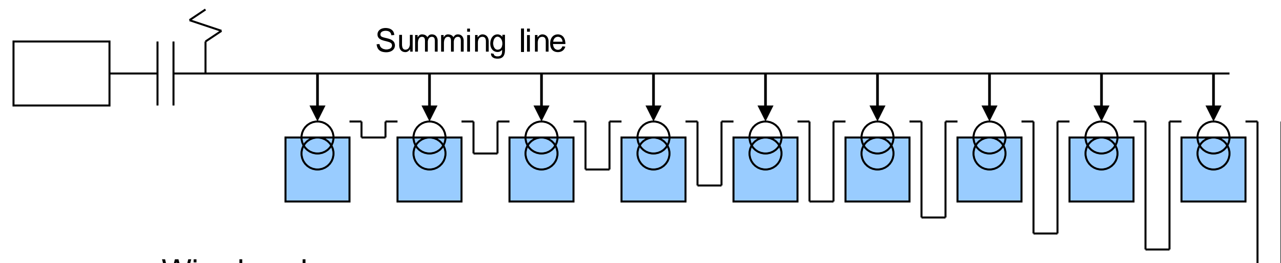


- We replace a strip with a line of pixels in HVCMOS technology.



Pixel detector compatible to strip-readout electronics

- Every pixel generates a digital pulse with unique amplitude of logic one.
- The pixel outputs are summed, converted to voltage signal and transmitted to readout ASIC.



Wire-bonds

Readout ASIC (such as ABCN)

Pixels

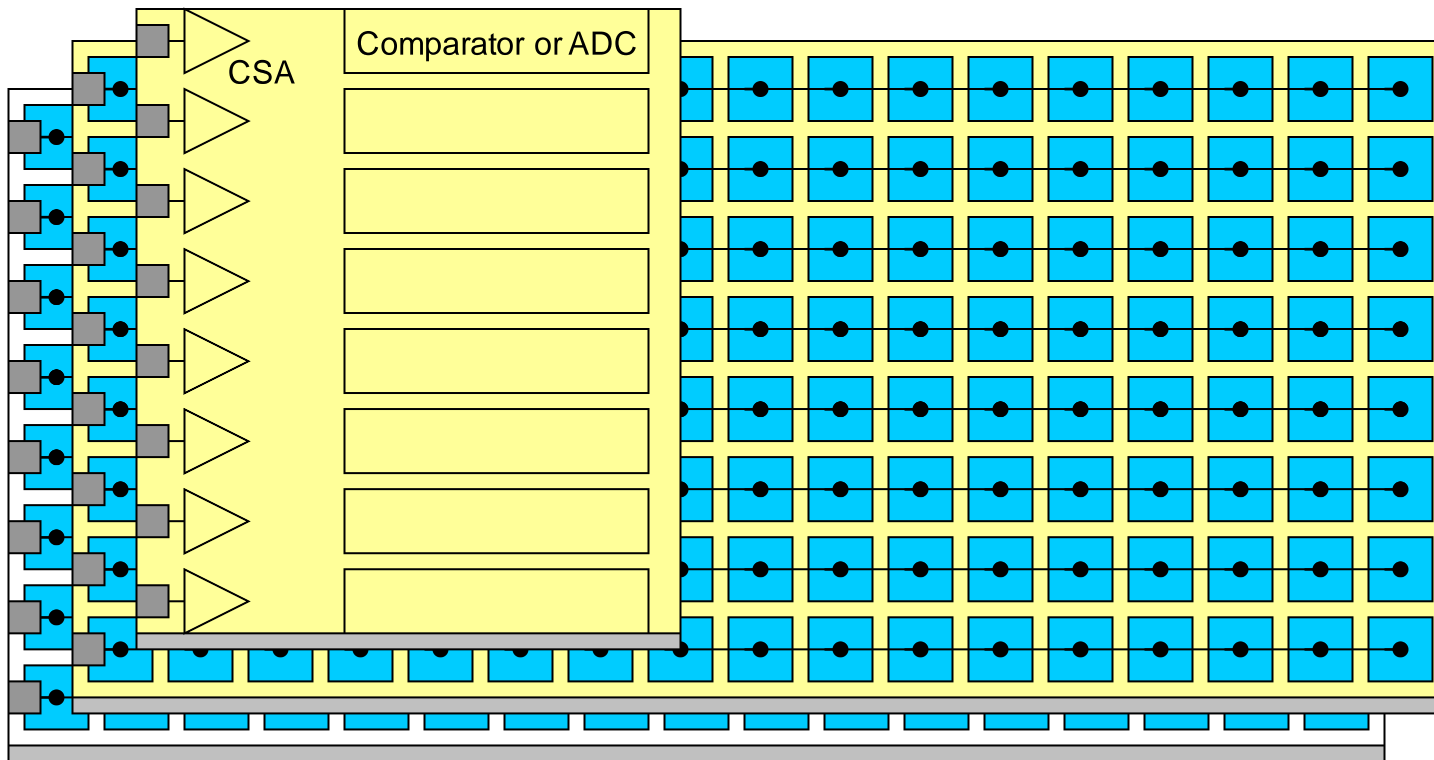
CMOS sensor

Comparator or ADC

CSA

- A large area CMOS sensor can be produced by stitching several 2cm x 2cm wafer reticles.
- Any arbitrary pixel group pattern is possible.
- Advantages:
- Commercial sensor technology – lower price per unit area
- Intrinsic 2D spatial resolution (e.g. 25 μm x 125 μm binary resolution)
- No need for bias voltages higher than 60V
- Operation at temperatures above 0C is according to tests possible (irradiations to 10^{15} n_{eq}/cm^2)
- Thinning possible

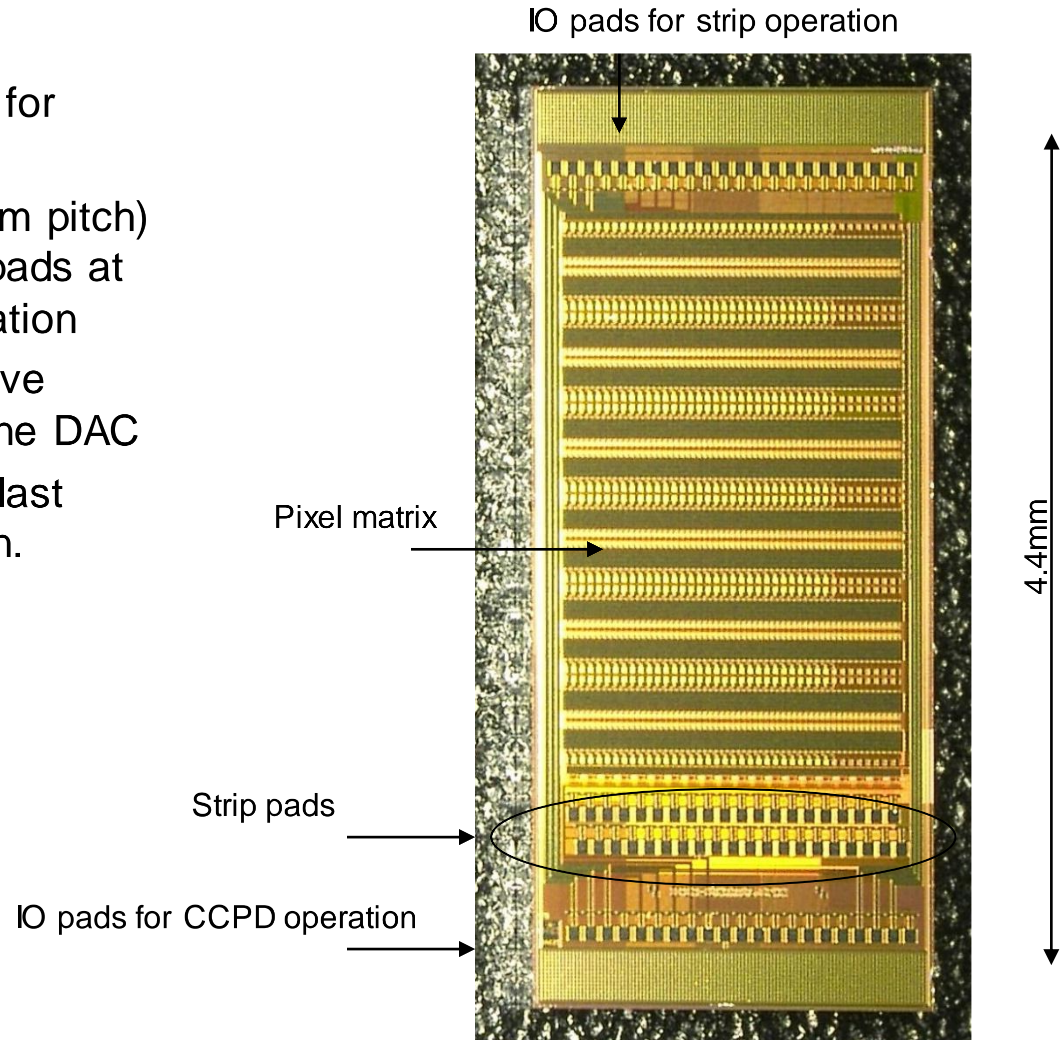
- Simultaneous readout from two 2D sensitive layers. Signals from two sensor layers can be easily combined in a single readout ASIC.

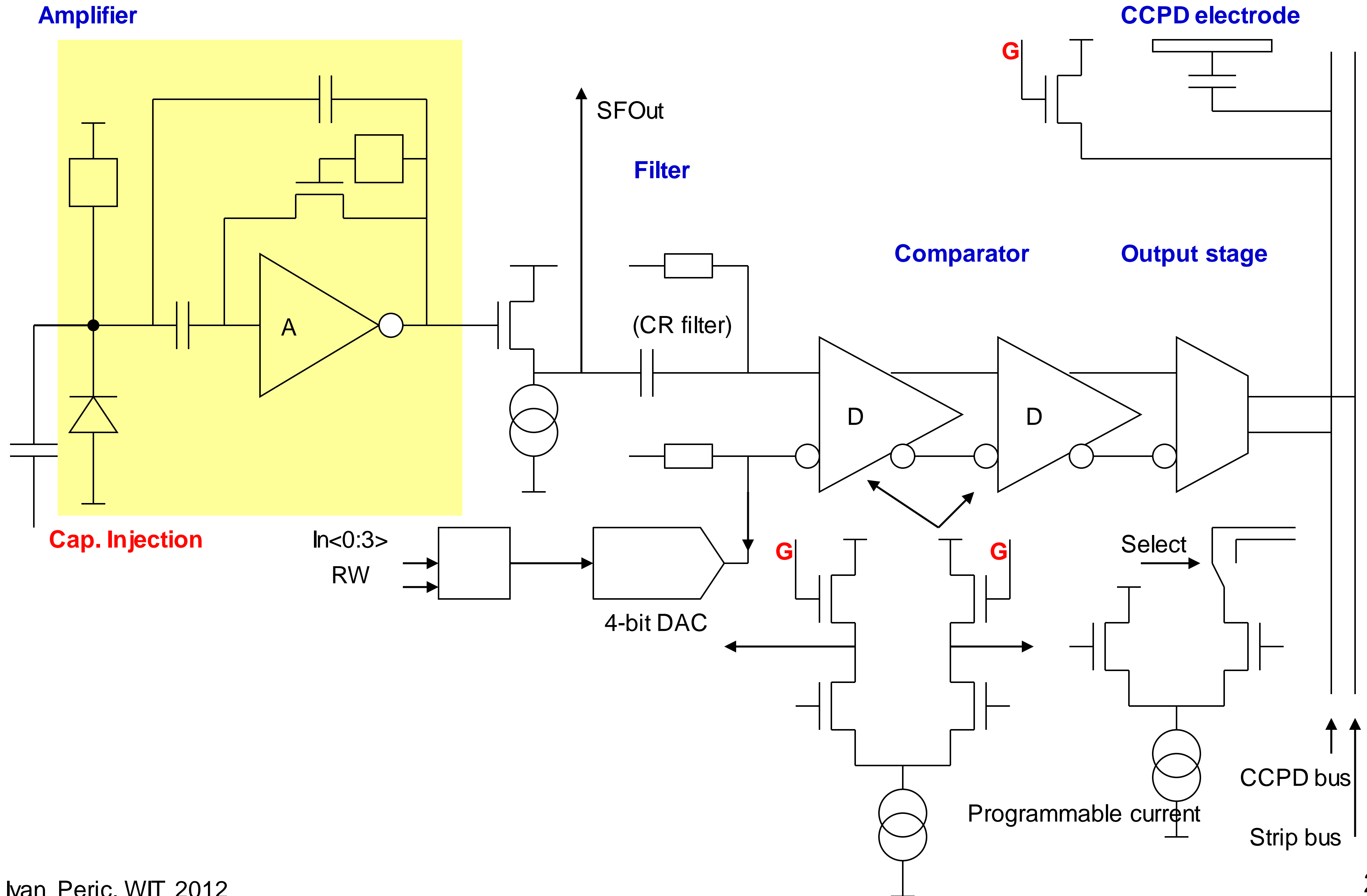


Test Chip HV2FEI4

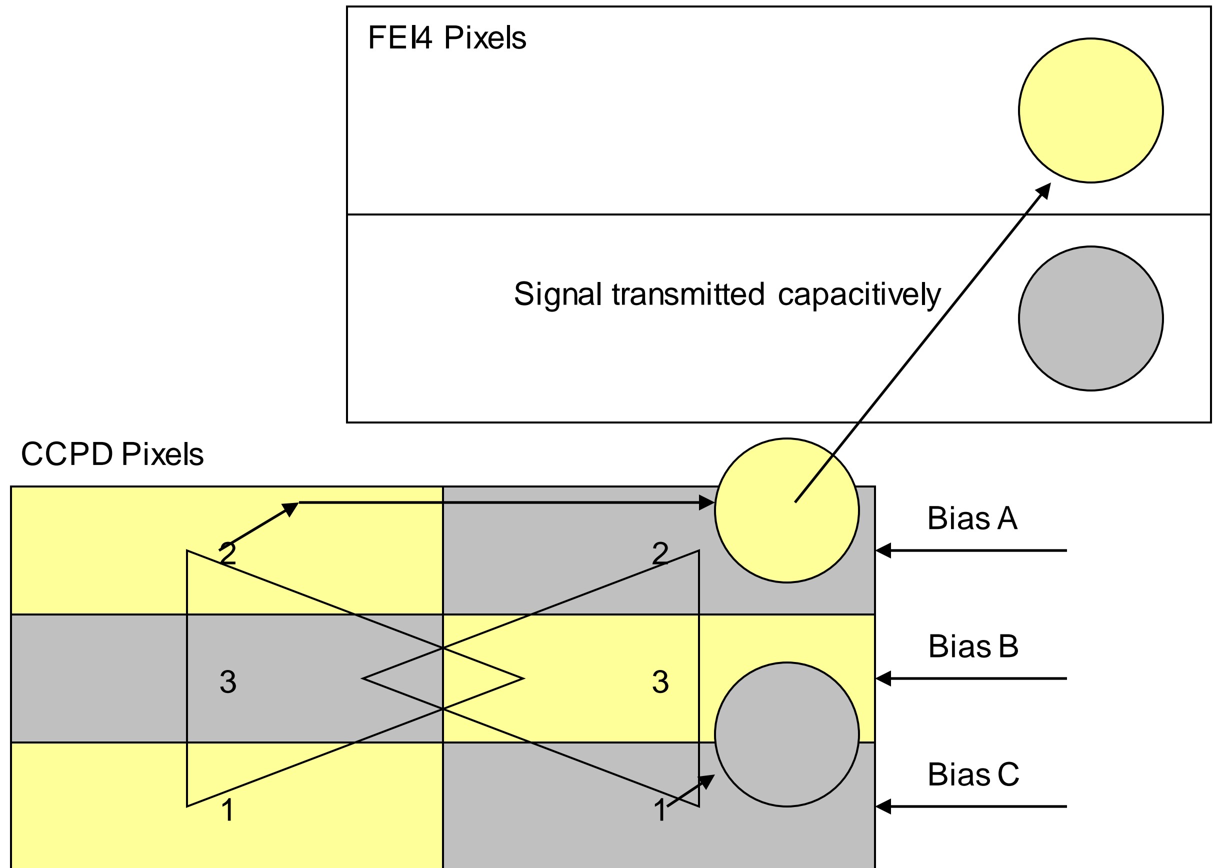
HV2FEI4

- Pixel matrix: 60x24 pixels
- Pixel size 33 μm x 125 μm
- 21 IO pads at the lower side for CCPD operation
- 40 strip-readout pads (100 μm pitch) at the lower side and 22 IO pads at the upper side for strip-operation
- Pixel contains charge sensitive amplifier, comparator and tune DAC
- We have received the chips last week – first results very soon.

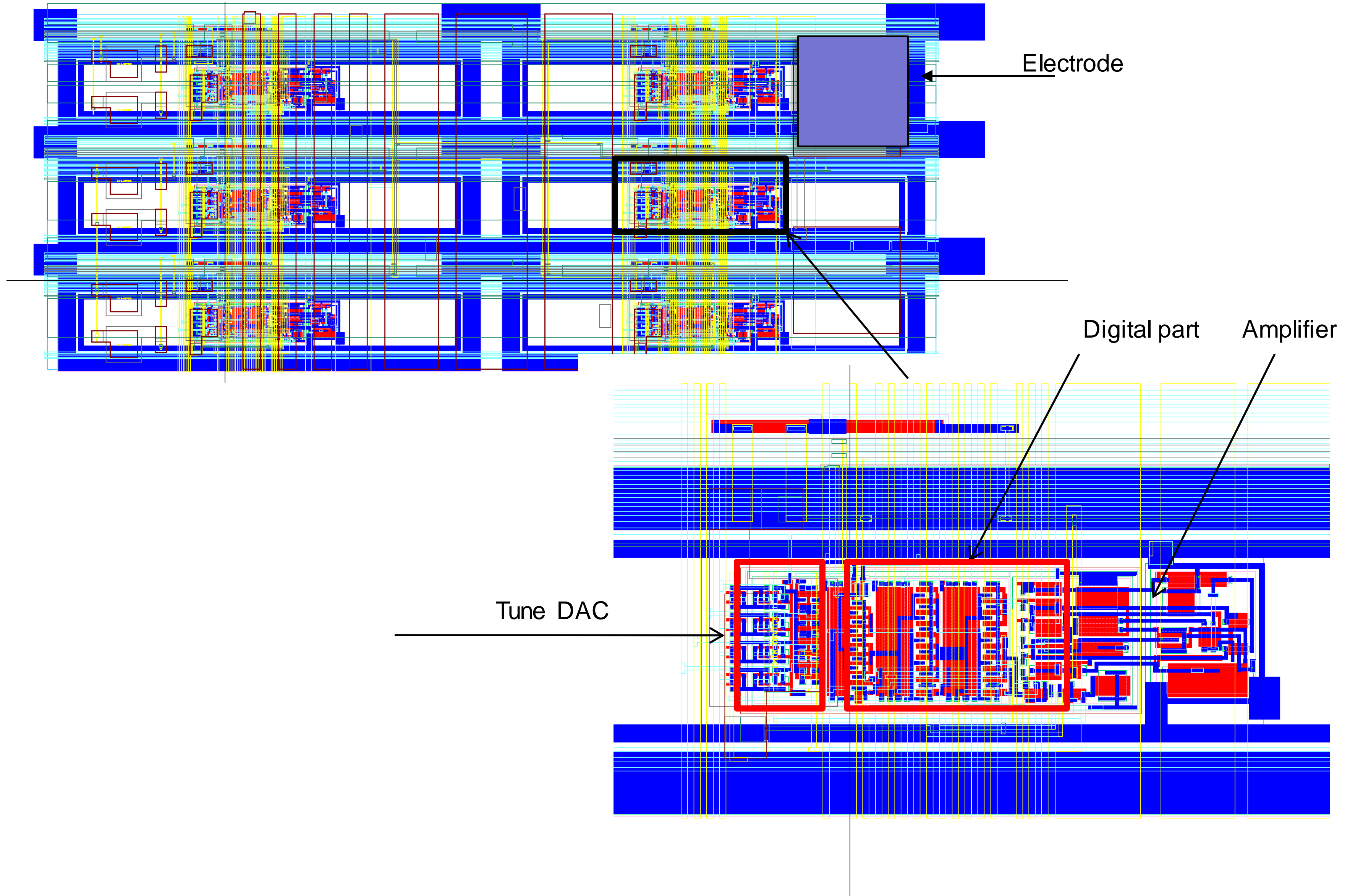



Amplifier
CCPD electrode
G
SFOut
Filter
Comparator
Output stage
A
(CR filter)
D
D
Cap. Injection
In<0:3>
RW
4-bit DAC
G
G
Select
Programmable current
CCPD bus
Strip bus

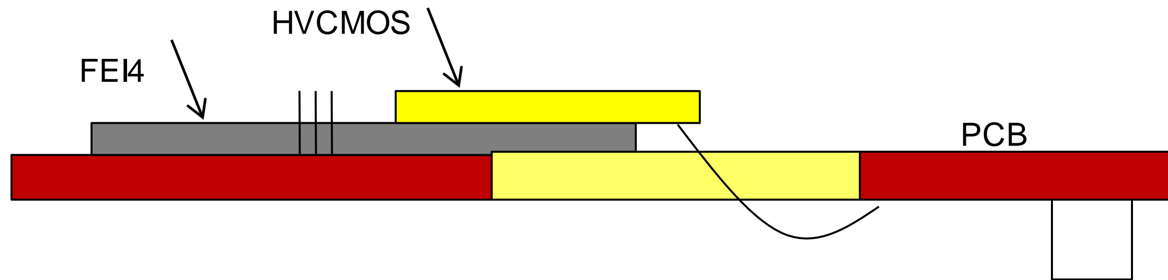
CCPD Operation

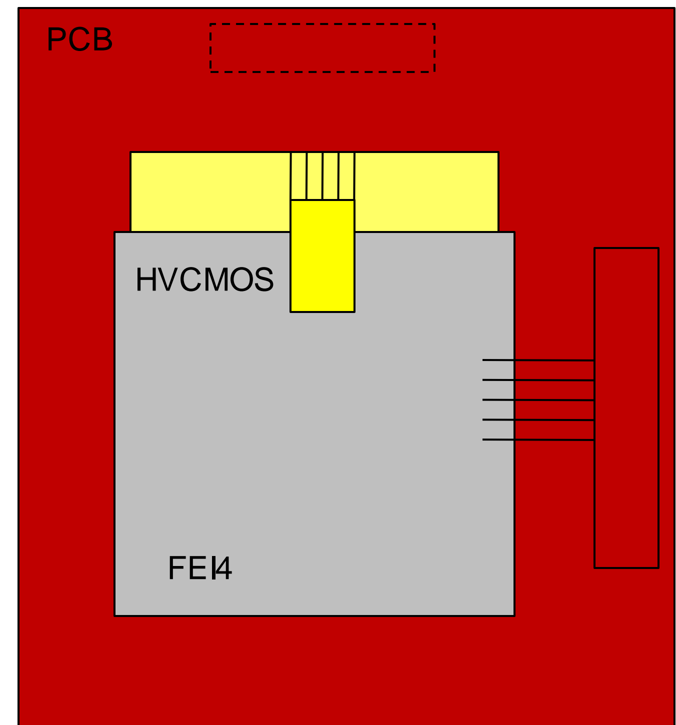


6 Pixels – Layout



Test setup



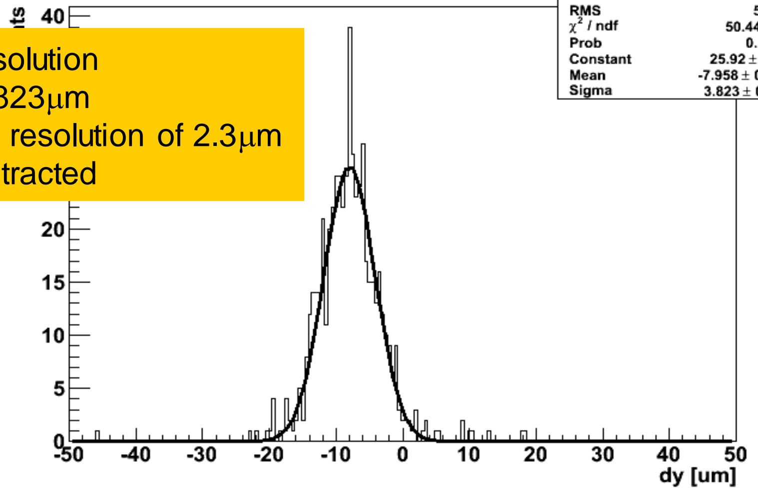


Experimental Results with other Prototypes

Efficiency and Signal Amplitude

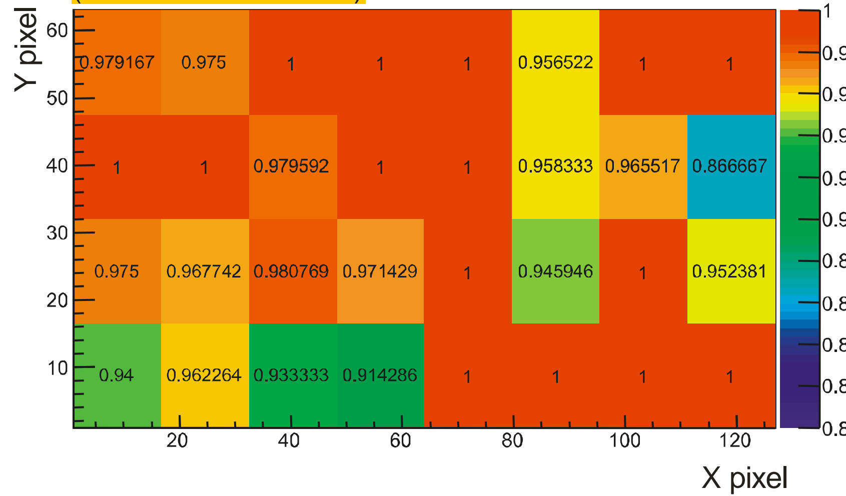
Rolling Shutter Detector

Test-beam results



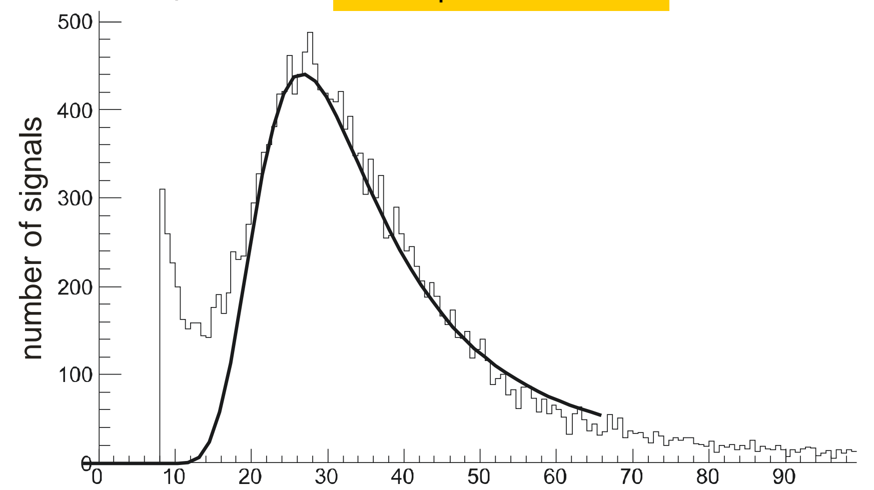
Spatial resolution
Sigma: 3.823µm
Telescope resolution of 2.3µm is not subtracted

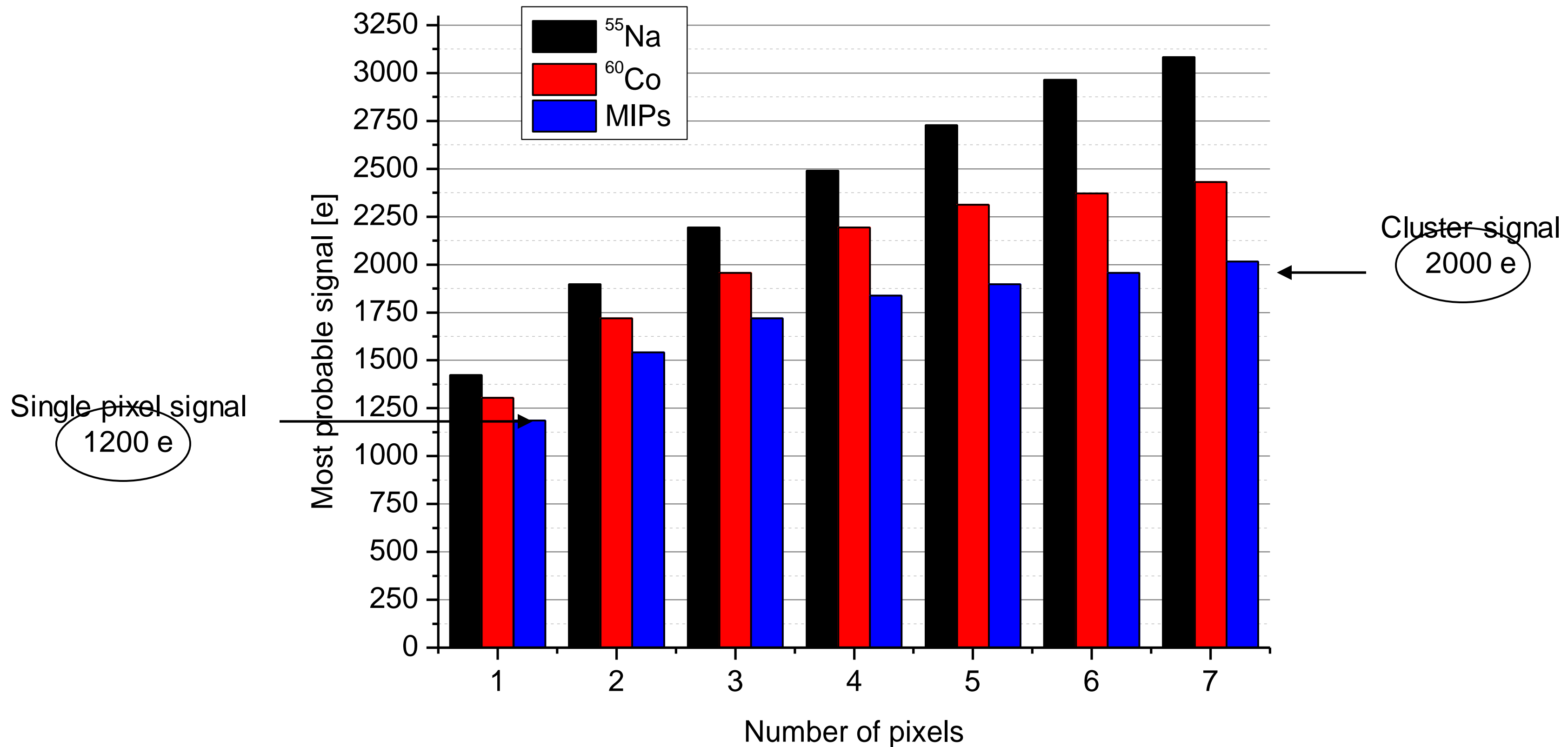
Efficiency vs pixel xy-coordinates
(Mean value = 0.9761)



Seed pixel SNR

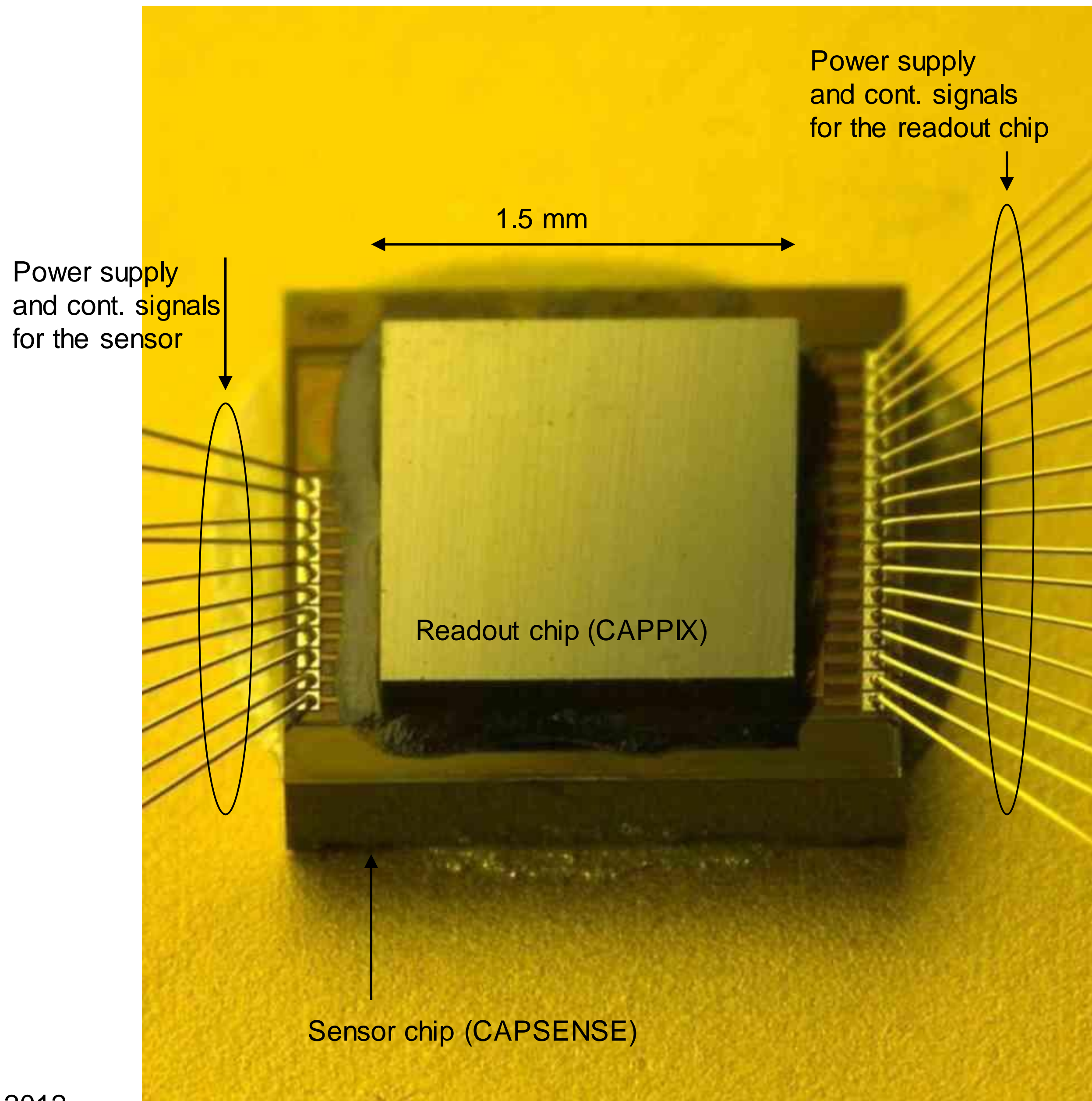
Seed pixel SNR = 27





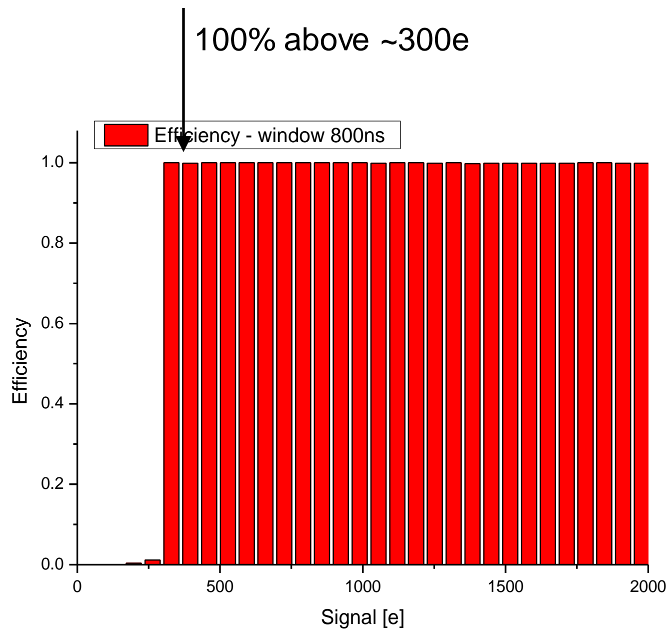
High energy particle signals depending on number of pixels in cluster.

CCPD Operation

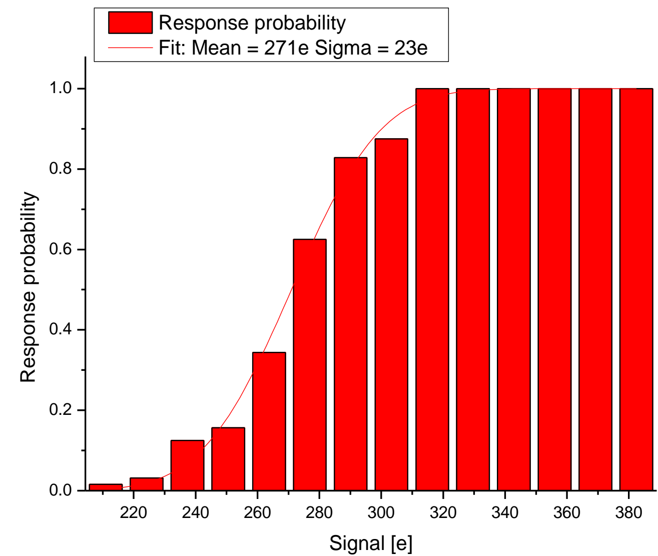

Power supply
and cont. signals
for the readout chip
1.5 mm
Power supply
and cont. signals
for the sensor
Readout chip (CAPPIX)
Sensor chip (CAPSENSE)

Noise measurement and efficiency

Response probability of all pixels in the matrix to test pulses that generate from 0 to 2000 electrons



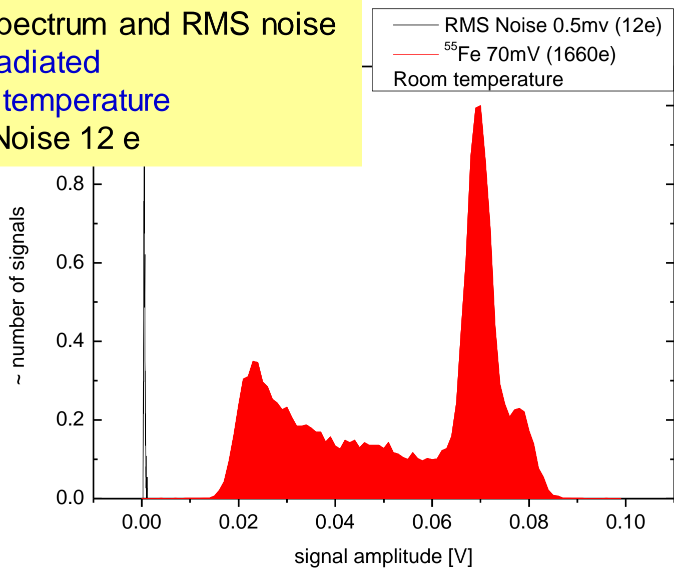
Threshold scan used to measure noise – noise 23e



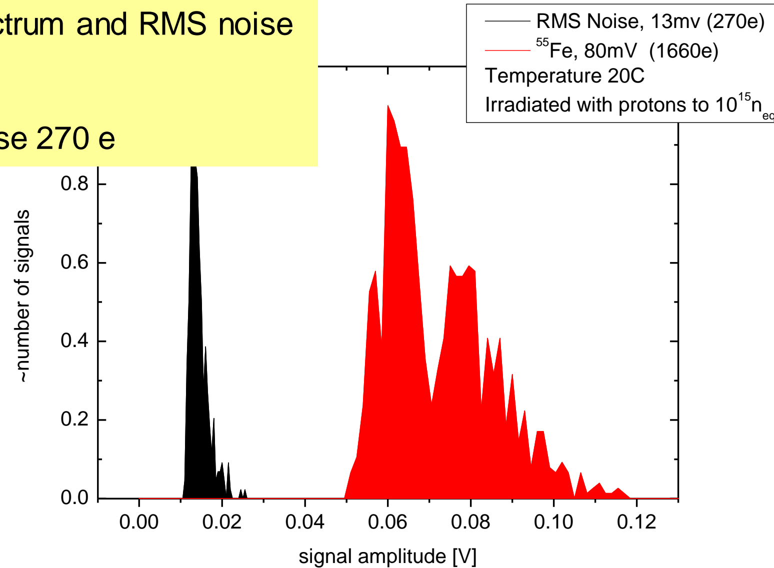
Radiation Tolerance
(CCPD2 Sensor)

Irradiation with protons (10^{15} n_{eq}/cm^2, 300 MRad)

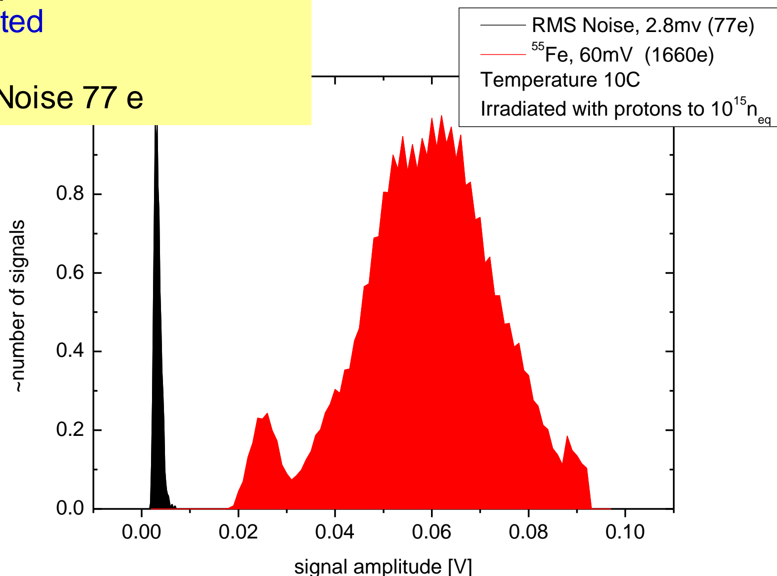
^{55}Fe spectrum and RMS noise
Not irradiated
Room temperature
RMS Noise 12 e



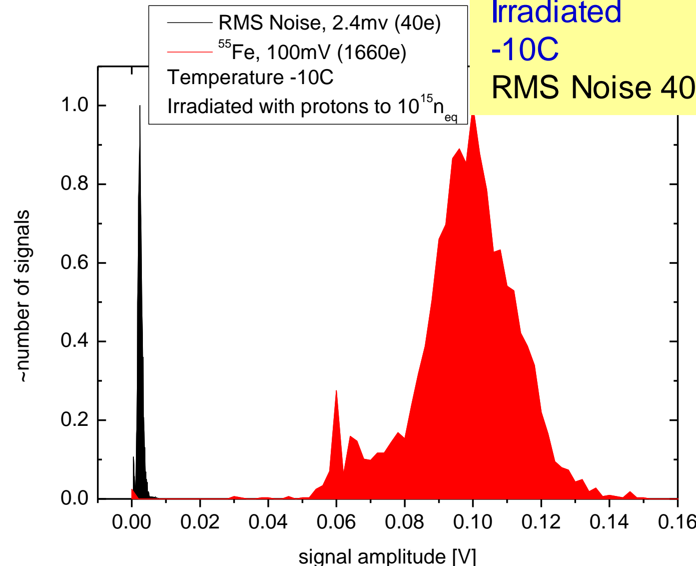
^{55}Fe spectrum and RMS noise
Irradiated
20C
RMS Noise 270 e



^{55}Fe spectrum, RMS noise
Irradiated
10C
RMS Noise 77 e

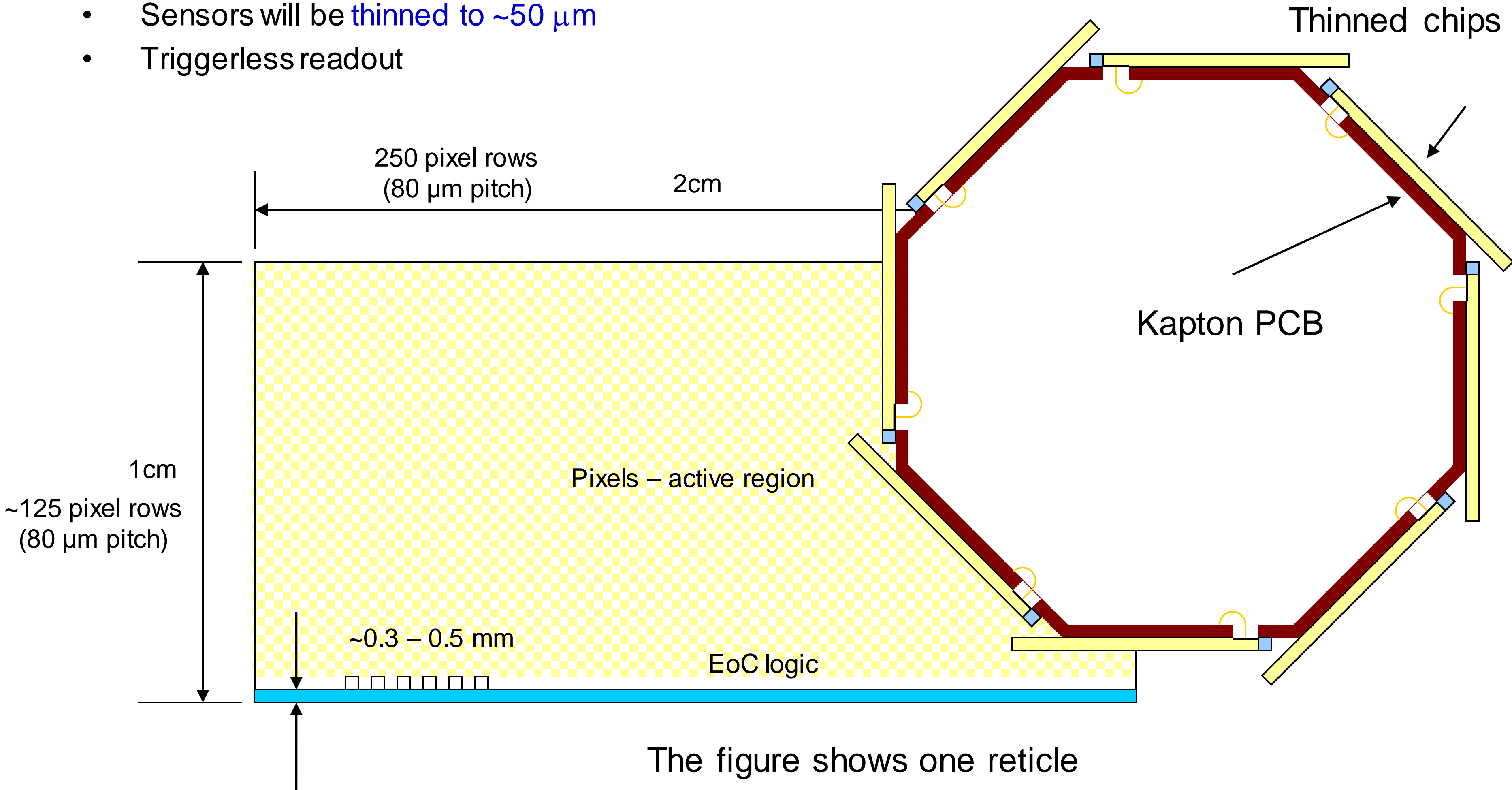


^{55}Fe spectrum, RMS noise
Irradiated
-10C
RMS Noise 40 e



Time Resolution

- Mu3e experiment at PSI (study of the lepton flavor violating decay mu -> eee)
- Proposed: four layers of pixels ~ 80x80μm² size – monolithic pixel detector in HVCMOS technology
- Time stamping with < 100ns resolution required to reduce the number of tracks in an image.
- Sensors will be thinned to ~50 μm
- Triggerless readout



The figure shows one reticle

- More details can be seen in poster session:
- Dirk Wiedner: “A tracker for the novel mu3e experiment based on high voltage monolithic active pixel sensors”

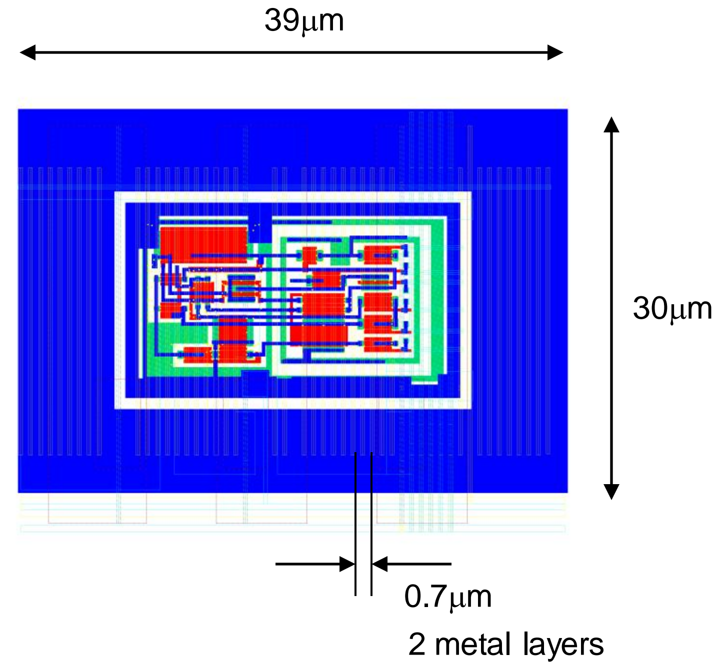
Mu3e Test Chip in 180nm Technology

1.8mm

42x36 pixels

Analog pixels

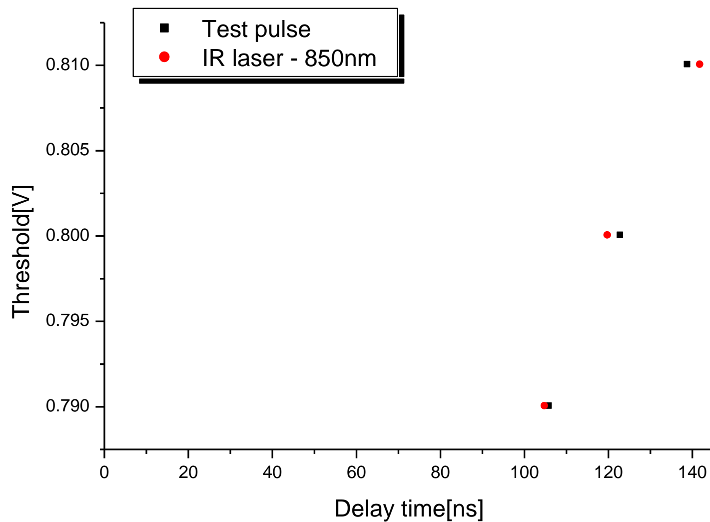
Digital channels

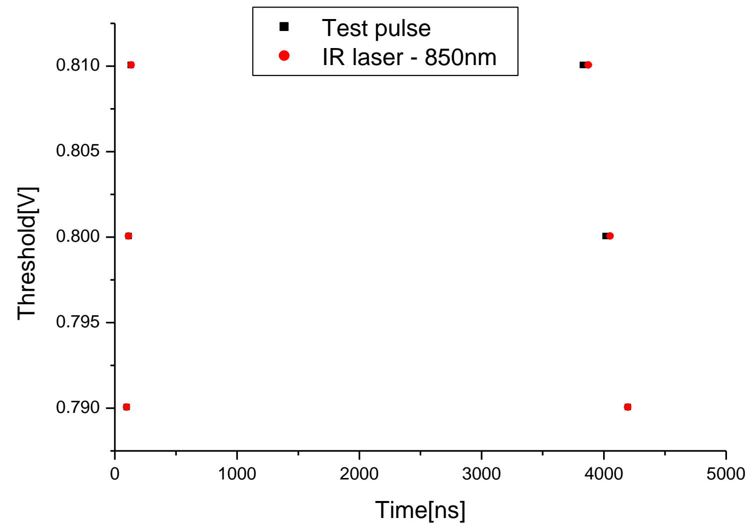


Analog pixel layout

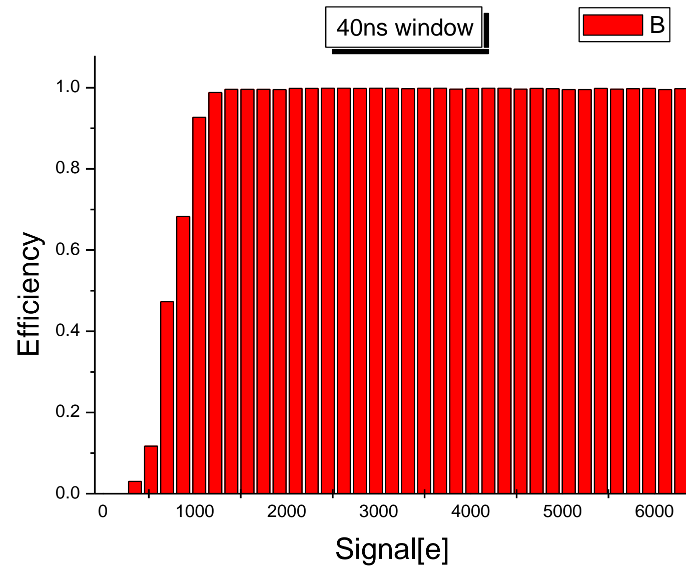
Pixel detector chip with CMOS pixel (42x40 pixels) matrix
Pixel size 39x30 micrometers
Separated digital and analog block
Signal time measurements possible

- Charge collection time – IR laser, comparison with the fast capacitive injection.
- No measurable delay versus the capacitive test pulse.



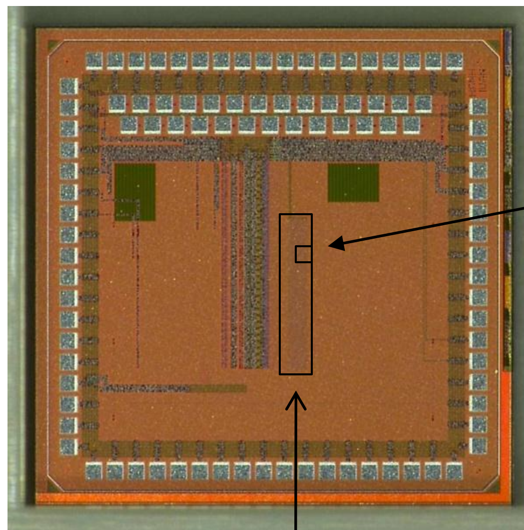


- In-time efficiency vs. signal amplitude (40ns time window)
- Detection of signals > 1230 e with 40ns time resolution possible.
- Power consumption of the pixel 7.5µm.

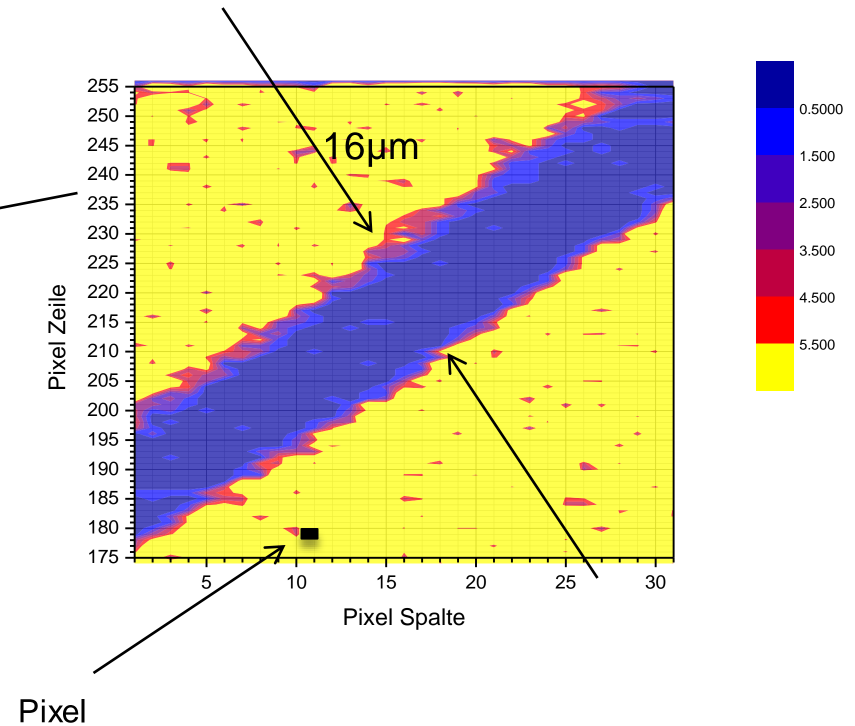


- Pixel size - 2.5µm

55Fe measurement
Shadow of 16µm thick golden bonding wire



Pixel matrix (32x256)



Experimental results - overview

HVPixel1 – **CMOS in-pixel electronics with hit detection**
Binary RO
Pixel size 55x55µm
Noise 60e
MIP seed pixel signal 1800 e
Time resolution 200ns

Capacitive coupled hybrid detector

CCPD2 -**capacitive coupled pixel detector**
Pixel size 50x50µm
Noise 30-40e
Time resolution 300ns
MIP SNR 45-60

Irradiations of test pixels
60MRad – MIP SNR 22 at 10C (CCPD1)
$10^{15}n_{eq}$ MIP SNR 50 at 10C (CCPD2)

HV2FEI4 chip (first test next week!!!)
CCPD for ATLAS pixel detector
Readout with FEI4 chip
Reduced pixel size: 33x125µm
RO type: capacitive and strip like
3 pixels connected to one FEI channel

Monolithic detector – continuous readout with time measurement

MuPixel –
Monolithic pixel sensor for Mu3e experiment at PSI
Charge sensitive amplifier in pixels
Hit detection, zero suppression and time measurement at chip periphery
Pixel size: 39x30 µm (test chip)
(80 x 80 µm required later)
MIP seed signal 1500e (expected)
Noise: ~40 e (measured)
Time resolution < 40ns
Power consumption 7.5µW/pixel

Monolithic detector - frame readout

PM2 chip - frame mode readout
Pixel size 21x21µm
4 PMOS pixel electronics
128 on-chip ADCs
Noise: 21e (lab) - 44e (test beam)
MIP signal - cluster: 2000e/seed: 1200e
Test beam: **Detection efficiency >98%**
Seed Pixel SNR ~ 27
Cluster signal/seed pixel noise ~ 47
Spatial resolution ~ 3.8 µm

HPixel - frame mode readout
In-pixel CMOS electronics with CDS
128 on-chip ADCs
Pixel size 25x25 µm
Noise: 60e (preliminary)
MIP signal - cluster: 2100e/seed: 1000e (expected)

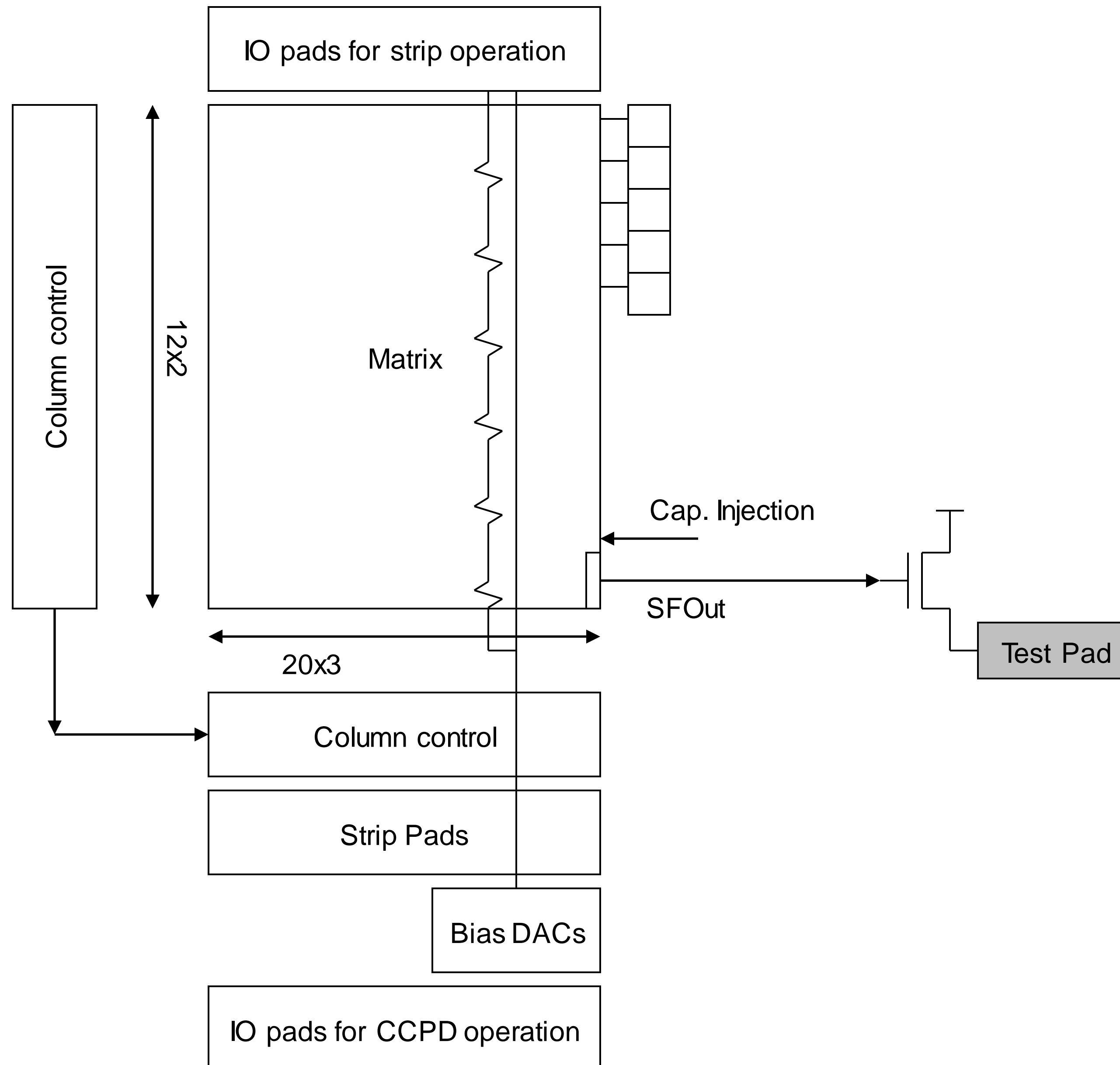
SDS - frame mode readout
Pixel size 2.5x2.5 µm
4 PMOS electronics
Noise: 20e (preliminary)
MIP signal (~1000e - estimation)

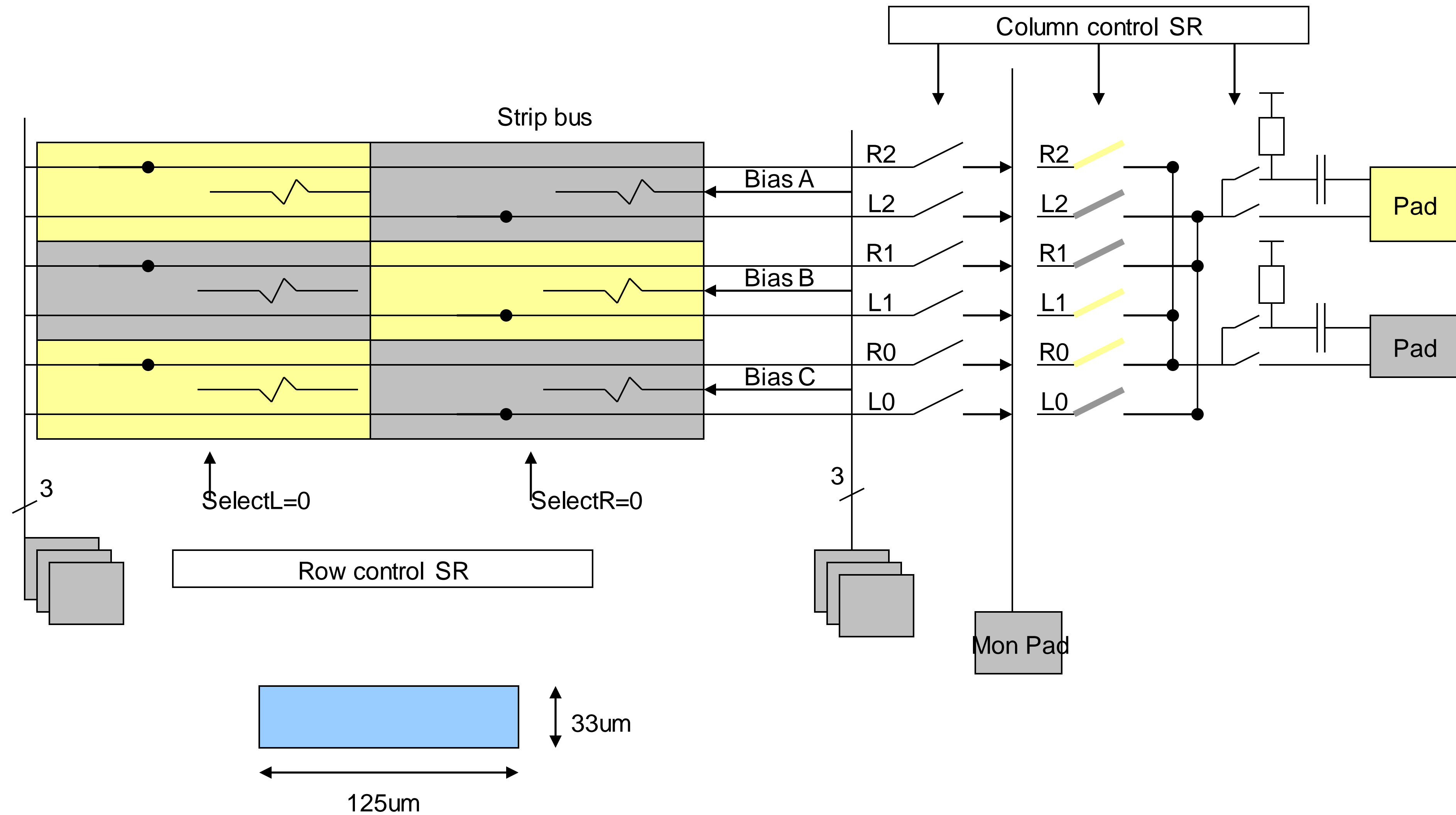
1. Technology 350nm HV – substrate 20 Ωcm uniform
2. Technology 180nm HV – substrate 10 Ωcm uniform
3. Technology 65nm LV – substrate 10 Ωcm/10 µm epi

- We have developed a new pixel sensor structure (smart diode array) for high energy physics that is implemented in high voltage CMOS technologies.
- The advantages over conventional silicon sensors include lower cost, lower mass, lower operating voltage, smaller pitch, and smaller clusters at high incidence angles, all with comparable radiation hardness.
- We have implemented various test structures in 350nm and 180nm technologies and measured excellent detection and radiation properties.
- Measured time resolution < 40ns (IR laser), detection efficiency ~98% (test beam)
- Irradiated up to 10^{15} n_{eq}/cm^2 and dose 300MRad
- We would like to integrate our sensors into existing ATLAS readout systems, for this we have two concepts:
- Capacitive coupled pixel detectors -> readout with pixel readout chips like FEI4
- Strip-like sensors -> readout with strip readout AISCs
- We have designed a test detector (in 180nm HV CMOS technology) to test the two concepts – first measurements soon.

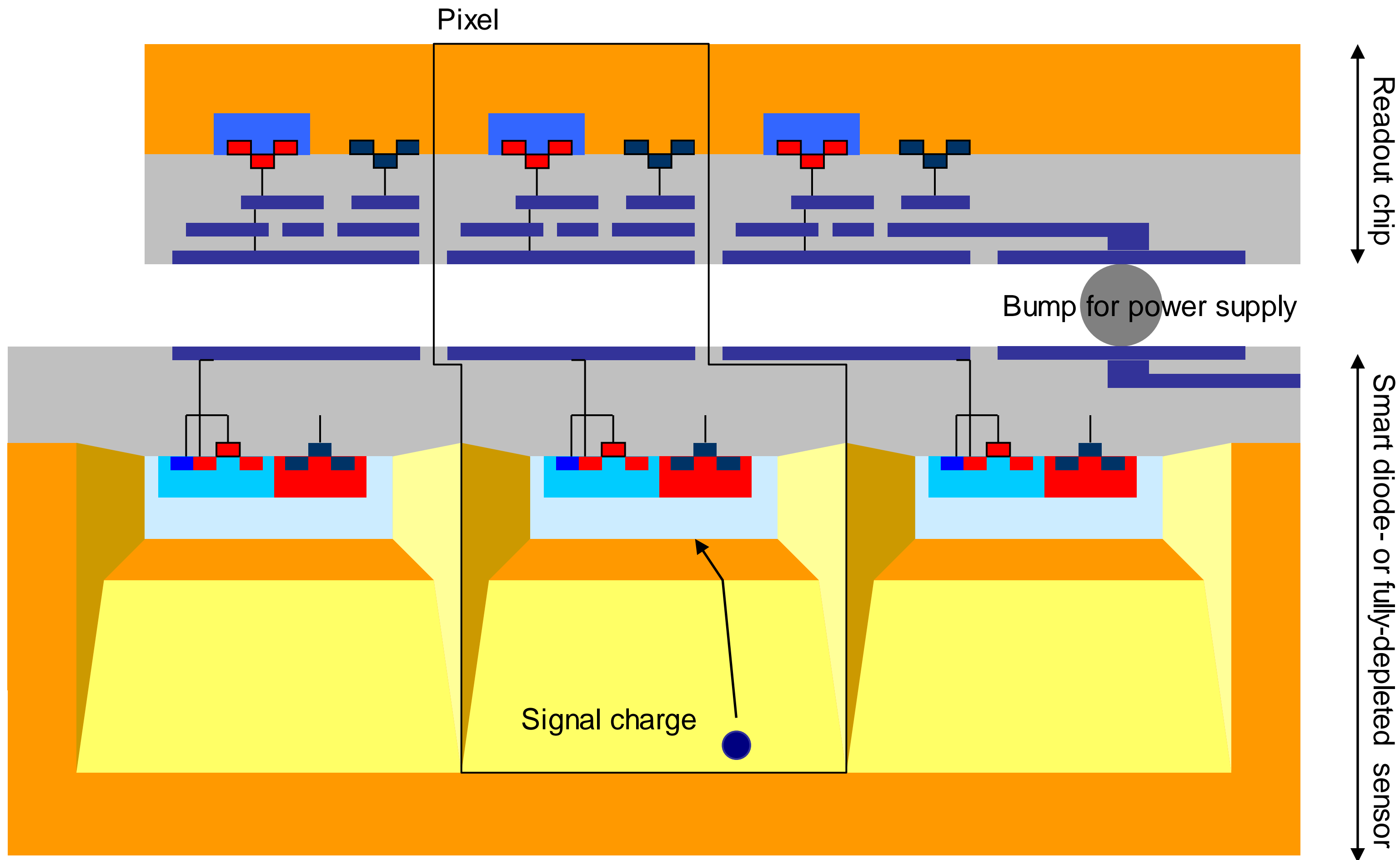
Thank you

Backup Slides


IO pads for strip operation
Column control
12x2
Matrix
Cap. Injection
SFOut
Test Pad
20x3
Column control
Strip Pads
Bias DACs
IO pads for CCPD operation



Column control SR
Strip bus
R2
Bias A
L2
R1
Bias B
L1
R0
Bias C
L0
R2
L2
R1
L1
R0
L0
Pad
Pad
3
SelectL=0
SelectR=0
3
Row control SR
Mon Pad
33um
125um



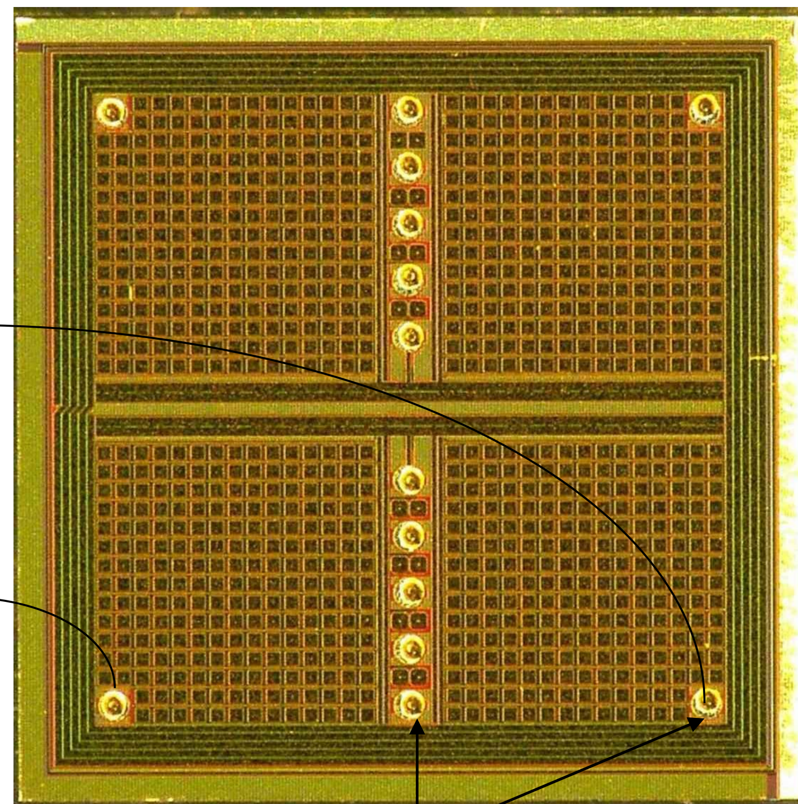
The sensor and readout chips are flipped and connected by a few bumps

Advantage – no need to wire-bond both chips

Power and signals for ROC provided by sensor chip

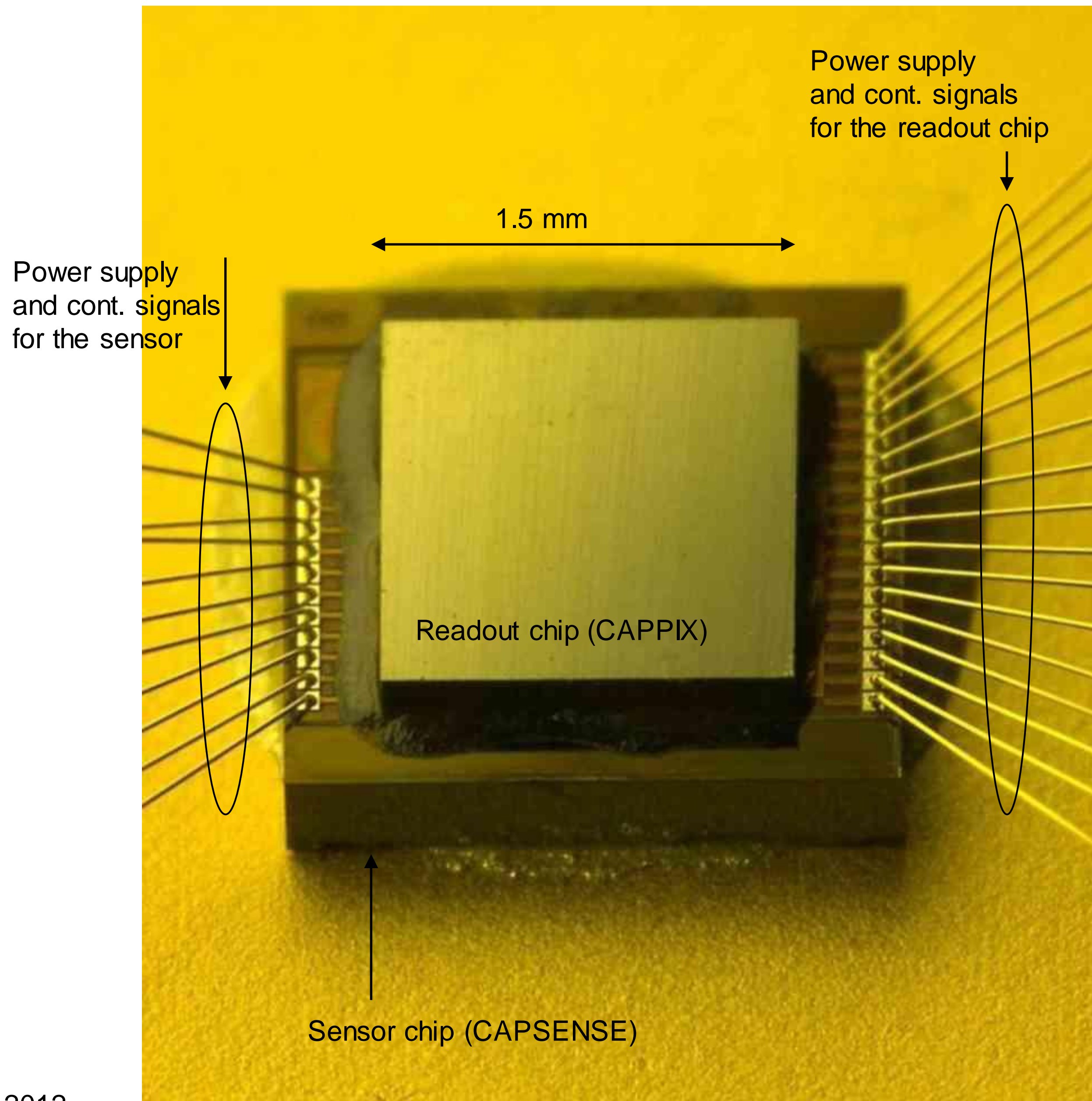
Edgeless sensor covered with many small ROCs can be made

CCPD2 – photographs of the chips

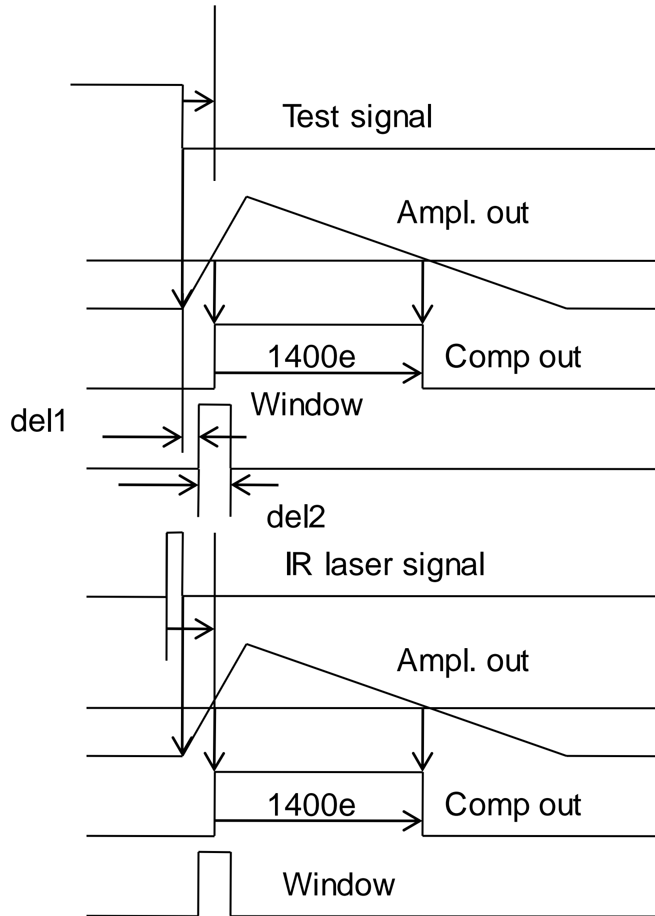


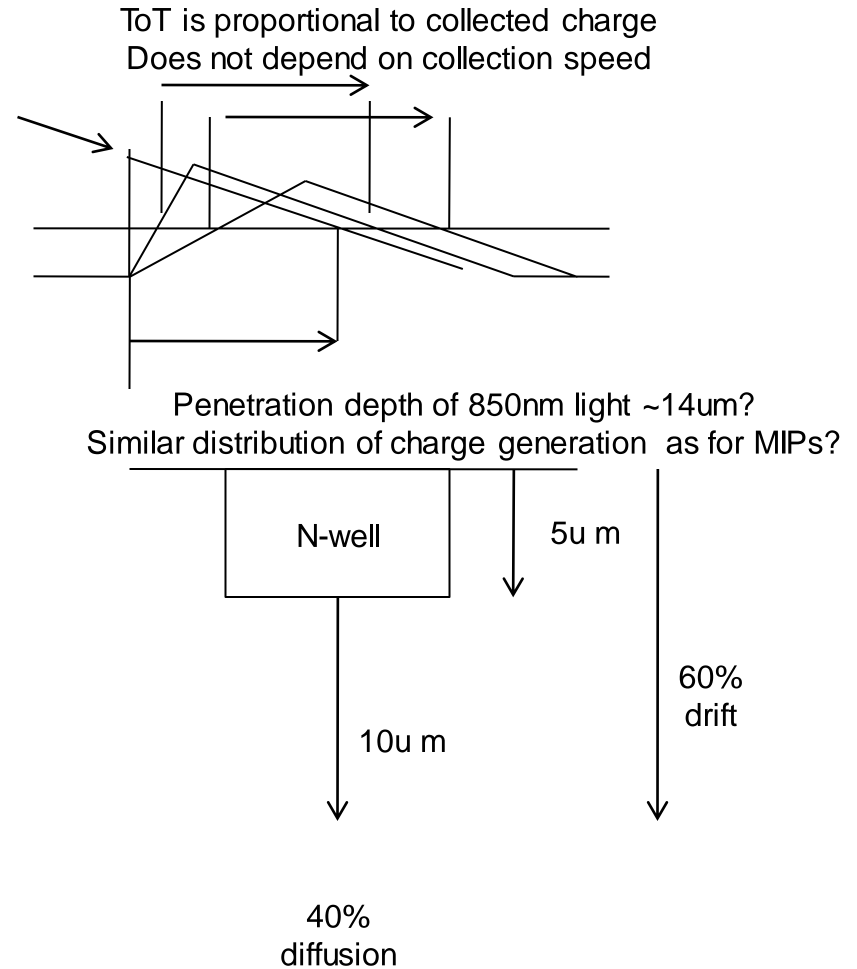
CAPPIX

Power and signal bumps


Power supply
and cont. signals
for the readout chip
1.5 mm
Power supply
and cont. signals
for the sensor
Readout chip (CAPPIX)
Sensor chip (CAPSENSE)

- Digital part





- Digital part