# Wireless Transfer:

# Multi-Gigabit Wireless data transfer at 60 GHz

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# OUTLINE

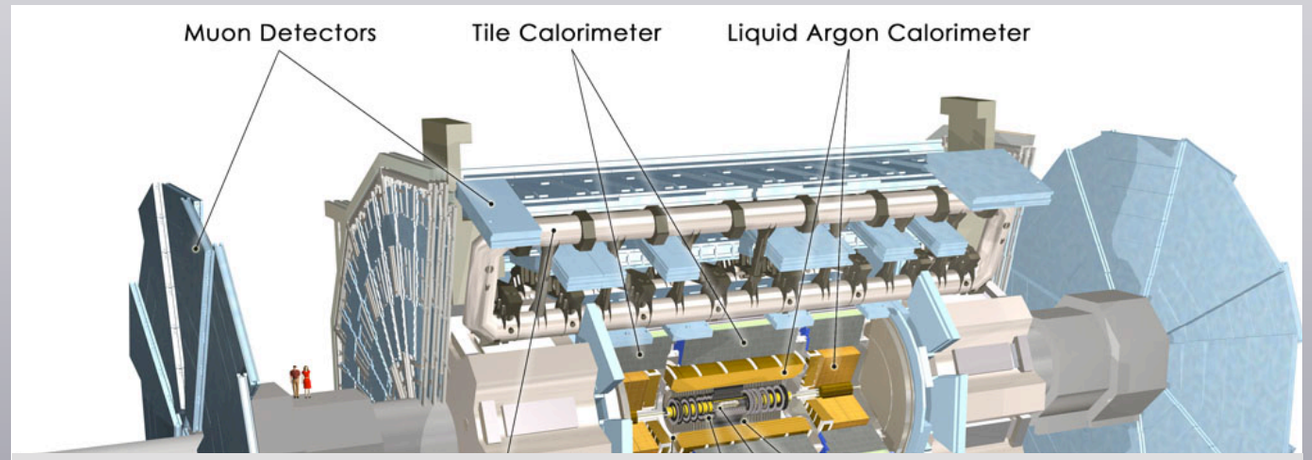
- **Motivation**
  - **Needs for wire-less in HEP (ATLAS@LHC)**
  - **Introduction of MilliMeter-Wave (MM-Wave)**
- **Proposed *60 GHz Transceiver System***
  - **Conceptual design**
  - **Simulation results**
- ***3-D* Opportunities**
- **Conclusions**

# Motivation

- The ATLAS and CMS experiments@LHC consists of several million channels
- Data Transfer rate is today limited by the available:
  - ***Bandwidth***

  limited by

  - ***Power budget (Gbps/W)***
  - ***Mass (Gbps/g)***
  - ***Space (Gbps/cm²)***




LHC detectors:

- $10^6$ to $10^8$ channels
- 50 kHz to 1 MHz readout rate
- Trigger system limited by readout bandwidth
- of (Tb/s) needed

***Example: Innermost silicon layer:***

- Required bandwidth is *50-100Tb/s*
- Detector divided into *20-50K* independent segments
- Required bandwidth per link is then *5 Gb/s*

***Wireless Multi-GigaBit/s readout ?***

# Motivation cont.

## *Use of the MilliMeter Wave (MM-Wave) technology at 60 GHz*

***Offers*:**

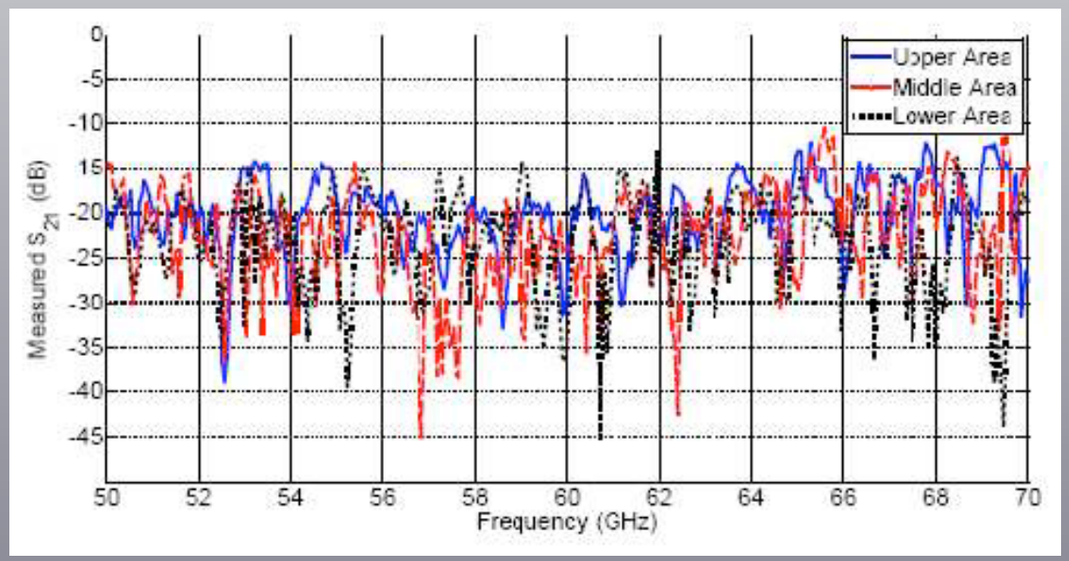
- Wireless ***unlicensed spectrum of 7-9 GHz bandwidth*** available world-wide
- Able to send ***Gigabits/s*** (***5-10 Gbps***) of information over short distances (10 m)
- High transmit power: ***40 dBm EIRP*** (Effective Isotropic Radiated Power)
- Largely unused today: ***low interference probability***
- ***60 GHz*** does not penetrate (walls, silicon, etc): ***security***
- Flexibility of placement
- Small form factor
- Allows for integration of antenna(s)

***How do we read it out?***

# Wireless readout architecture?

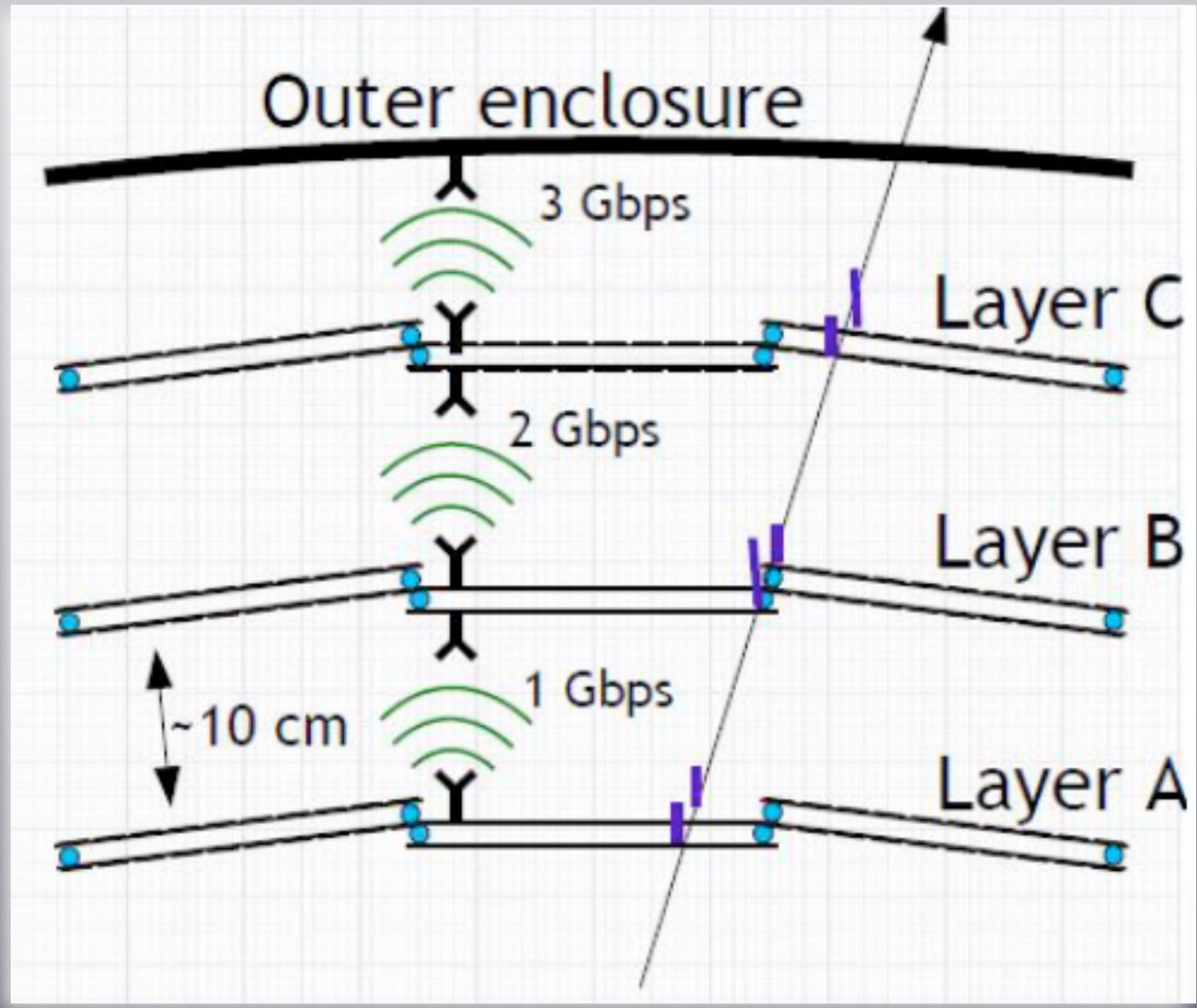
Readout path (ideally) along particle path:
- Helps Track Trigger!

- *60 GHz* signal cannot penetrate through the silicon layers




- *Solution*: Send the data through the Silicon layers by a wire/vias connection, with an antenna on both sides.

R. Brenner@Wuppertal 2011



# Proposed 60 GHz Transceiver System

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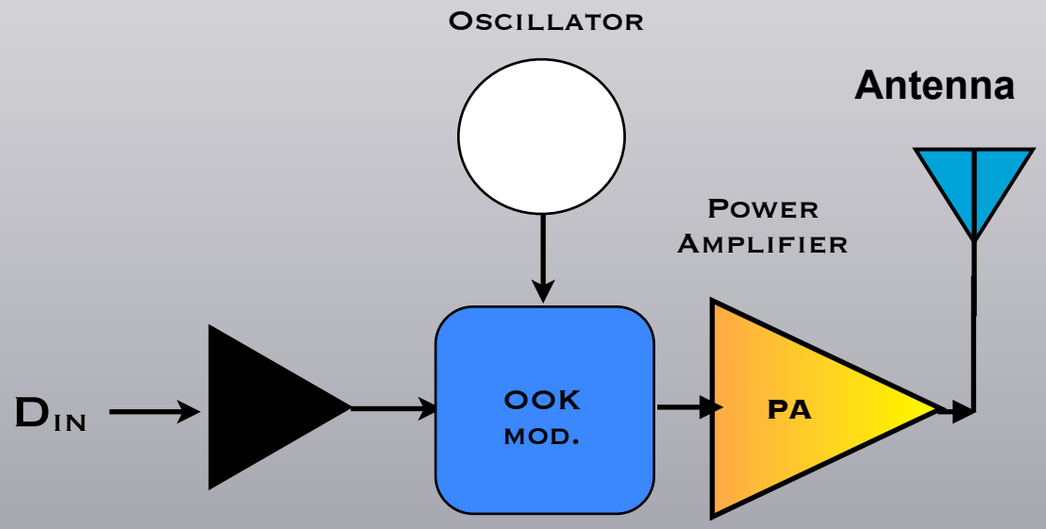
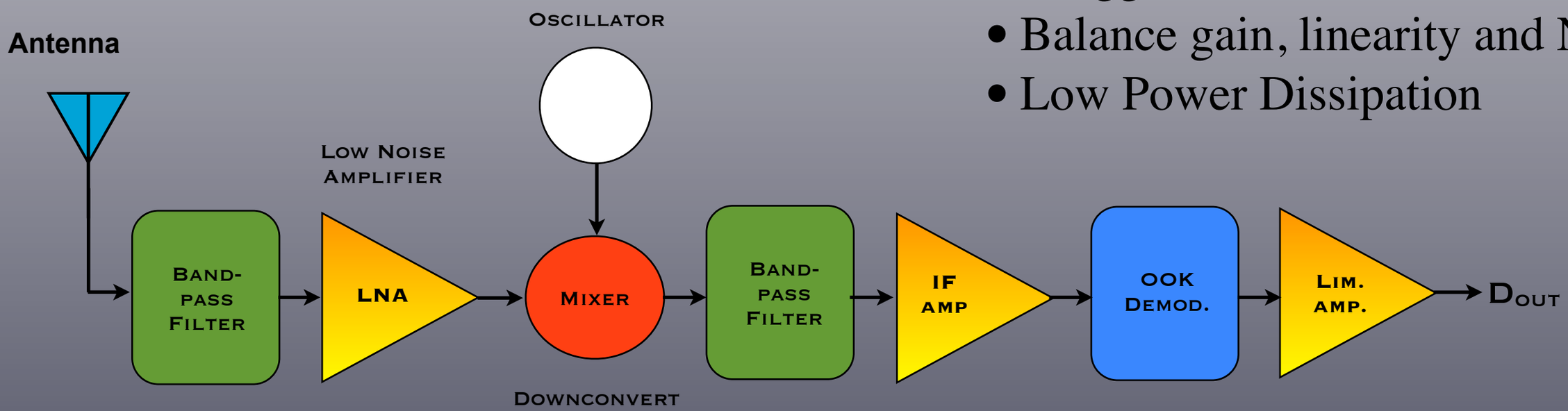



**Transmitter:**

- Deliver necessary output power
  - High power efficiency
  - High gain and stability

**Receiver:**

- Need aggressive LNA
  - Balance gain, linearity and NF
  - Low Power Dissipation



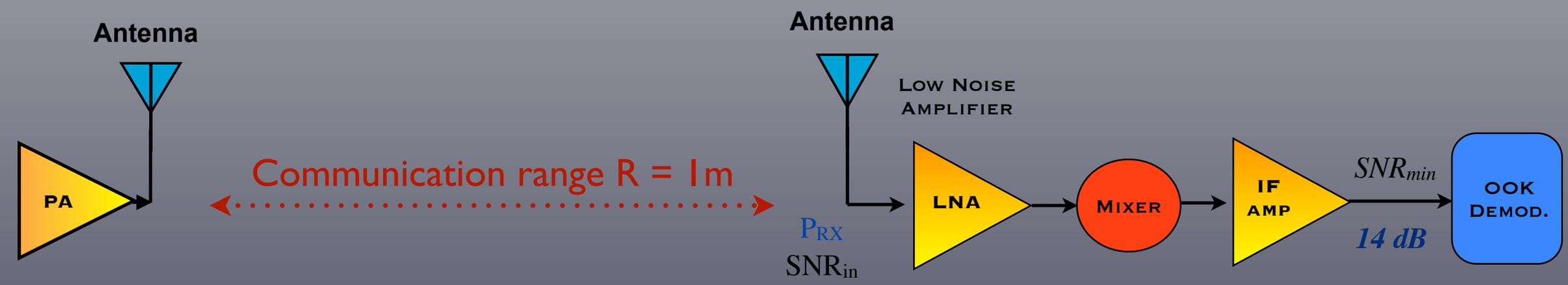
# Link-budget

Required Bit-Error-Rate (BER): **$10^{-12}$**

OOK Modulation: $(E_b/N_0)$ = **17 dB** ⟶ $SNR_{\min} = \left(\frac{E_b}{N_0}\right) \cdot \frac{R}{BW} = 14dB$

$$P_{RX} = SNR_{\min} \cdot N_0 \cdot BW \cdot F = -56dBm$$

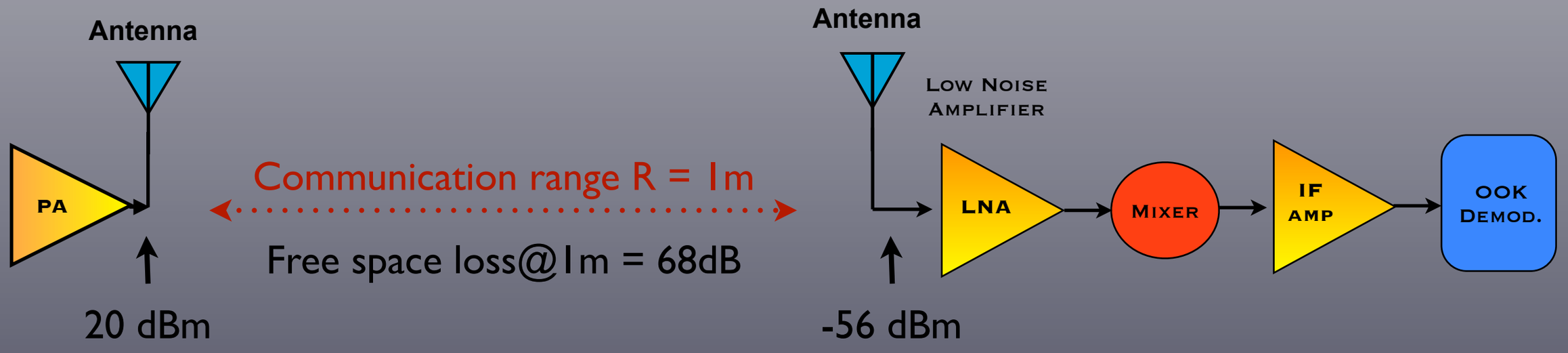
- $E_b/N_0$: Energy per bit to noise power spectral density
- $R$: Data bit rate
- $BW$: Bandwidth
- F: Noise Figure
- $P_{RX}$: Receiver sensitivity



# Link-budget cont.

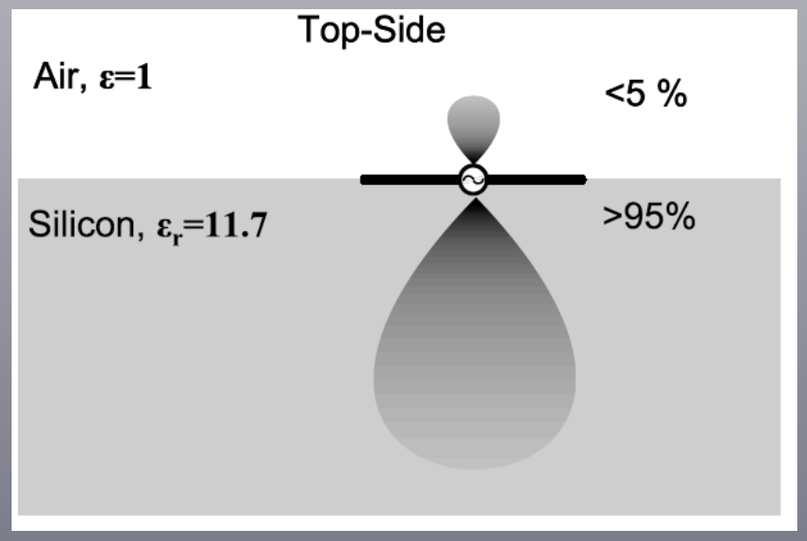
$$P_{TX} = P_{RX} - G_{TX} - G_{RX} + L_{TX} + PL(R) + L_{RX} + FM$$

$P_{TX}$ = Transmitted output power (dBm)
$P_{RX}$ = Required Power (-56 dBm)
$G_{TX}$ = Transmitter antenna gain (8 dBi)
$G_{RX}$ = receiver antenna gain (8 dBi)
$L_{TX}$ = Transmitter losses (connections, other losses) (2 dB)
$L_{RX}$ = Receiver losses (connections, other losses) (2 dB)
FM = Fading Margin (20 dBm)
$PL(R)$ = Free space loss = $20\log\frac{4\pi R}{\lambda}[dB] = 68\ dB@1\text{m}, 28\ \text{dB}@10\ \text{cm}$



# Key Challenges for MM-Wave Design

- Lossy/conductive substrate → poor isolation and lower Q components
  - LNA and VCO challenging
- High dielectric constant $\varepsilon_r$=11.7
  - For on-chip antenna: Most of the electromagnetic energy would be drawn into the substrate




- Difficult to deliver high output power (low supply and break-down voltage).
  - PA challenging

# SiGe HBT BiCMOS versus CMOS

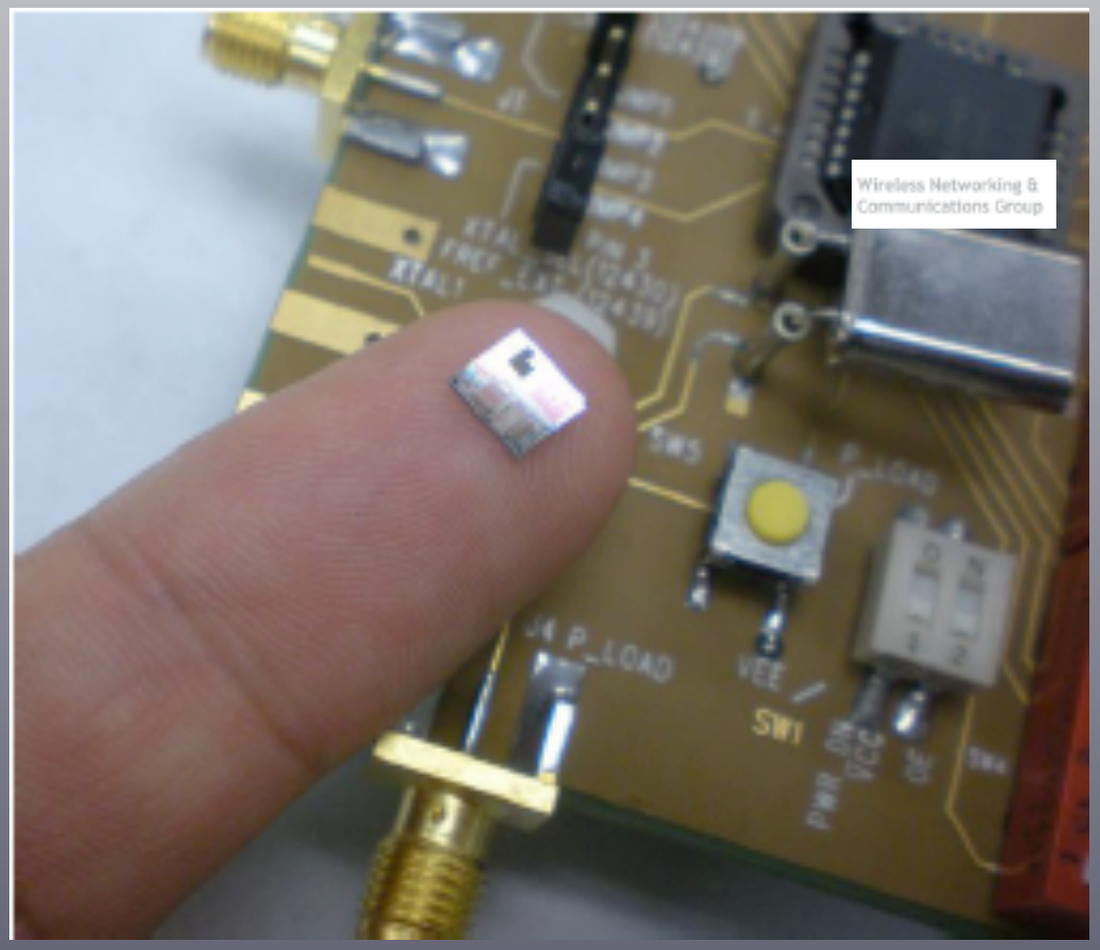
- For equal performance, SiGe requires less aggressive lit.(2gen.)
- SiGe has Higher Breakdown Voltage at fixed performance
- SiGe has much larger gm/um$^2$ (need big MOSFETs for high $f_{max}$)
- SiGe has much lower 1/f Noise
- Modeling of SiGe HBTs is easier for high frequency design (first time pass)
- Matching of the bipolar devices is superior compared to the CMOS devices
- Radiation hardness?

***SiGe BiCMOS technology combines both high speed HBTs with relatively high breakdown voltage and standard CMOS transistors allowing a very high integration level***

# Why ON-Chip Antennas?

- MM-Wave signals have small wavelengths at 60 GHz (5 mm)
  - Possible to integrate receive and transmit antenna(s) on chip.
- Multiple metal layers on ICs available
  - Can be used to fabricate MM-wave antennas.
- Eliminate cable/connectors loss
- No need for ESD
- Reduces integration cost

**Contains two antennas**
**5*5 mm²**



# Low Noise Amplifier

- Large gain to reduce $NF_{tot}$
- Reduced Noise Figure $NF_{min}$
- Handle large signals without distortion
- Input, output impedance matching
- Isolation between input and output
- Low power consumption

$$NF_{tot} = NF_{LNA} + \frac{NF_{other} - 1}{G_{LNA}} .....$$

## Design metrics

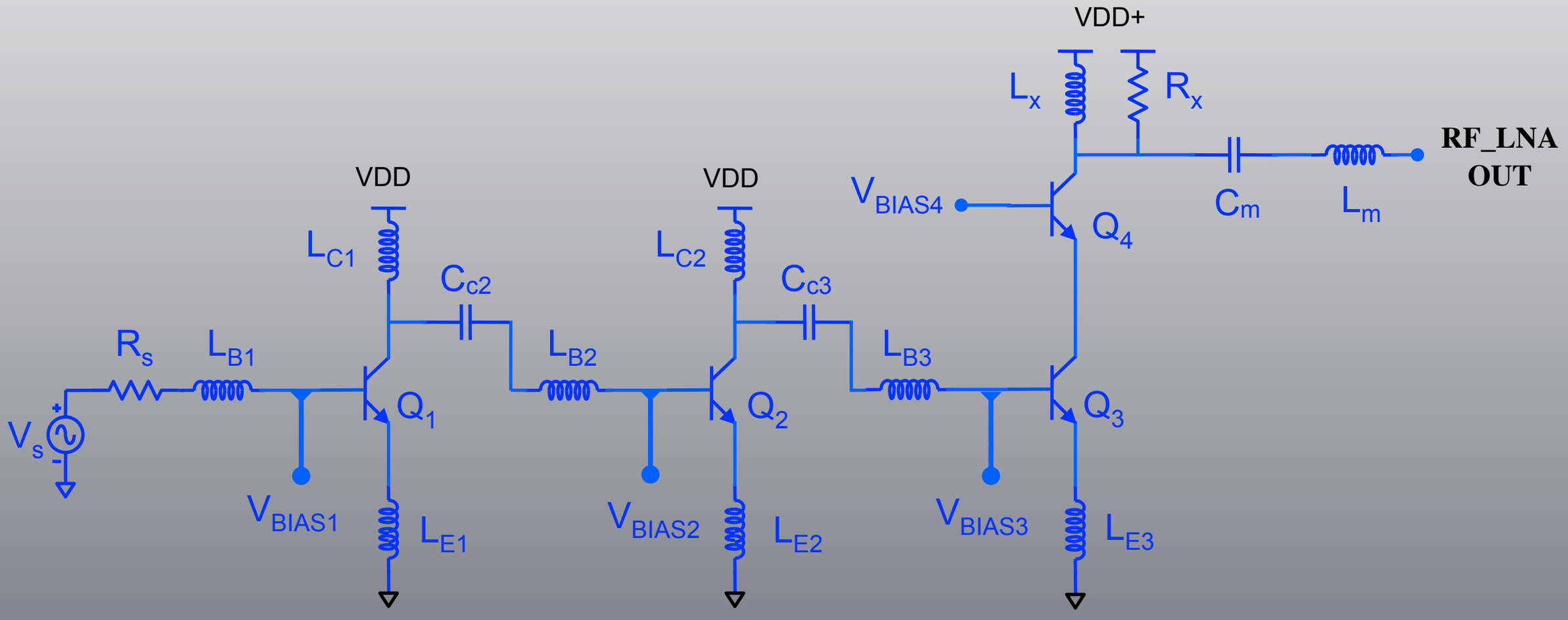
| | |
|---|---|
| Gain $S_{21}$ | 20 dB |
| NF | 5 dB |
| $P_{1dB}$ | 20 dBm |
| Reverse Isolation ($S_{12}$) | -60 dB |
| Supply Voltage | 1.2-1.5 V |
| Power dissipation | 10 mW |
| Input/output Impedance | 50 Ω |

# LNA Circuit

Noise

Gain

Gain

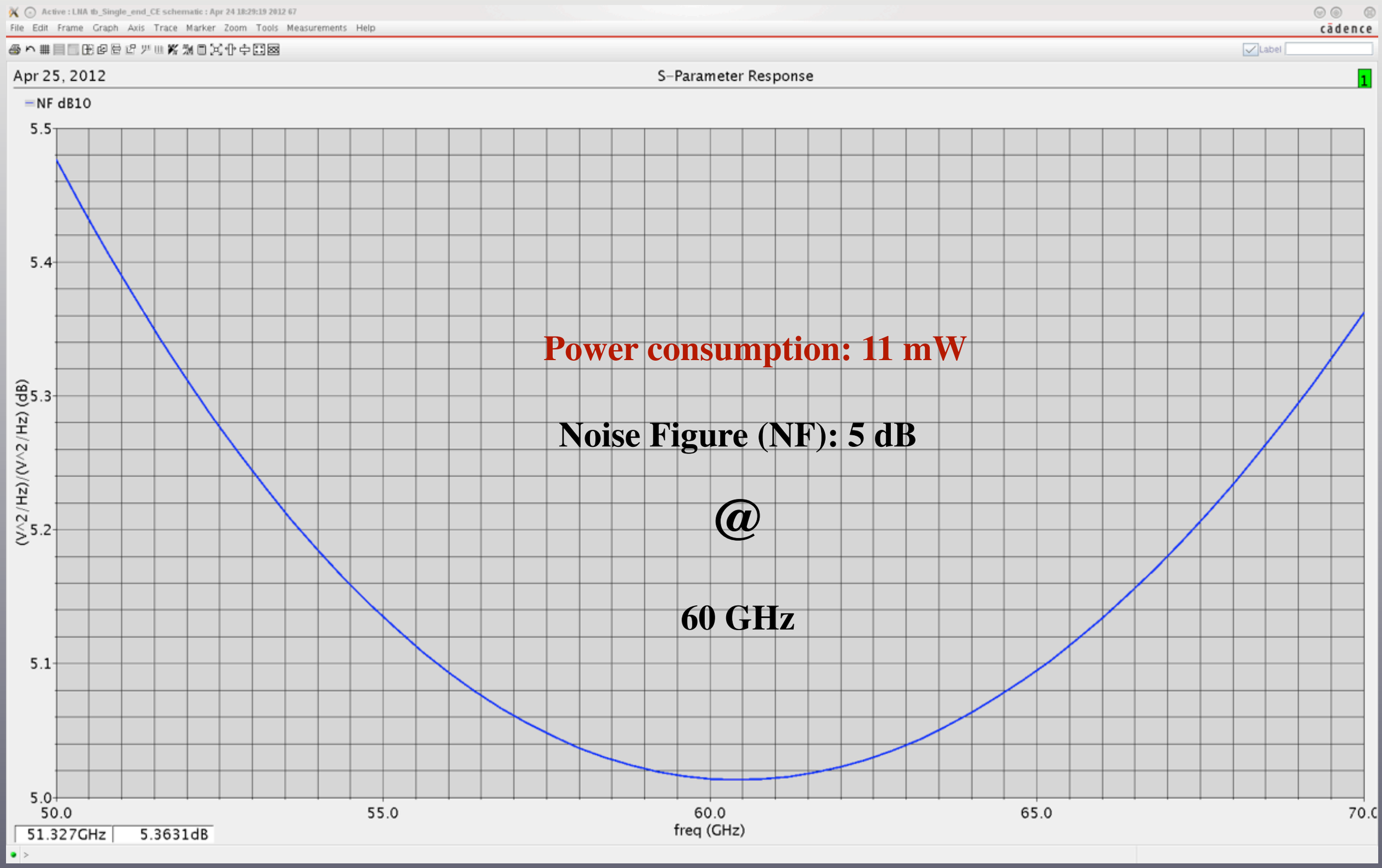



**Common-Emitter Stage**

**Common-Emitter Stage**

**Cascode Stage**

# LNA Simulations




**Power consumption: 11 mW**

**Noise Figure (NF): 5 dB**

**@**

**60 GHz**

# LNA Simulations

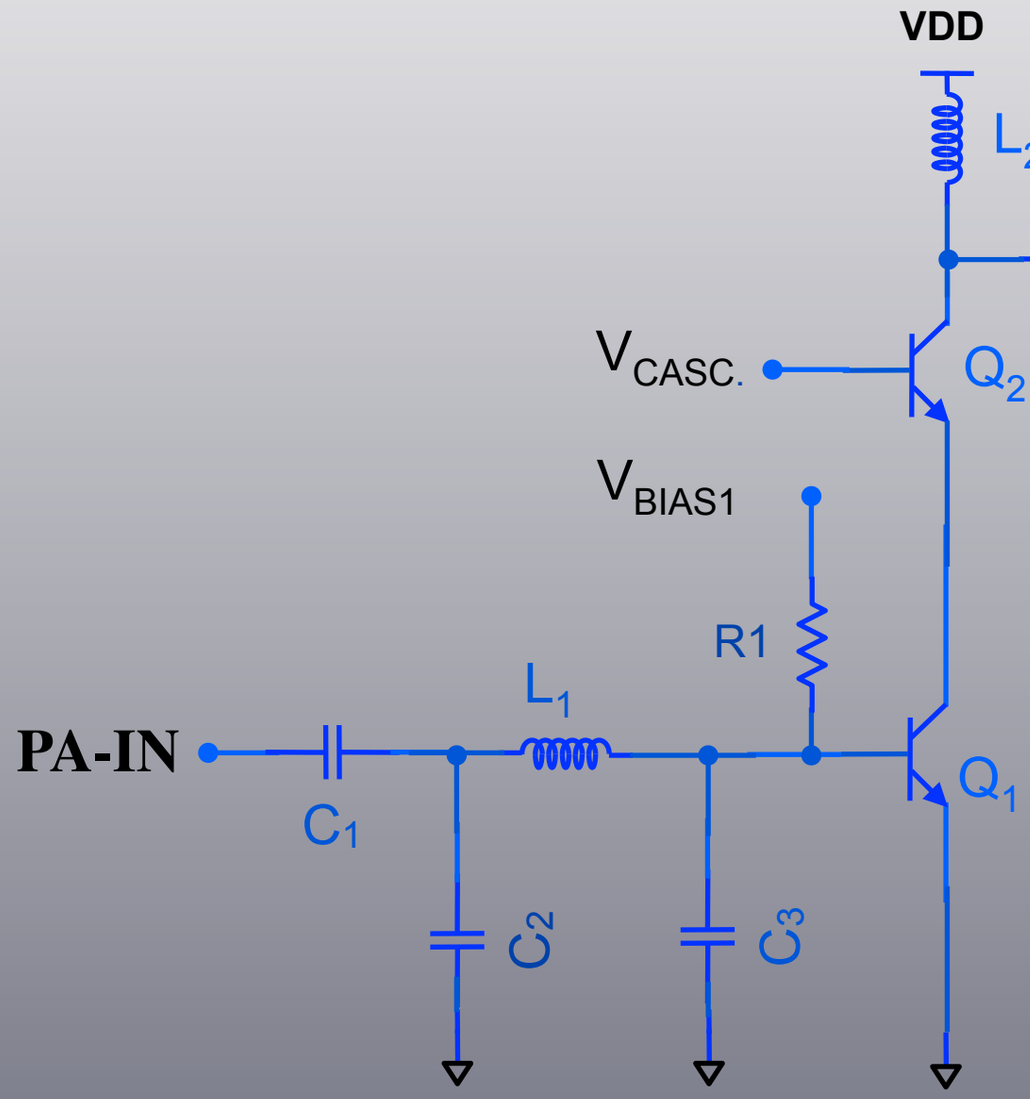
# Power Amplifier

- Last amplifying stage in the transmitter chain
- Drive the Antenna(s)
- **Output power**
- **Efficiency**
- **Linearity**
- **PAE (Power added Efficiency)**
- **Power gain**

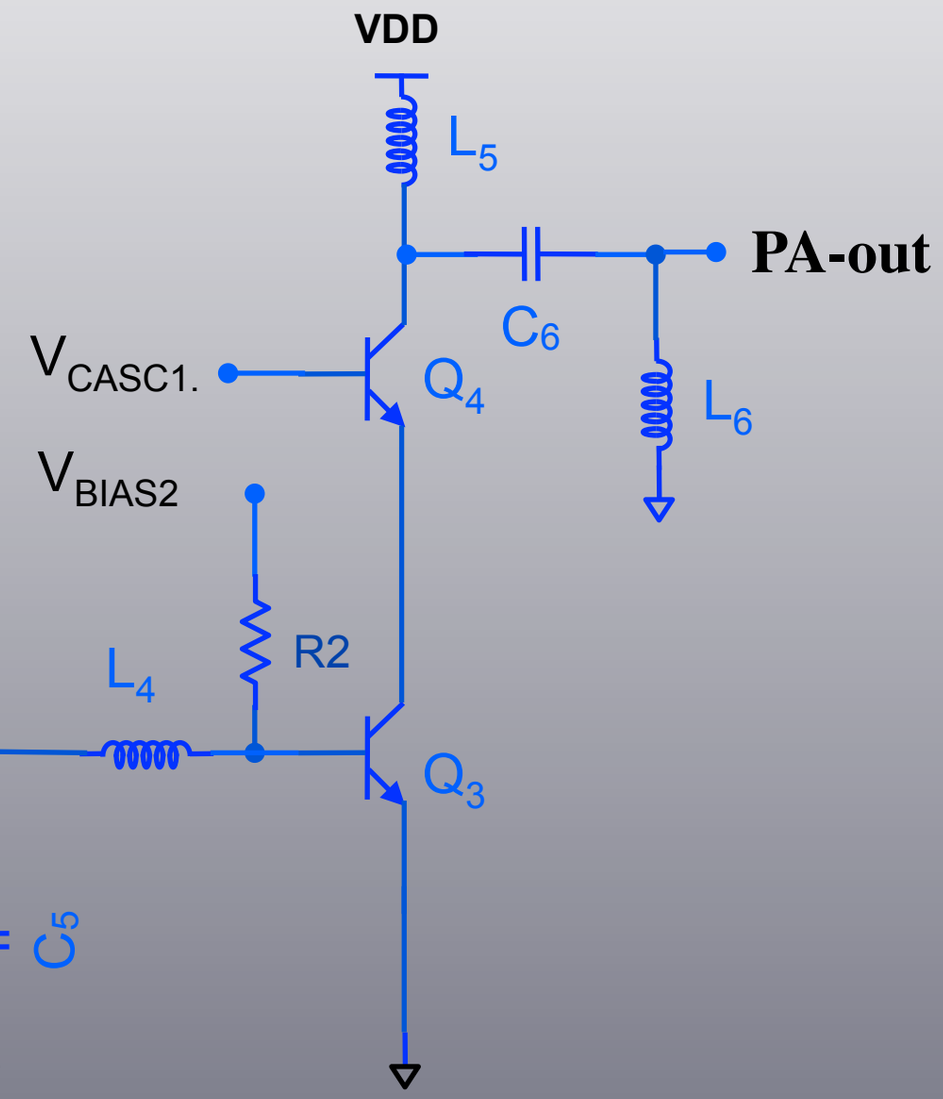
| | |
|---|---|
| Output Power | 20 dBm |
| Power Efficiency | 20% |
| Gain | 30 dB |

- Class of operation: AB
  - Trade-off between good linearity and good efficiency

# 2-Stage PA



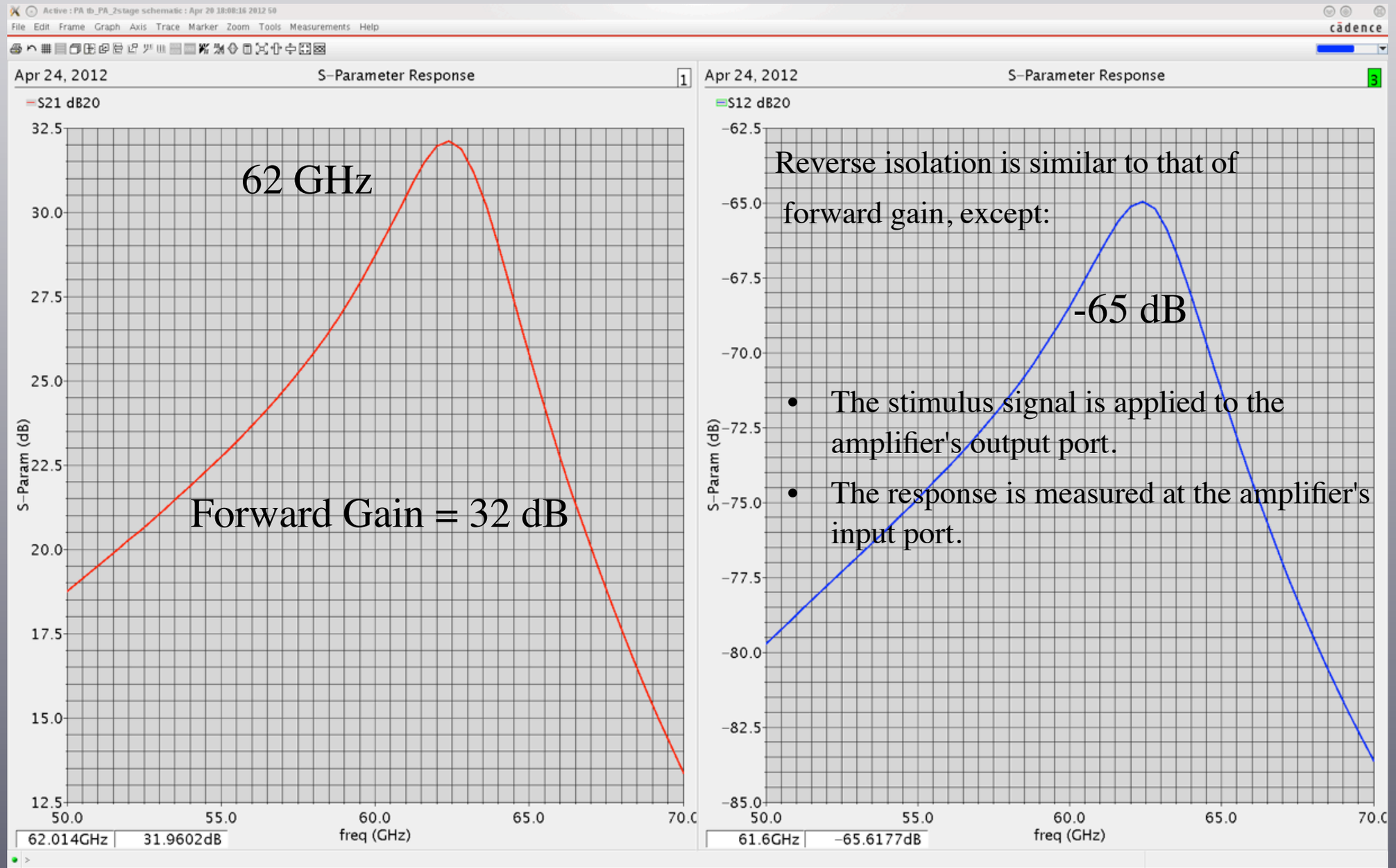

Cascode stage 1




Cascode stage 2

# Power Amplifier

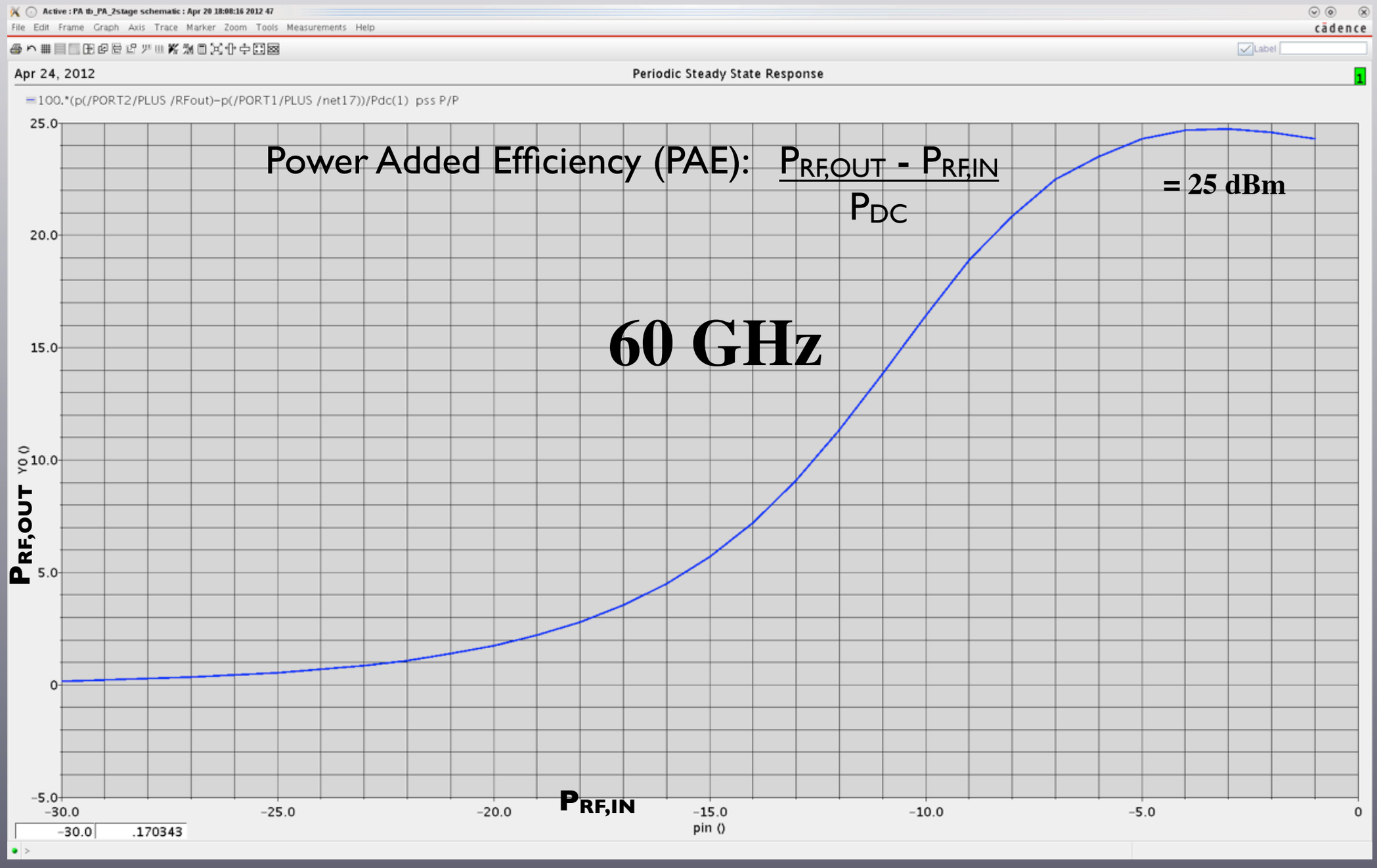
## Simulations




- The stimulus signal is applied to the amplifier's output port.
- The response is measured at the amplifier's input port.

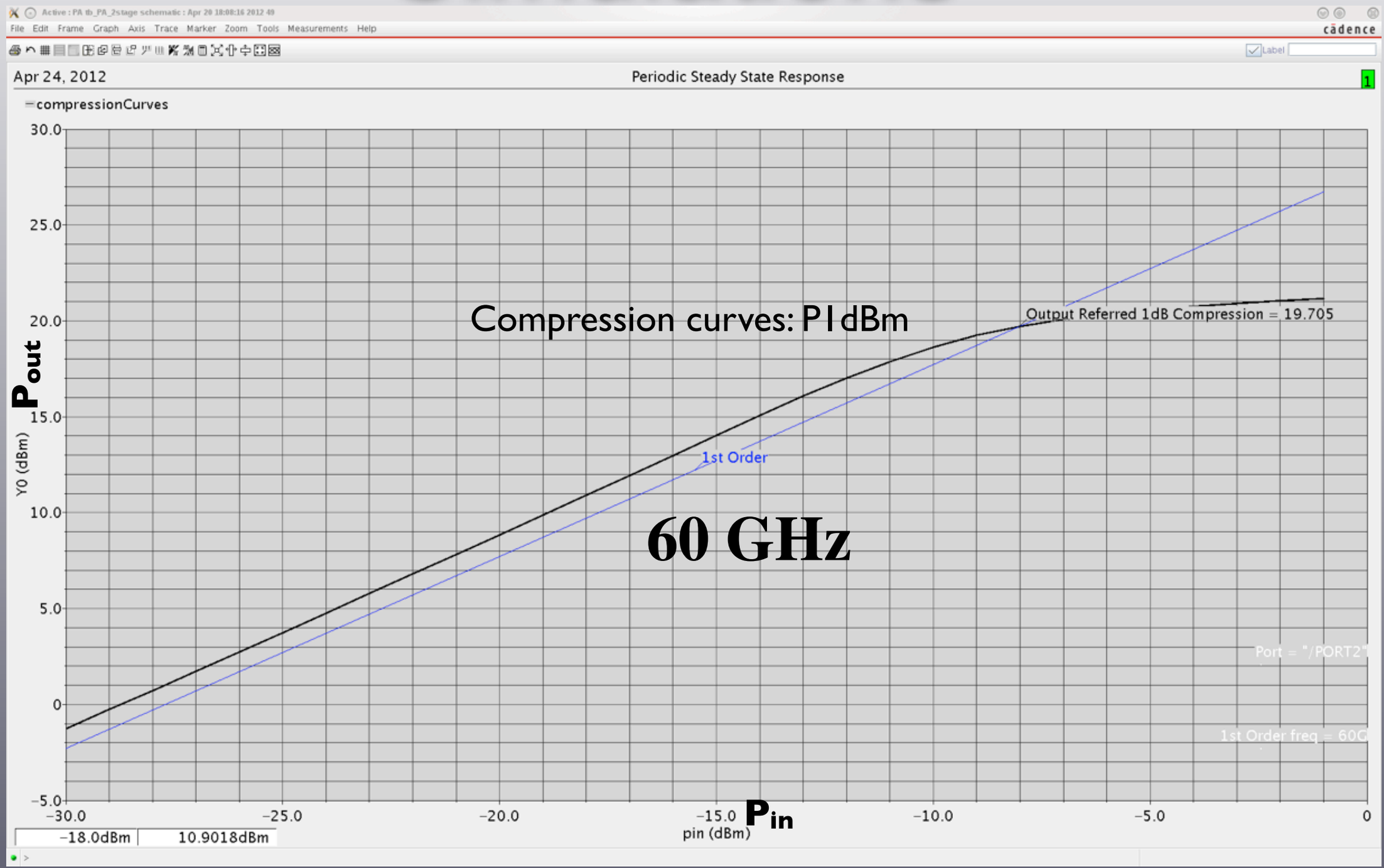
# Power Amplifier

## Simulations

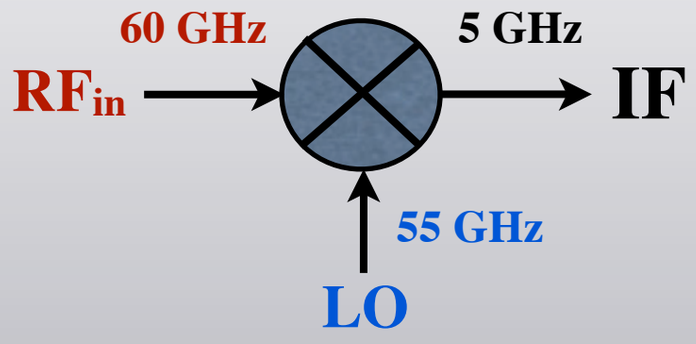


# Power Amplifier

## Simulations



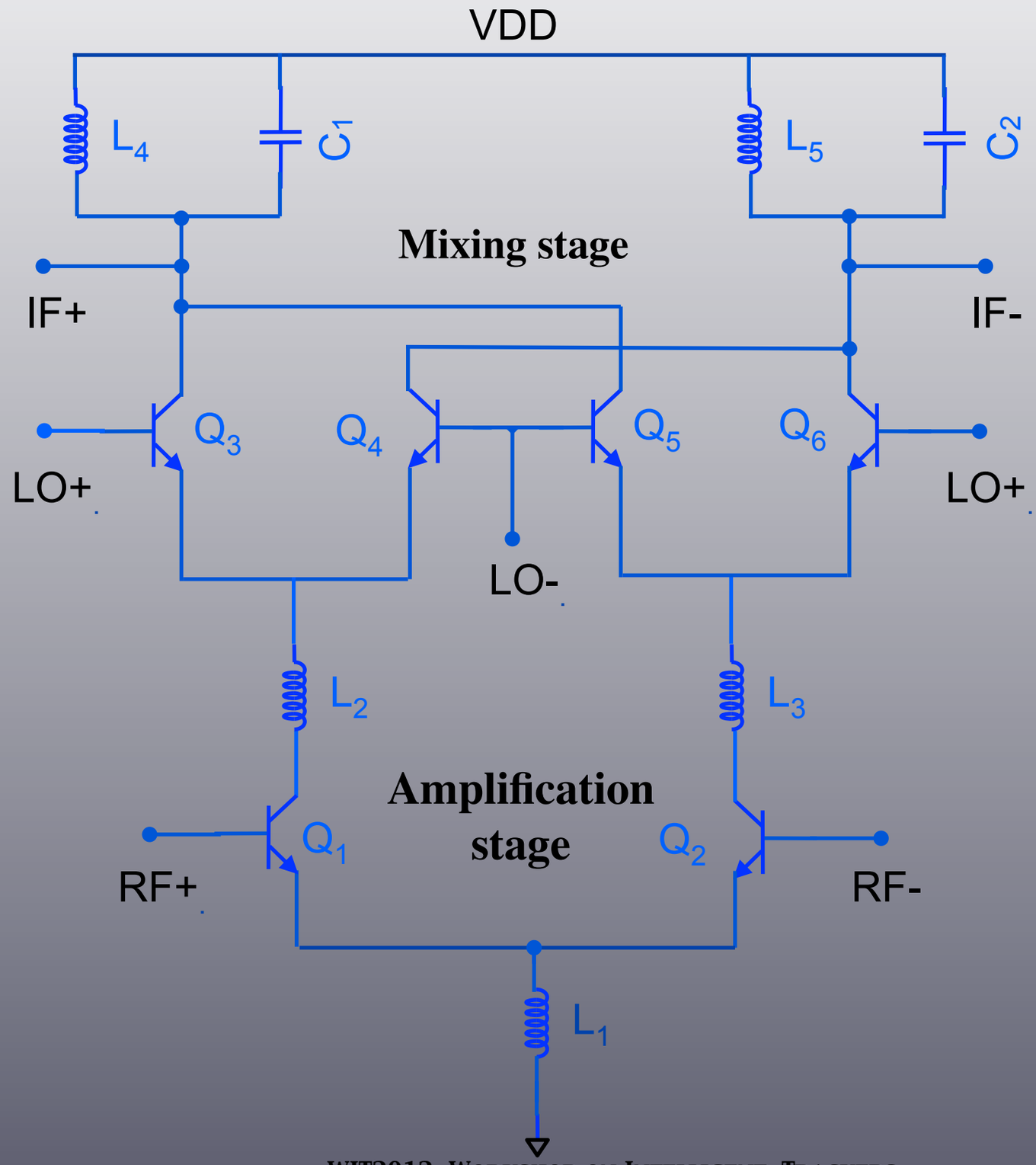
# MIXER Stage




## Metrics

- *Noise Figure*
- *Linearity*
- *Isolation*
- *Conversion gain*

- **Gilbert Cell structure**
  - Very good Isolation
  - Differential structure
    - Complete port-to-port isolation



# Voltage Controlled Oscillator

**Leeson's equation**

$$L_{PM} = 10\log\left[\frac{FkT}{A}\frac{1}{8Q_L^2}\left(\frac{f_o}{f_m}\right)^2\right]$$

**Where:**

$L_{PM}$ = Single Side Band, Phase Noise density [dBc/Hz]

$A$ = LO output power

$F$ = Noise Factor at operating power level

$k$ = Boltzmann's constant $1.38*10^{-23}$ [J/K]

$T$ = Temperature [K]

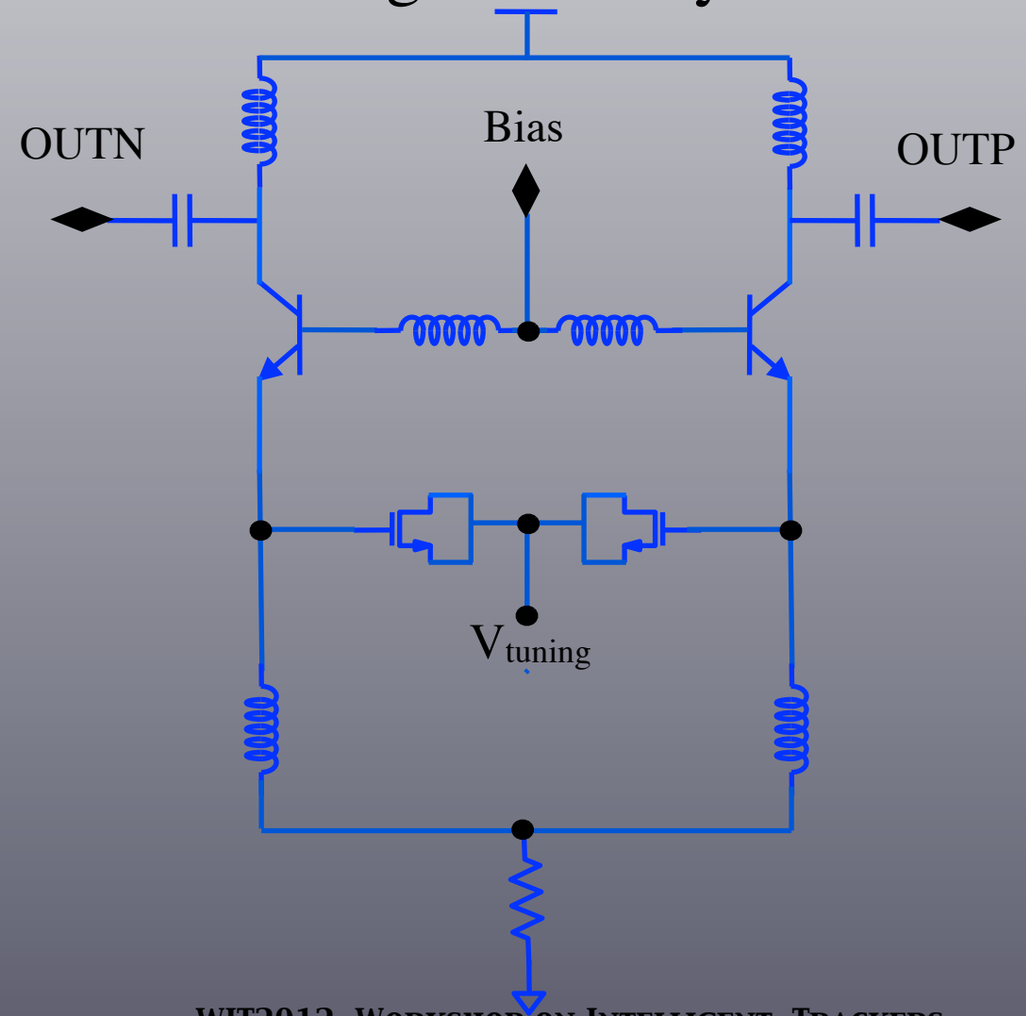
$Q_L$ = Loaded-Q [dimensionless]

$f_o$ = Oscillator carrier frequency [Hz]

$f_m$ = Frequency offset from the carrier [Hz]

**VCO metrics:**

- Accuracy of oscillation
- Phase noise
- Tuning sensitivity and linearity



# Modulation

Method used to convert analog or digital information to signals at RF frequency suitable for transmission.

**Modulation technique is a key consideration, since it determines:**

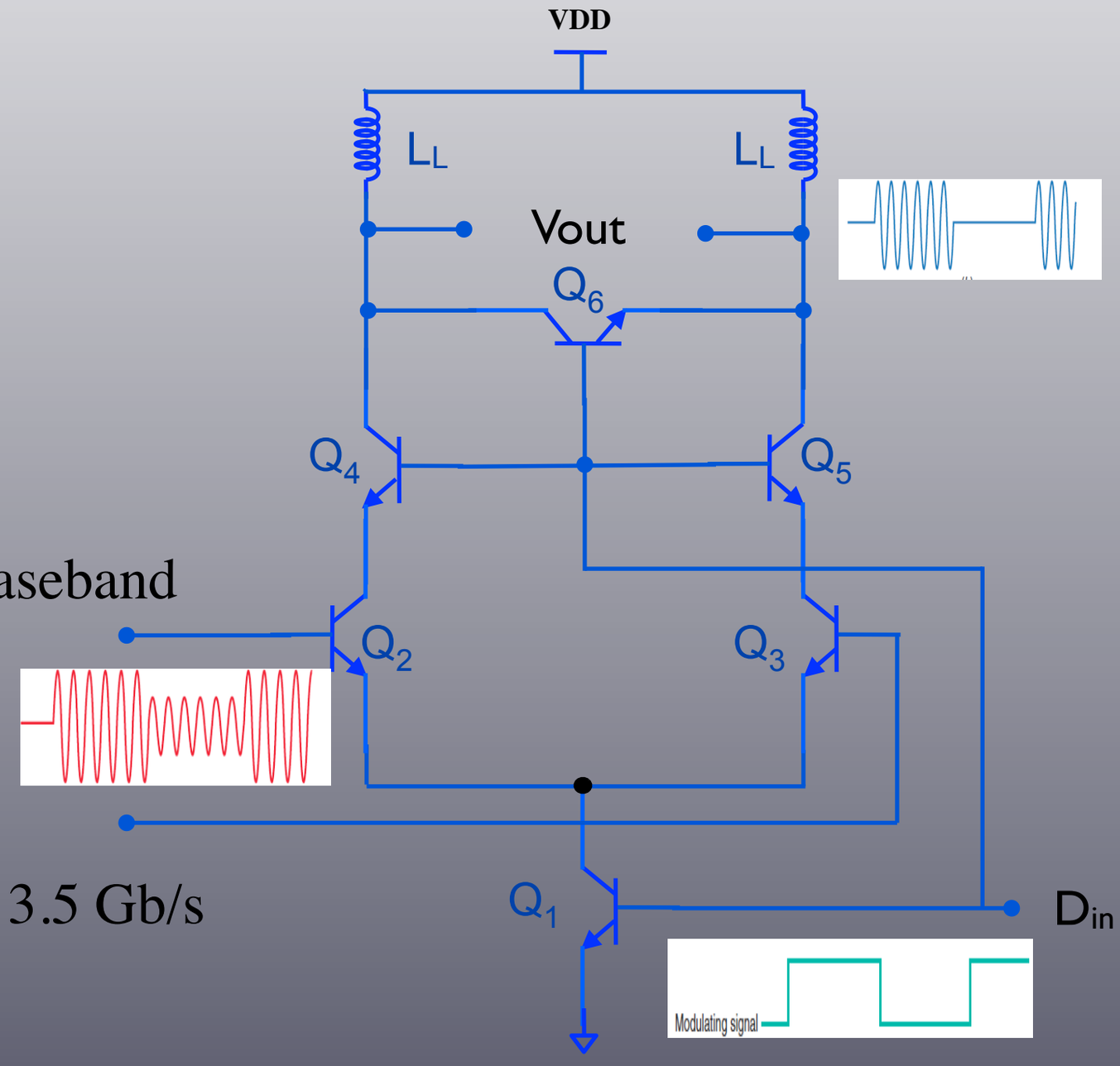
- System bandwidth
- Power efficiency
- Sensitivity
- Complexity

- OOK: On-Off Keying
- BPSK: Binary-phase shift key
- 8PSK: Phase Shift Key
- QAM: Quadrature Amplitude Modulation

| Modulation format | Theoretical bandwidth efficiency limits |
|---|---|
| OOK | 0.5 bit/second/Hz |
| BPSK | 1 bit/second/Hz |
| 8PSK | 2 bit/second/Hz |
| 16 QAM | 3 bit/second/Hz |

# On-Off Keying (OOK) Modulation

- Relatively Simple design
- Non-Coherent modulation
  - No phase reference
- Do not requirer linear PA
- Purely analog Modulator/Demodulator
  - Eliminates the digital interface and baseband circuitry
- Bandwidth efficiency (0.5 bits/s/Hz)
  - Maximum data rate would be around 3.5 Gb/s



# Current Timeline

**LNA**
**OOK**
**Mixer**
**VCO**
**PA**

→ **Started.**

**To be finished by the end January 2013**

**Amplifier Layout**

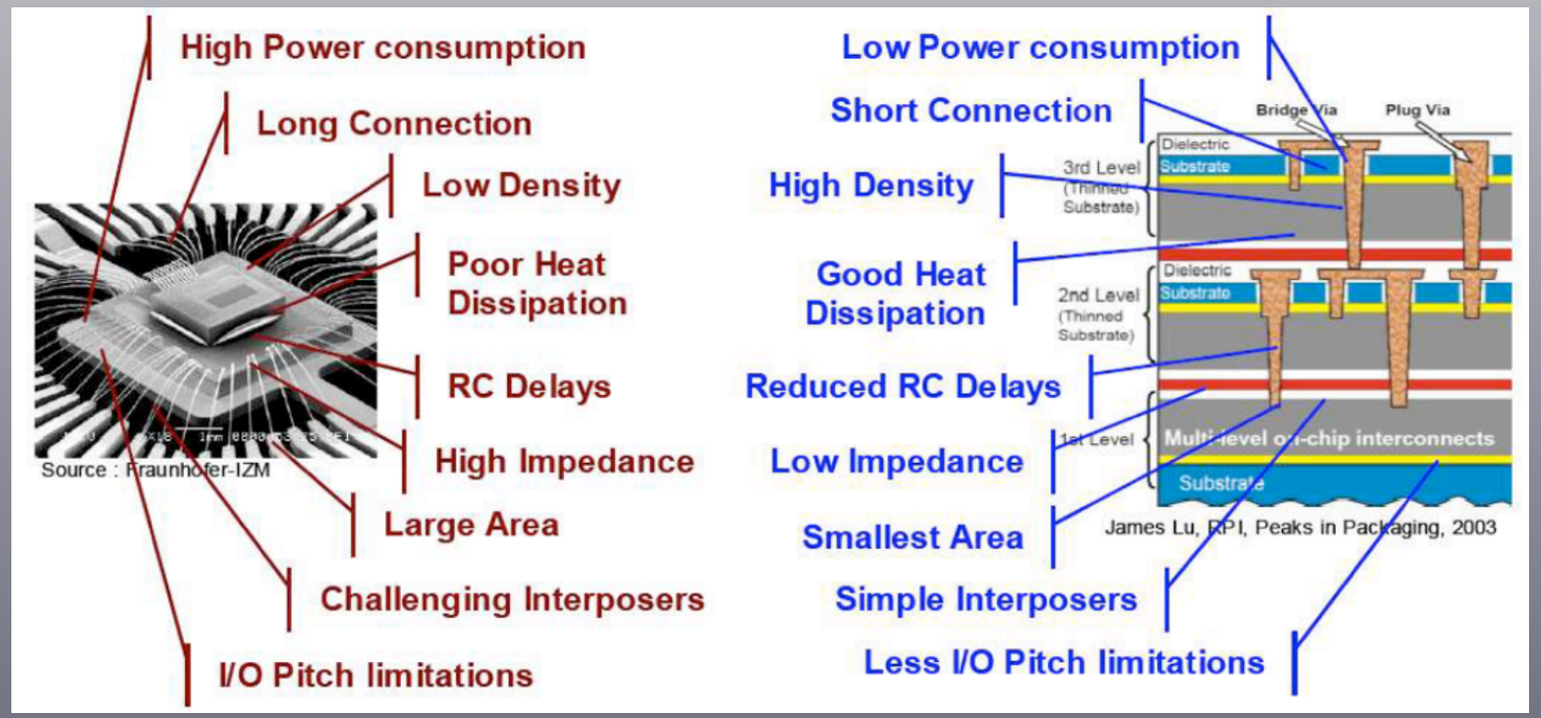
→ **Will Start February 2013**

***First prototype submission June 2013***

# 3-D Opportunities

# What are the Drivers for 3D integration

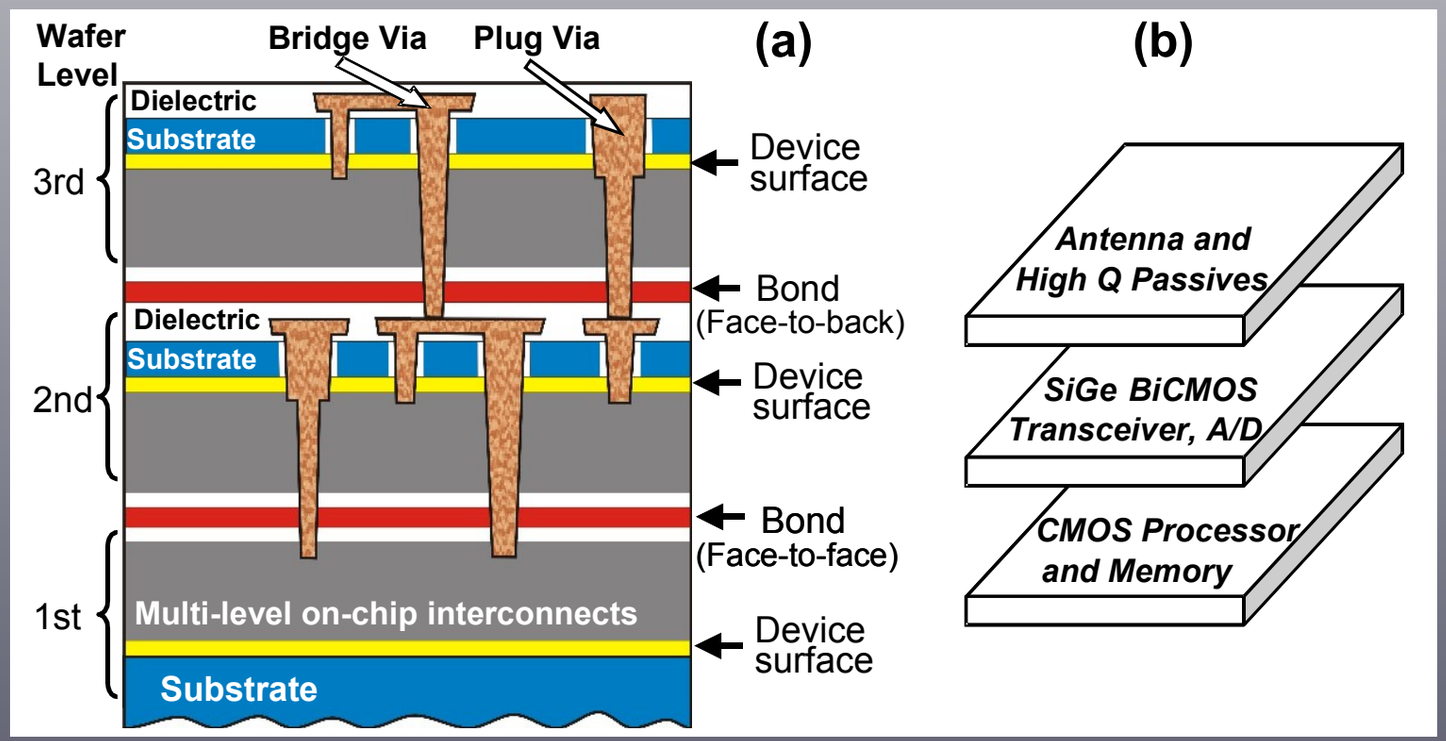
- **Better electrical performance**
- **Lower power consumption and noise**
  - Smaller wire-length will decrease the average load capacitance and resistance.
  - Lower wire to wire capacitance reduce noise coupling between signal lines.
- **Form factor improvement**
- **Lower cost**
- **More functionality**
- **Heterogeneous integration**




**Companies are now heavily involved in 3D development**

# 3D IC for HEP

- Move from horizontal 2-D chip layouts to 3-D chip stacking.
- Increased performance - Outscaling Moores's law(More than Moore).
- **Decreasing system risk.**
  - E.g. Stacking a 130 nm analog die with a 65 nm digital die, rather then trying to build a 65 nm mixed signal SOC.
- **Reducing cost: at some point, 3-D integration will be cheaper than shrinking further the 2-D design.**



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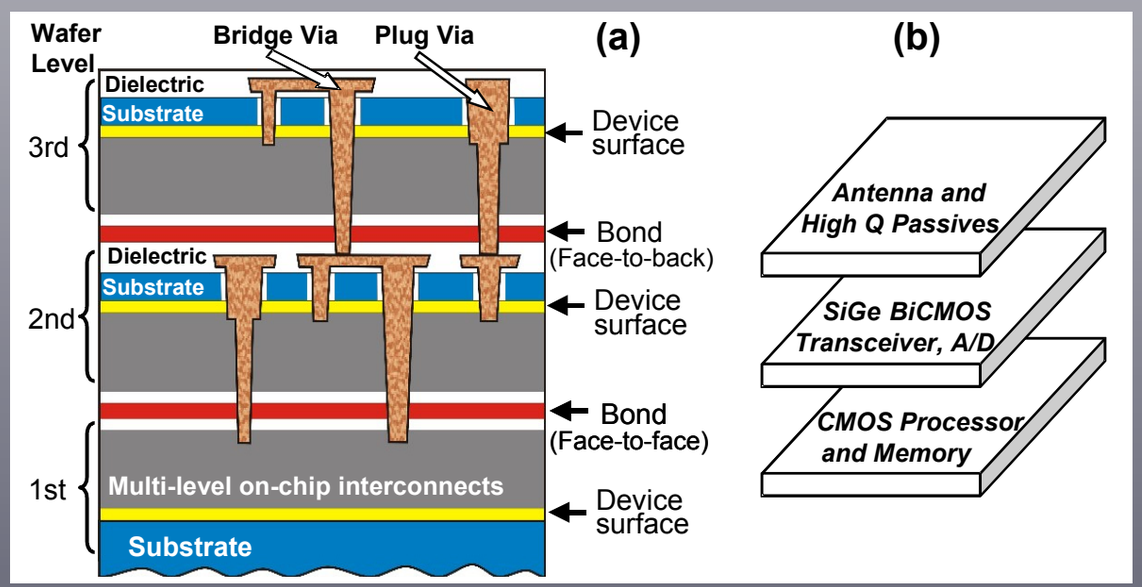
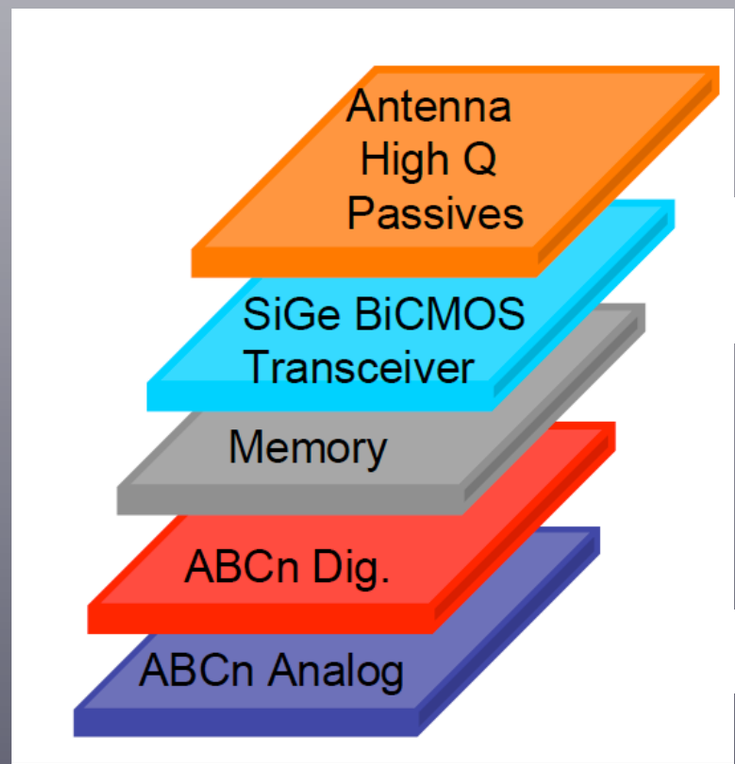


# Conclusions

- MM-wave technology presented as a possible solution for current bandwidth limitations of LHC experiments (ATLAS, CMS)
- A 60 GHz transceiver has been proposed
  - Schematic of some blocks shown
  - Simulations of some blocks shown
- SiGe BiCMOS (and CMOS) technology very well suited for 60 GHz wireless communication front-ends.

- There are several challenges to integration of MM-wave systems on a silicon substrate in spite of its numerous advantages

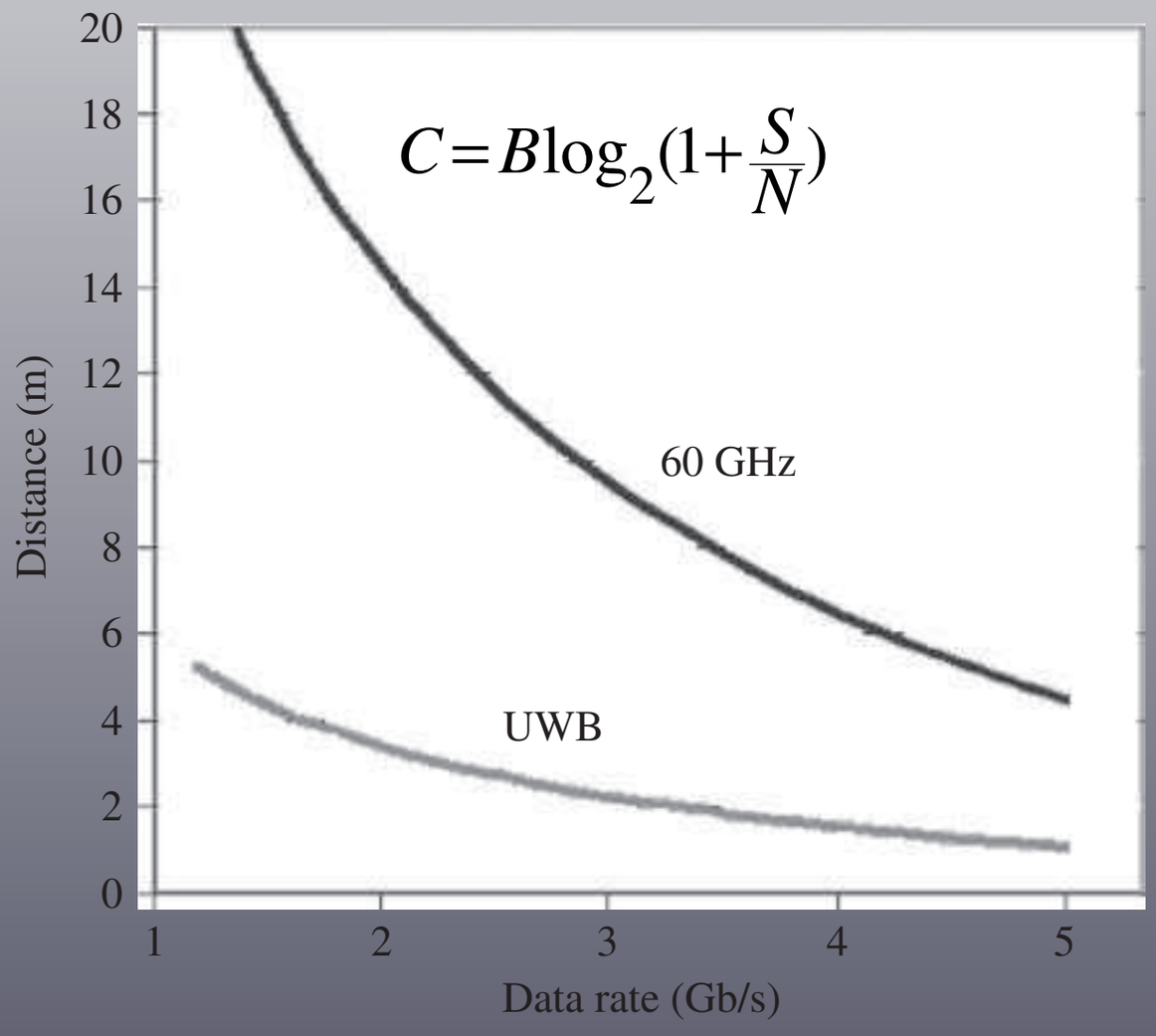
- 3-D integration opens up new possibilities for the near future that can potentially remove the drawbacks of the 2D solution.

# Backup

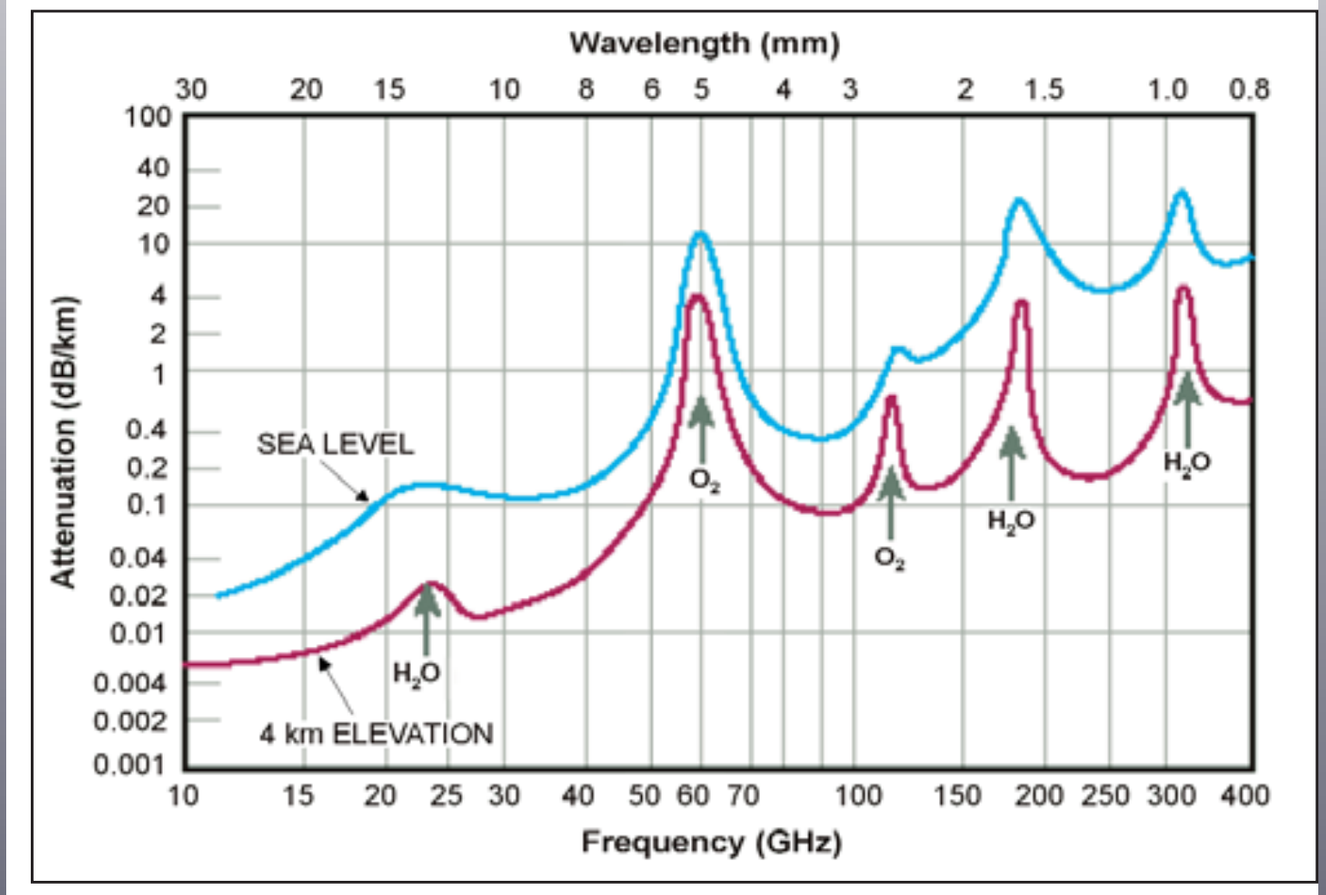
# Channel Performance

***To support Multi-gigabits/s data transfer, the channel need large bandwidth B and large allowable signal power S.***

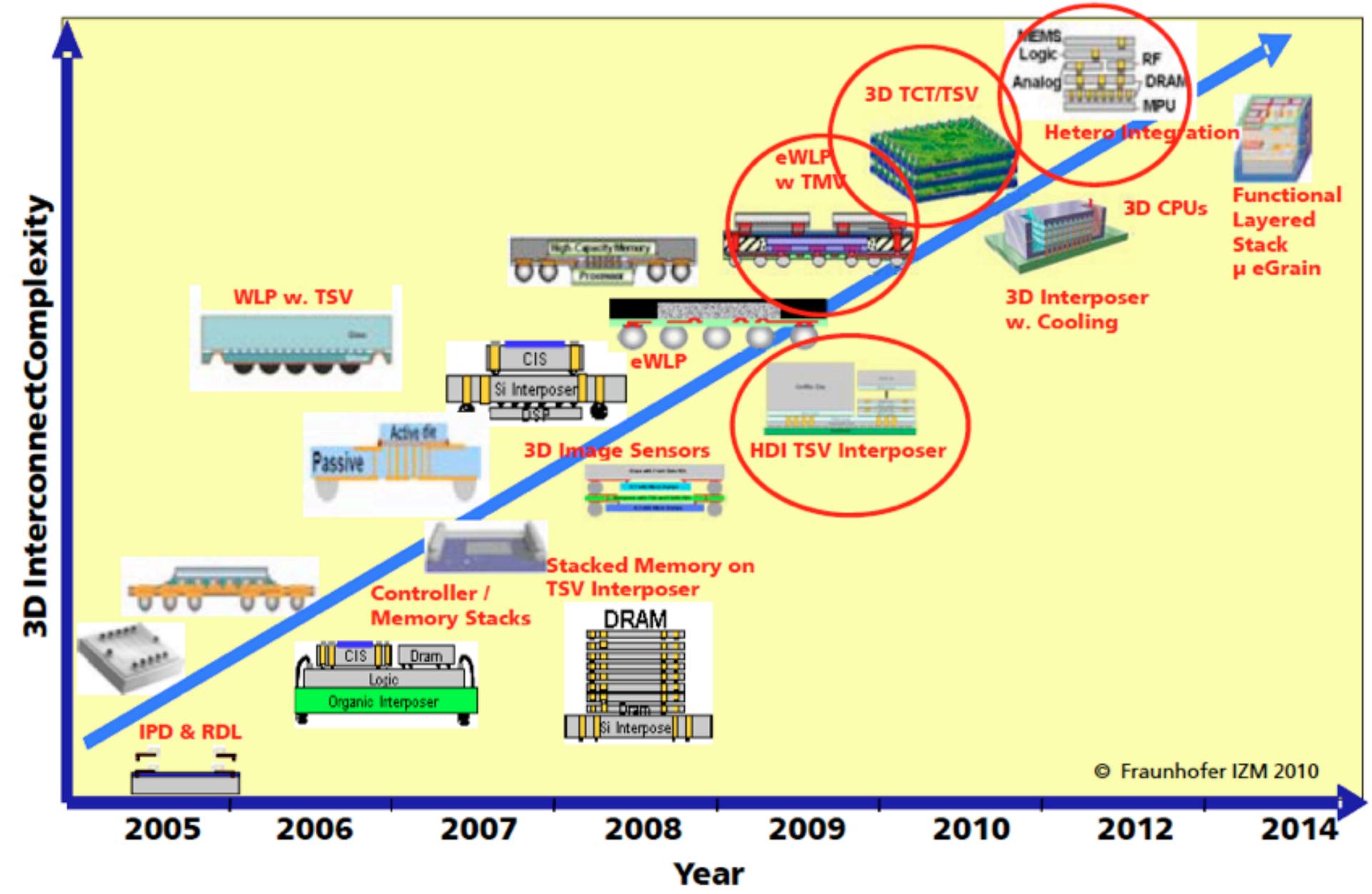
**Shannon's theorem**




**Oxygen attenuation**



# Roadmap 3D WL System Integration







SEMICON West2011

Fraunhofer IZM

# Global Roadmap for 3D Integration with TSV

YOLE DÉVELOPPEMENT

Qualification — First product on the market! — ~ 1 year

## Logic & Analog "3D-SOC/SiP"

Logic only interposers: Logic 32nm / TSI; Logic 28nm / TSI

Low-end ASICs: Logic N; Logic N+2; Analog / RF

Full '3D IC': eFlash; eDRAM; Logic; RF; MEMS; Analog

## Logic + Memory

"wide I/O interfaces"

Baseband / APE — Mobile appliances: LPDDR3 memory; BB / APE

Flash; DRAM; TSI; Logic

HPC: Logic multi-cores

CPU / GPU / MCM: Mem; Logic; TSI

eDRAM; Logic 22-28nm; TSI

FPGA / high perf. ASICs

## HB-LED modules

Silicon Module: LED

LED; Driver

Multi-chip modules: LED; LED; Driver

## Stacked Memories

Stacked DDR3 ≥ 1.6Ghz ≥ 16Gbit

Stacked NAND Flash / NVM

## Power, Analog & RF

Ground TSV: PA / IGBT / MOSFET

RF-SiP: IPD

Embedded IPD: IPD; IPD

Embedded High perf. Analog: PMU; Tx

Power GaN: Sapphire or Silicon

## MEMS & Sensors

Sensor: MEMS; ASIC

3D interposer: ASIC; MEMS; interposer

MEMS cavity: MEMS; Cap

Opto WLP: Sensor

Glass vias: MOEMS

Multi-ASIC: CMOS / MEMS; ASIC; Analog/RF

## CMOS imagers

ShellOP "Edge": SOC CIS

TSV / WLP: SOC CIS

WLOptics: SOC CIS

Consumer BSI: SOC CIS 1.1µm

High-end BSI: CIS; ISP + mem

CIS; DSP; mem

3D integrated CIS + WLAuto-focus

2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 | 2016





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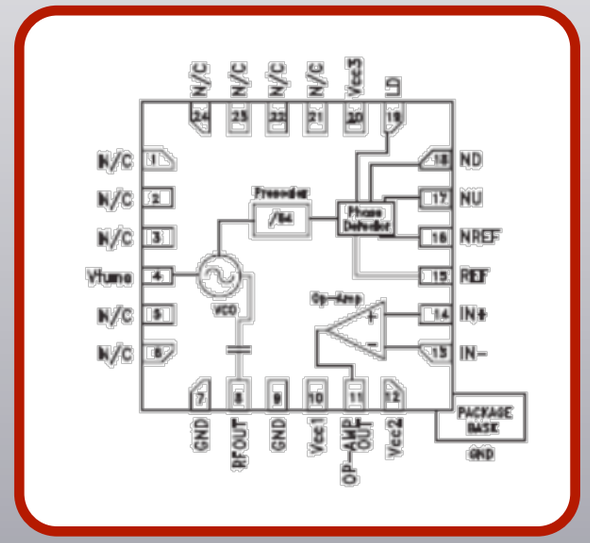
# First tests

## Using Commercial ASIC: Gotmic TX/RX Q060A01

- Reference clock  system test
  - ASIC for 15 GHz reference clock generation
  - Verified locking behavior
  - Signal quality promising
- Receiver operation at 1.7 Gbit/s (60 GHz carrier)
  - $I_{BIAS}$ fine tuning
  - 15 GHz generator for higher sensitivity
  - External reference transmitter system used
  - Binary phase shift keying applied




Fraunhofer Heinrich Hertz Institute

D. Wiedner@Physics at Terascale 2012